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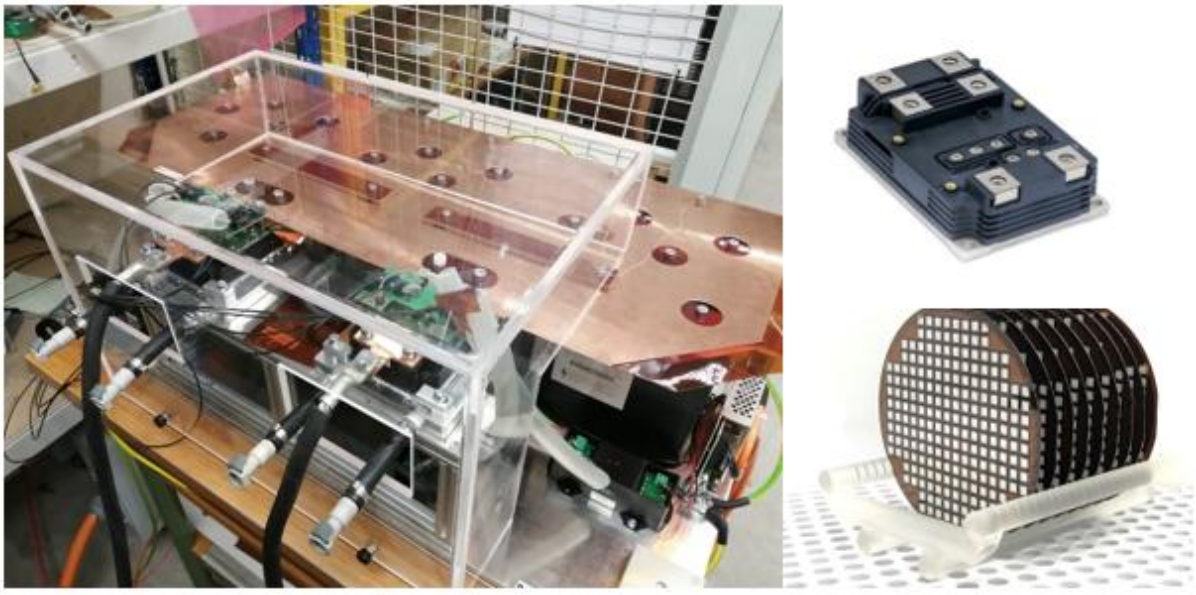
Final report from 28 November 2025

SiC-MILE

SiC Medium Voltage Devices



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Summary

The development of energy efficient technologies is not only a major concern for sustainable growth, but also an important economic issue in societies facing increasing electricity energy prices. A recommended strategy to achieve such a goal is to direct efforts towards the development of technologies used in high-power electronic converters since a significant part of global electrical energy consumption is converted and lost in those systems. Since about 40-45% of the global electrical energy is consumed in motors, with large part of it concentrated into industrial and transport applications. Medium voltage power converters are strongly present in such applications, thereby posing a great potential for global energy saving. As the building blocks for the power electronics converters, power semiconductors play a crucial role into improving energy conversion efficiency. Power semiconductors based on Silicon carbide (SiC) can strongly reduce the power losses of converters compared to mainstream Si technology. The SiC-MILE project aimed to demonstrate a technology to enable the future development of medium voltage (MV) SiC MOSFETs, power modules and railway converter products, focusing on the 3.3 and the 6.5 kV voltage classes.

The design and processing of the 3.3 and 6.5 kV SiC chips, as well as the packaging, the electrical evaluation of the chips on wafer and module level and their reliability have been detailed in this report. Furthermore, the construction of a dedicated converter test bench to characterize the Si and SiC power modules losses under real converter operations with highly accurate thermal and electrical methods has been developed.

The SiC-MILE was able to achieve the following results, which are in accordance to the proposed deliverables:

Prototypes of 3.3kV and 6.5kV SiC MOSFETs were successfully manufactured in the product line of Hitachi Energy. The electrical parameters were analyzed. TCAD simulations were performed to optimize the cell layout and to find the most suitable parameters. Then the first MOSFET devices were fabricated. For the 3.3kV devices two learning cycles were concluded, where the channel profiles, channel length and JTE dose was optimized. The V_{th} values are slightly dispersed between 2.0V-3.0V. The Rds,on values are between 150mOhm-250mOhm, and the leakage is for all devices between 1-10 uA. For the 6.5kV MOSFET devices the focus of the optimization was mainly on the termination design. Different p+ rings as well as JTE doses were used to find the most optimum device. Modules were fabricated from the most suitable dies and were characterized. It was then successfully demonstrated Si and SiC modules at 3.3 kV and 6.5 kV, with electrical characterization validating their suitability for MV applications.

Further, a demonstrator of a 3.3kV Si and SiC MV converter has been built at the FHNW, including capabilities for thermal and electrical characterization of energy losses over a wide range of frequencies and different gate resistance. The goal was to extract the converter losses under a range of parameters that can then be applied for different train topologies and systems. The characterized energy losses where then used to calibrate a railway SiC converter using different topologies, frequency operation, cooling temperatures and drive cycles. In comparison to a Si railway converter, the SiC converter exhibits higher efficiency and load ability over a wide range of frequencies because of the lower energy losses. This allows to not only build smaller systems because of reduced cooling and magnetics needs, but also to allow longer autonomous range in trains featuring batteries. Whereas the 6.5kV SiC modules have been fabricated, they have failed during tests in the converter, and its development will continue further towards product qualification.

As a further important result of this project, we have performed the first detailed LCA studies of SiC power semiconductors, which have shown that the new technology compared to Si mainstream exhibits significantly lower equivalent CO2 emission during lifecycle, in both manufacturing and usage phases. The usage phases during lifetime has the highest contribution to the significant lower CO2 footprint of SiC. Notably, although the substrate grey energy per module of SiC is higher than Si, the front-end grey energy is significantly lower because the current density of SiC chips is higher, and SiC modules do not require an extra Si anti parallel diode.

And finally, we were able to demonstrate a staggering reduction in energy losses between 40 and 75% in SiC traction converters compared to currently available Si based commercial technologies, depending on the drive cycle and topology conditions. If a condition of 50% lower losses is considered, this would correspond to a 13 GWh/yr electricity energy saving in Switzerland, which corresponds to almost the total energy generated by the Swiss Beznau (KKB) and Gösgen (KKB) nuclear power plants combined per year.

Zusammenfassung

Die Entwicklung energieeffizienter Technologien ist nicht nur ein wichtiges Anliegen im Hinblick auf ein nachhaltiges Wachstum, sondern auch eine wichtige wirtschaftliche Frage in Gesellschaften, die mit steigenden Strompreisen konfrontiert sind. Eine empfohlene Strategie zur Erreichung dieses Ziels besteht darin, die Anstrengungen auf die Entwicklung von Technologien zu richten, die in elektronischen Hochleistungsumrichtern eingesetzt werden, da ein erheblicher Teil des weltweiten Stromverbrauchs in diesen Systemen umgewandelt wird und verloren geht.
Etwa 40-45 % der weltweiten elektrischen Energie wird in Motoren verbraucht, wobei ein großer Teil davon in Industrie- und Verkehrsanwendungen anfällt. Mittelspannungsstromrichter sind in solchen Anwendungen stark vertreten und stellen somit ein großes Potenzial für globale Energieeinsparungen dar. Als Bausteine für die Leistungselektronik spielen Leistungshalbleiter eine entscheidende Rolle bei der Verbesserung der Energieumwandlungseffizienz.
Leistungshalbleiter auf der Basis von Siliziumkarbid (SiC) können die Leistungsverluste von Umrichtern im Vergleich zur herkömmlichen Si-Technologie stark reduzieren. Ziel des SiC-MILE-Projekts war es, eine Technologie zu demonstrieren, die die künftige Entwicklung von Mittelspannungs-SiC-MOSFETs, Leistungsmodulen und Bahnstromrichterprodukten ermöglicht, wobei der Schwerpunkt auf den Spannungsklassen 3.3 und 6.5 kV lag.
Das Design und die Verarbeitung der 3.3- und 6.5-kV-SiC-Chips sowie das Packaging, die elektrische Bewertung der Chips auf Wafer- und Modulebene und ihre Zuverlässigkeit werden in diesem Bericht ausführlich beschrieben. Darüber hinaus wurde ein spezieller Umrichterprüfstand entwickelt, um die Verluste von Si- und SiC-Leistungsmodulen im realen Umrichterbetrieb mit hochgenauen thermischen und elektrischen Methoden zu charakterisieren.
Mit dem SiC-MILE konnten die folgenden Ergebnisse erzielt werden, die mit den vorgeschlagenen Zielen übereinstimmen:
Prototypen von 3.3 kV und 6.5 kV SiC-MOSFETs wurden erfolgreich in der Produktlinie von Hitachi Energy hergestellt. Die elektrischen Parameter wurden analysiert. Es wurden TCAD-Simulationen durchgeführt, um das Zellenlayout zu optimieren und die am besten geeigneten Parameter zu finden. Dann wurden die ersten MOSFET-Bauelemente hergestellt. Für die 3.3-kV-Bauelemente wurden zwei Lernzyklen durchgeführt, in denen die Kanalprofile, die Kanallänge und die JTE-Dosis optimiert wurden. Die V_{th}-Werte liegen leicht gestreut zwischen 2.0V-3.0V. Die Rds,on-Werte liegen zwischen 150mOhm-250 mOhm, und die Leckage liegt bei allen Bauteilen zwischen 1-10 uA. Bei den 6.5kV-MOSFET-Bauelementen lag der Schwerpunkt der Optimierung vor allem auf dem Entwurf der Anschlüsse. Es wurden verschiedene p+-Ringe sowie JTE-Dosen verwendet, um das optimale Bauteil zu finden. Aus den am besten geeigneten Chips wurden Module hergestellt und charakterisiert. Anschließend wurden Si- und SiC-Module bei 3.3 kV und 6.5 kV erfolgreich demonstriert, wobei die elektrische Charakterisierung ihre Eignung für MV-Anwendungen bestätigte.

Darüber hinaus wurde am FHNW ein Demonstrator eines 3,3-kV-Si- und SiC-Mittelspannungswandlers gebaut, der über die Möglichkeit zur thermischen und elektrischen Charakterisierung von Energieverlusten über einen weiten Frequenzbereich und unterschiedliche Gate-Widerstände verfügt. Das Ziel war es, die Umrichterverluste unter einer Reihe von Parametern zu extrahieren, die dann für verschiedene Zugtopologien und Systeme verwendet werden können. Die charakterisierten Energieverluste wurden dann zur Kalibrierung eines Eisenbahn-SiC-Wandlers mit unterschiedlichen Topologien, Frequenzen, Kühltemperaturen und Fahrzyklen verwendet. Im Vergleich zu einem Si-Umrichter weist der SiC-Umrichter aufgrund der geringeren Energieverluste einen höheren Wirkungsgrad und eine höhere Belastbarkeit über einen breiten Frequenzbereich auf. Dies ermöglicht nicht nur den Bau kleinerer Systeme aufgrund des geringeren Kühlungs- und Magnetisierungsbedarfs, sondern auch eine größere autonome Reichweite in Zügen mit Batterien. Die 6.5-kV-SiC-Module wurden zwar hergestellt, sind aber bei Tests im Umrichter gescheitert, so dass dessen Entwicklung bis zur Produktqualifikation fortgesetzt wird.
Als weiteres wichtiges Ergebnis dieses Projekts haben wir die ersten detaillierten LCA-Studien zu SiC-Leistungshalbleitern durchgeführt, die gezeigt haben, dass die neue Technologie im Vergleich zu Si-Mainstream sowohl in der Herstellungs- als auch in der Nutzungsphase deutlich geringere äquivalente CO_2-Emissionen während des Lebenszyklus aufweist. Die Nutzungsphasen während der Lebensdauer

haben den größten Anteil an der deutlich geringeren CO_2-Bilanz von SiC. Bemerkenswert ist, dass die Substrat-Grauenergie pro Modul bei SiC zwar höher ist als bei Si, die Front-End-Grauenergie jedoch deutlich niedriger ist, da die Stromdichte von SiC-Chips höher ist und SiC-Module keine zusätzliche antiparallele Si-Diode benötigen.

Schließlich konnten wir nachweisen, dass die Energieverluste in SiC-Traktionsumrichtern im Vergleich zu den derzeit verfügbaren kommerziellen Technologien auf Si-Basis um 40 bis 75 % geringer sind, je nach Antriebszyklus und Topologiebedingungen. Wenn man von 50 % geringeren Verlusten ausgeht, würde dies einer Energieeinsparung von 13 GWh/Jahr in der Schweiz entsprechen, was fast der gesamten Energie entspricht, die von den schweizerischen Kernkraftwerken Beznau (KKB) und Gösgen (KKB) zusammen pro Jahr erzeugt wird.

Résumé

Le développement de technologies à haut rendement énergétique n'est pas seulement une préoccupation majeure pour la croissance durable, mais aussi une question économique importante dans les sociétés confrontées à l'augmentation des prix de l'énergie électrique. Une stratégie recommandée pour atteindre cet objectif consiste à orienter les efforts vers le développement de technologies utilisées dans les convertisseurs électroniques de haute puissance, étant donné qu'une part importante de la consommation mondiale d'énergie électrique est convertie et perdue dans ces systèmes. En effet, environ 40 à 45 % de l'énergie électrique mondiale est consommée par les moteurs, dont une grande partie est concentrée dans les applications industrielles et de transport. Les convertisseurs de puissance à moyenne tension sont très présents dans ces applications, ce qui représente un grand potentiel d'économie d'énergie au niveau mondial. En tant qu'éléments constitutifs des convertisseurs électroniques de puissance, les semi-conducteurs de puissance jouent un rôle crucial dans l'amélioration de l'efficacité de la conversion de l'énergie. Les semi-conducteurs de puissance basés sur le carbure de silicium (SiC) peuvent réduire considérablement les pertes de puissance des convertisseurs par rapport à la technologie Si classique. Le projet SiC-MILE visait à démontrer une technologie permettant le développement futur de MOSFET SiC moyenne tension (MV), de modules de puissance et de convertisseurs ferroviaires, en se concentrant sur les classes de tension 3.3 et 6.5 kV.

La conception et le traitement des puces SiC de 3.3 et 6.5 kV, ainsi que l'emballage, l'évaluation électrique des puces au niveau des plaquettes et des modules et leur fiabilité ont été détaillés dans ce rapport. En outre, la construction d'un banc d'essai de convertisseur dédié pour caractériser les pertes des modules de puissance Si et SiC dans des opérations de convertisseur réelles avec des méthodes thermiques et électriques très précises a été développée.

Le SiC-MILE a permis d'obtenir les résultats suivants, qui sont conformes aux résultats attendus :

Des prototypes de MOSFET SiC de 3.3 kV et 6.5 kV ont été fabriqués avec succès. Les paramètres électriques ont été analysés. Des simulations TCAD ont été réalisées pour optimiser la disposition des cellules et trouver les paramètres les plus appropriés. Les premiers dispositifs MOSFET ont ensuite été fabriqués. Pour les dispositifs de 3.3 kV, deux cycles d'apprentissage ont été menés à bien, au cours desquels les profils et la longueur des canaux ainsi que la dose de JTE ont été optimisés. Les valeurs de Vth sont légèrement dispersées entre 2.0V et 3.0V. Les valeurs de Rds,on sont comprises entre 150mOhm-250mOhm, et la fuite est pour tous les dispositifs comprise entre 1 et 10 uA. Pour les dispositifs MOSFET de 6,5 kV, l'optimisation s'est principalement concentrée sur la conception de la terminaison. Différents anneaux p+ ainsi que des doses JTE ont été utilisés pour trouver le dispositif le plus optimal. Des modules ont été fabriqués à partir des matrices les plus appropriées et ont été caractérisés. Des modules Si et SiC ont ensuite été démontrés avec succès à 3.3 kV et 6.5 kV, la caractérisation électrique validant leur adéquation aux applications MV.

De plus, un démonstrateur de convertisseur moyenne tension 3,3 kV Si et SiC a été construit au FHNW, qui a la capacité de caractériser thermiquement et électriquement les pertes d'énergie sur une large gamme de fréquences et différentes résistances de grille. L'objectif était d'extraire les pertes du convertisseur en fonction d'une gamme de paramètres qui peuvent ensuite être appliqués à différentes topologies de train et à différents systèmes. Les pertes d'énergie caractérisées ont ensuite été utilisées pour calibrer un convertisseur SiC ferroviaire en utilisant différentes topologies, fréquences de fonctionnement, températures de refroidissement et cycles d'entraînement. Par rapport à un convertisseur ferroviaire Si, le convertisseur SiC présente un rendement et une capacité de charge plus élevés sur une large gamme de fréquences en raison des pertes d'énergie plus faibles. Cela permet non seulement de construire des systèmes plus petits grâce à la réduction des besoins en refroidissement et en magnétisme, mais aussi d'augmenter l'autonomie des trains équipés de batteries. Alors que les modules SiC de 6,5kV ont été fabriqués, ils ont échoué lors des tests dans le convertisseur, et son développement se poursuivra jusqu'à la qualification du produit.

Autre résultat important de ce projet, nous avons réalisé les premières études ACV détaillées sur les semi-conducteurs de puissance en SiC, qui ont montré que la nouvelle technologie, comparée au Si

traditionnel, présente des émissions équivalentes de CO_2 nettement inférieures pendant le cycle de vie, tant dans la phase de fabrication que dans la phase d'utilisation. Les phases d'utilisation pendant la durée de vie contribuent le plus à la réduction significative de l'empreinte CO_2 du SiC. Il convient de noter que, bien que l'énergie grise du substrat par module de SiC soit supérieure à celle du Si, l'énergie grise de l'étage d'entrée est nettement inférieure car la densité de courant des puces SiC est plus élevée et les modules SiC ne nécessitent pas de diode antiparallèle Si supplémentaire.

Enfin, nous avons pu démontrer une réduction stupéfiante des pertes d'énergie entre 40 et 75 % dans les convertisseurs de traction en SiC par rapport aux technologies commerciales basées sur le Si actuellement disponibles, en fonction du cycle d'entraînement et des conditions topologiques. Si l'on considère une réduction de 50% des pertes, cela correspondrait à une économie d'énergie électrique de 13 GWh/an en Suisse, ce qui correspond à la quasi-totalité de l'énergie produite par les centrales nucléaires suisses de Beznau (KKB) et de Gösgen (KKB) combinées par an.

Main findings («Take-Home Messages»)

1. Medium-voltage SiC MOSFET modules can significantly reduce energy losses in industrial drives. This translates into substantial cost and sustainability benefits.
2. The project successfully developed and tested 3.3kV and 6.5kV SiC modules at Hitachi Energy Ltd. and FHNW. These demonstrators proved the feasibility and performance advantages of SiC technology for high-power applications.
3. SiC-based traction converters can achieve up to 60% less energy losses compared to Si-based technologies.
4. Life cycle assessments showed much lower CO_2 emissions for SiC modules.
5. SiC-MILE established the first European supply chain and technology platform for MV SiC MOSFET modules. This positions Europe as a leader in energy-efficient power electronics for industry and transport.

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List of abbreviations

SFOE	Swiss Federal Office of Energy
AMPERE	Name of a previous SFOE-funded project related to SiC MOSFET development.
CH	Switzerland (country code, used in addresses)
DC	Direct Current (used in context of DC link voltage)
FACTS	Flexible AC Transmission Systems
FHNW	Fachhochschule Nordwestschweiz
HV	High Voltage
HVDC	High Voltage Direct Current
IC	Collector Current (used in switching waveform context)
ICES	Drain Leakage Current (test parameter for modules)
IGBT	Insulated Gate Bipolar Transistor
JTE	Junction Termination Extension (edge termination technique in MOSFETs)
KKB	Kernkraftwerk Beznau/Gösgen (Swiss nuclear power plants)
LS	Low Side (used in module characterization)
LV	Low Voltage
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor.
MV	Medium Voltage
R&D	Research and Development
RBSOA	Reverse Bias Safe Operating Area
Rg	Gate Resistance (external resistor for gate control)
Rds,on	On-State Resistance (MOSFET parameter)
RT	Room Temperature
Si	Silicon
SiC	Silicon Carbide
TRL	Technology Readiness Level
BR	Breakdown Voltage (MOSFET parameter)
VCE	Collector-Emitter Voltage
VGS	Gate-Source Voltage
Vth	Threshold Voltage (MOSFET parameter)
WBG	Wide Bandgap (semiconductor technology)

1 Introduction

1.1 Context and motivation

The vision of the SiC-MILE project is to establish a technology to enable the future development of medium voltage SiC MOSFET products, targeting the 3.3 and the 6.5kV voltage classes. The material properties of SiC enable the fabrication of power semiconductors with superior on resistance for equivalent blocking voltage, which, in turn, goes well beyond fundamental limit of Si technology, and very high frequency operation. Recently, the SFOE funded project AMPERE demonstrated the first prototypes of SiC MOSFET rated at 6.5 and 10kV at the Hitachi Hitachi Energy Corporate Research Center and the FHNW in Switzerland, reaching a major step towards the implementation of these devices (Figure: 1). The devices rated for Medium Voltage (MV) applications will have a major impact on future electrical energy management by means of medium voltage power electronics, where massive investments will be implemented over the coming decades. This will result in benefits not only for the infrastructure across Switzerland, but also provide a low-cost, low-carbon, and high-robust energy to society.

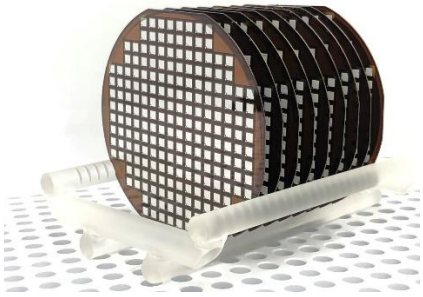
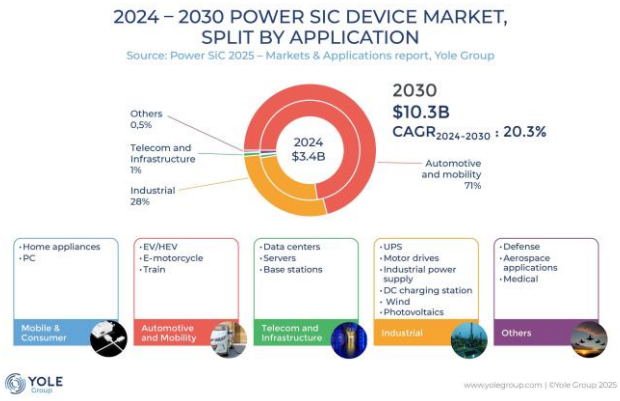


Figure: 1: SiC MOSFET wafers fabricated from SFOE funded AMPERE project.

Driven by the need of energy efficient technologies for sustainable growth, the market of SiC reached about 3.8B US$ in 2024 with the forecast to reach 10.3B US$ by 2030, featuring a CAGR of more than 20% in the period (Figure: 2 left). In 2024, 41% of the market was dominated by automotive applications, followed by 27% from industrial systems. 46% of all the material used was SiC and the market expansion is mainly driven by a rise in 32% in EV adaptation, a 21% increase in smart grid infrastructure and a 17% uptick in 5G base station installation. The transition for the implementation of SiC in a higher variety of applications is also driven by the progress of the transition from 6” to 8” SiC wafers in 2024. Qualification activities of these larger wafers are currently running across the industry aiming for a larger employment by 2026. SICC has accelerated the 8” wafer availability through delivery of their wafers to the open market. Another trend that has dominated the year of 2025 is the transition of internally managing most of the SiC value chain, meaning that integrating the design, device manufacturing and packaging to fulfill the requirements of the automotive customers.

Although a significant part of the growth is pushed by the EV technologies at the LV range, MV SiC technology will significantly develop in a series of applications. From the exemplary market study, MV SiC will correspond to at least 10% of the market. However, those Figures are highly underestimated because it assumes low availability of MV SiC products in the market. This technology hindering issue will be tackled in this project, which will speed the time to market of the MV SiC modules up and thus to further increase market share. Figure 2(right) shows the application of SiC technologies and its GaN and Si counterparts for a wide range of conversion power and operating frequencies. MV SiC devices targeted in this project will be implemented in traction, FACTs, HVDC light, wind and MV industrial drives, which is a multi-billionaire market worldwide and heavily present in Switzerland. The availability of SiC MV modules for example will certainly speed up the implementation of new converter technologies into those applications.

a



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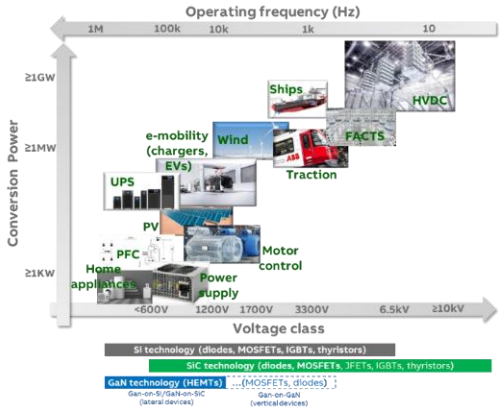


Figure: 2: SiC market forecast (Yole SiC report, 2025 From EV to AR/VR: SiC's expanding reach powers new tech waves (a) Distribution of applications vs. voltage class (lower axis) and operating frequency (upper axis). (b) The applications-related range of Si, SiC and GaN technologies is also shown for comparison http://www.yole.fr/iso_album/illus_power_sic_marketforecast_yole_nov2020.jpg) .

Together with advances in power modules design, the use of SiC technology in rail traction converters can reduce losses as well as enable reduction in size and weight. In wind turbine converters, the use of MV SiC can lead to lower total losses as well as benefits in terms of lower turbine nacelle size and tower heights. For Mega-Watt range applications such as HVDC, the deployment of SiC technology can also deliver substantial benefits in terms of energy efficiency coupled with reductions in size, weight and cost of the power system.

Figure 3 shows the major players in MV SiC technology, indicating that in Europe, Hitachi Energy is the only technology developer. Notice that very large European power semiconductor corporations such as Infineon, STMicroelectronics and ON-semi are not in the market. This is explained by the fact

that Hitachi Energy is the technology leader in MV and HV power semiconductors, whose strong position is underpinned by its pioneering on Si thyristor and IGBT technologies. So far, the most explored technology in Hitachi Energy is the 3.3 kV class.

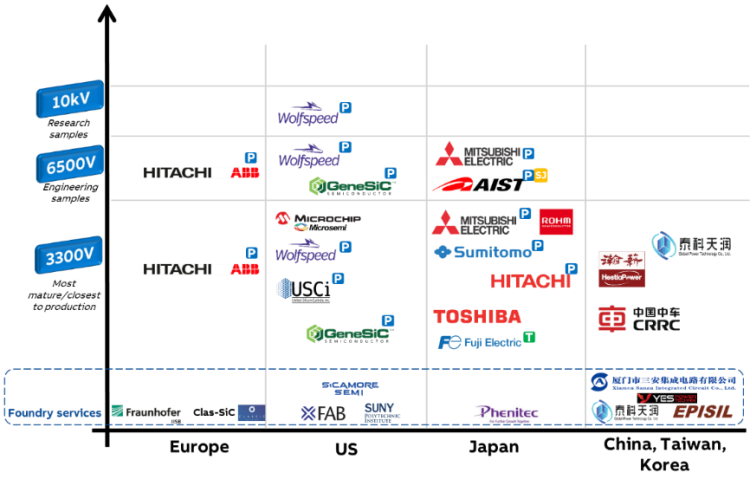


Figure: 3: Map of SiC semiconductor player for voltage ranges of 3.3kV and higher.

Figure 4 depicts a table with all available 3.3 kV technologies in the market and its descriptions from the main competitors of Hitachi Energy. It is important to notice that all those are not commercially available and are on the stage of technological development. Also, most of them reassemble LinPak modules as the new industrial standard.

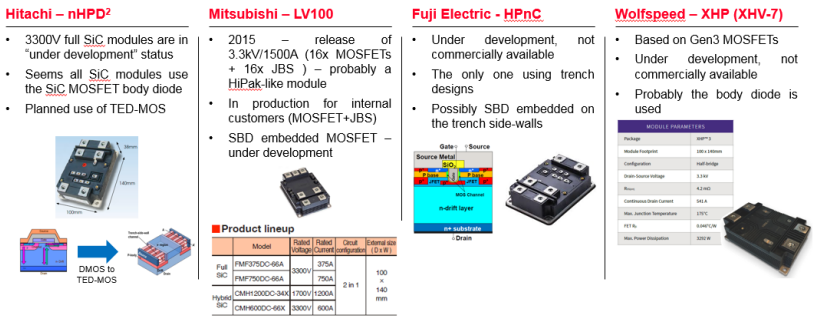


Figure: 4: Summary of 3.3kV full SiC power modules of competitors.

Recently, Hitachi Energy have developed an innovative MOS gate stack technology based on high-k dielectrics for power electronic devices. For the first time, we have successfully demonstrated fully functional vertical power SiC MOSFETs using high-k-based MOS interfaces. The recent results on 1.2kV-rated SiC MOSFETs showed unrivalled levels of threshold voltage stability during static and dynamic stress operation using Si-like gate voltage swings of +/- 15V.

Through a collaboration between the FHNW and Hitachi Energy Semiconductors, SiC-MILE seeks to establish the MV technology platform before moving to a potential product, and thus to enable development of national energy-related WBG-based HV power electronics applications. This collaboration initially started in the SFOE project - number SI/501529 – Fortgeschrittenes SiC-Material für Leistungs-Elektronikgeräte – link: https://www.aramis.admin.ch/Texte/?ProjectID=40193. In this previous project, primary technology platforms for state-of-the-art MV discrete SiC devices have been developed, encompassing simulations, microtechnology processes, integration schemes and characterization systems. To achieve the SiC Mile ambitious goals, the FHNW with long experience in applied semiconductor devices and power electronics will be technologically backed by Hitachi Energy`s leadership position in high power devices developed in Lenzburg, as well as the unique know-how in power electronics applications from several Swiss-based business units. Hitachi Energy, in fact, is a leader in manufacturing high power IGBTs featuring high performance and reliability, with decades of R&D experience, and thus the right European company to tackle this challenge. The FHNW, in turn, sets high support to energy efficient applied research through its “Energy Chance” strategy, including the hosting of a SCCER-FURIES program, NRP70 research project (“Swiss transformer”) and some other SFOE SiC-based research projects.

1.1 Purpose of the project

Switzerland is one of the main poles of power electronics technology development in Europe and in the world, which is, in turn, the basis for the vast majority of energy related systems, including rail, renewables, electric vehicles, industrial drives, grid technology and so forth. SiC is the next technological step in power electronics, which is expected to take over significant market share of its Si counterpart because of its undisputable advantage in energy efficiency. One remarkable example is the use of LV SiC MOSFETs in the new Tesla electric cars, substituting the Si IGBT technology to provide longer all electric range. Whereas the LV SiC market (up to 1.7 kV class) is in full commercialization in renewables and EVs, the MV SiC technology (3.3 to 6.5 kV) is only offered as development samples.

The purpose of SiC-MILE is to demonstrate a new generation of 3.3 and 6.5 kV SiC MV chips and packages with required performance, reliability and costs, and to validate them in a converter demonstrator to assess their potential in MV drive applications. The results will be further evaluated for estimating the energy saving potential in Switzerland in traction applications. Such products are not yet available in today’s market, and its industrialization will further enable the development of new MV applications featuring SiC devices (e.g. MV drives and distributor transformers), which, in turn, will allow significant reduction of losses.

A significant research and development effort on material processing, microfabrication and process integration must be made to achieve reliable and robust chip designs with optimal performance and yield.

Optimized gate oxide stacks to reduce leakage current, optimal epi-layer design to minimize on-resistance, and robust termination designs are some of the state-of-the-art innovations required in this project. Additionally, these chips must be electrically interconnected in a highly optimized power module packaging to achieve ultra-low stray inductances, compactness, equal current ratio sharing between the chips and high robustness and reliability. Implementing new materials for chip-substrate connection (e.g. silver sintering) is an additional innovation to the SiC technology module presented in this project. The SiC Mile project also innovates in designing a customized test bench converter to characterize the power modules under converter operation like a real application. Such a test allows the comparison of SiC and Si technologies under identical conditions to accurately depict WBG technology's potential.

Hitachi Energy Semiconductors is an important supplier of components to ABB units based in Switzerland, such as Medium Voltage Drives, FACTS and High-power rectifiers. Directly after successfully passing technology development phase, first demonstrators will be presented to these end customers. The project will therefore generate nationally further revenues at the application side and help maintain high technology manufacturing in Switzerland. This will speed the development of applications that significantly influence energy efficiency and CO2 emission reduction in Switzerland. As such, the project poses the following relevance:

Technology/scientific relevance:

1. Generation of innovative platforms in SiC based chip/module/converter technology.
2. Impact the development of SiC converter technology in application universities/companies in Switzerland and abroad.
3. Support significant increase of energy efficiency and reduction of CO2 emission in Switzerland as a basis technology for efficient energy systems, for example in traction converters of trains or industrial drives.

Strategic/economic relevance:

1. Supports the technology development at Hitachi Energy semiconductor business unit in Switzerland, which provides more than 550 jobs, and Figure:s as a large exportation company for energy efficient power semiconductors.

2. Enable the development of new SiC products based in Switzerland.

3. Enable the nucleation of a unique supply chain in Switzerland for the development of MV drive products based on SiC, both at Hitachi Energy and ABB Drives.

4. Enable of new system products such as trains or MV industrial drives that will profit end customers.

5. Reduced long-term in-service degradation, lowering maintenance needs and costs of power electronics systems.

6. Smaller power semiconductor players in Switzerland will further profit from the technology output and the SiC market boost in the country, which will further push product demands.

1.2 Project objectives

The objective of this project is to demonstrate a new technology of railway power system based on advanced SiC power semiconductors. This technology has the potential to strongly reduce energy consumption in Switzerland and worldwide by reducing energy losses for industrial drive applications.

Specifically, the goal is to demonstrate 3.3 and 6.5 kV SiC MOSFETs chips and packaging modules fabricated in an industrial environment, and to validate the technology in a MV power electronics converter demonstrator to estimate loss reduction

Design, processing technology, and development of dedicated measurement systems are within the scope of the project. Hitachi Energy will build on these platforms to rapidly accelerate the technology readiness. The specific targets required to achieve these ambitious objectives are twofold:

1. To fabricate 3.3 and 6.5 kV SiC MOSFET MV module demonstrators in a Si fab, moving the technology from laboratory to fab (TRL 5 to TRL 7-8). This target requires extremely advanced technology of semiconductor manufacturing that involves interdisciplinary sciences such as Chemistry, Physics, Maths and overall engineering. The targets for the chips and power modules are currents rating of around 300 – 400 A, chip switching losses at nominal conditions smaller than 8 mJ and module stray inductance smaller than 30 nH.

2. The research questions for this target address:

    a) What chip/modules designs can fulfil performance, robustness and reliability required for real industrial applications? Intensive simulation and integration development will be performed to deliver the required specifications.
    b) How processes of a Si fab can be adapted to SiC materials? Incorporation of SiC into high volume Si fabs is paramount to achieve cost viability. Owning the fact that processes are different in several cases over more than 200 steps, there will be significant scientific/engineering work to achieve this target.
    c) How to make SiC cost effective? As aforementioned processes and integrations must be cost optimized to compensate for the high costs of SiC substrates.
    d) What are the challenges and advantages of manufacturing SiC from the technology and financial perspectives? The individualities of the technology will be thoroughly assessed.

e) What are the technology advantages of SiC MOSFET modules compared to those based on Si IGBTs? This research question will provide the basis for the applications of the technology.

3. To build a half-bridge converter demonstrator featuring the 3.3 kV and 6.5 kV SiC module technology. This topology is the building block for power electronics and provides most of information needed for the assessment of systems. We target a converter demonstrator efficiency of between 96 – 98 % for the Si IGBT converter and > 99% for the SiC MOSFET converter at similar operating conditions. We will then compare their performance under different operations and as such to access their potential performance in railway applications in Switzerland.

4. The research questions for this target are:

   a) What is the SiC module performance in a converter application? R_{ds}, switching losses, rise and fall time module as well as converter metrics such as stability under constant switching, energy losses and efficiency over switching frequency and power range will be assessed as systematically.
   b) What is the performance of the SiC technology under high frequency switching?

Which applications will mostly profit from the MV SiC technology? This research question must be addressed from the technology and financial perspectives using system simulations. Main applications will be assessed in MV VFD and traction converters. 3.3 kV SiC-based railway traction converters applications are expected to present up to 59 % improvement of the electric-energy loss when compared to Si IGBT-based converters, depending on the drive cycle [1].

2 Approach, method, results and discussion

The SiC Mile project aims to perform a complete product analysis. The project starts with the SiC chip design and power module assembly. Afterwards, the power converter design and experimental testing of the fabricated modules, followed by energy losses investigation in drive-based applications, is performed. Finally, the life cycle analysis is executed (Figure 5).

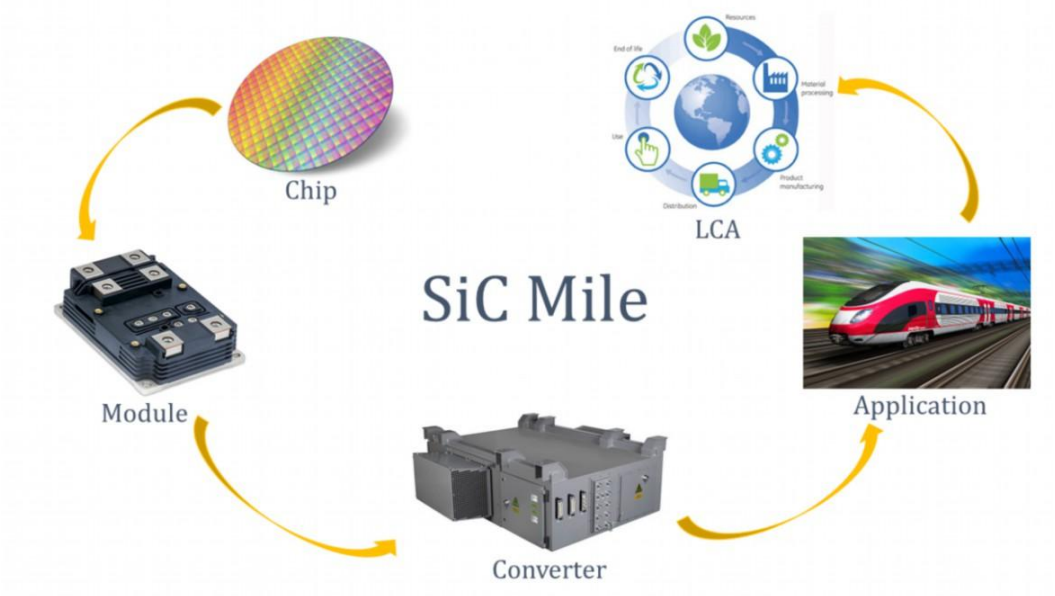


Figure: 5: SiC Mile project methodology overview.

This project flow initially starts with 3.3 and 6.5 kV SiC chip design and packaging. The focus is initially given to fabrication and integration schemes. Then, the chip design steps are elucidated, focusing on epi-layer design, doping profiles and gate oxide optimization. The packaging design is mainly focused on the module stray inductance optimization.

The second part focuses on designing and constructing of the converter test bench to characterize 3.3 and 6.5 kV Si IGBTs modules. The design considerations and two distinct measurement protocols to characterize the converter power losses (thermal and electrical methods) are presented.

The two testbench converters present the following technical parameters:

1) 3.3 kV Si testbench converter: 1.8 kV operating voltage, a maximum current of 300 Arms, maximum switching frequency of around 2 kHz, driving gate voltage of +15V/-10V and inductor load of 2.5 mH.
2) 6.5 kV Si testbench converter: 3.6 kV operating voltage, a maximum current of 300 Arms, maximum switching frequency of around 2 kHz, driving gate voltage of +15V/-10V and inductor load of 2.5 mH.

The first characterization method is based on the thermal exchange method, in which the inlet and outlet cooling fluid temperature and fluid flow are monitored to provide the module power losses. Such a method can provide high accuracy when accurate temperature sensors are used with state-of-the art flowmeters. In addition, power loss characterization with power analyzer equipment is also performed. Both methods together provide improved accuracy and reliable results.

2.1 SiC chip and module development

2.1.1. Development of integration schemes

The SiC MOSFET integration process comprises consecutive fabrication modules which must be properly developed and assembled to achieve the desired chip performance and yield. Indeed, each module is formed by subsequent processing steps that are tested and optimized according to well defined learning cycles. The design of the respective learning platform includes the splitting of processing conditions, where the combination of critical variables and development steps is tested in a different way. The assessment of the resulting matrix allows us to select optimal conditions according to defined design rules and the targeted specifications for the device. In few cases the learning cycles can still be performed using Si wafers. However, most of them require testing on 150mm SiC wafers, not only substrates, but specifically epi-wafers.

Below is an overview of the main fabrication modules and the foremost learning cycles we have implemented during the SiC MOSFET integration:

Table 1: Typical semiconductor processing steps.

Processing Module	**Learning cycle**	**Goal**
Implantation Hard-Mask	Hard-mask layer stack selection/deposition	Proper screening of implantation species
	Hard mask etch	90deg etch profile for accurate implantation regions
Implantations	Implantation profile	Selection of implantation energies and doses for Channel, Source, P-well, Termination, JFET, Pplus, regions
Targets	Targets shape and polarity	Proper alignment of different layers across the process. Critical for right overlapping and desired critical dimensions. Targets must overcome different processing conditions
	Targets etch	Targets depth and sidewalls are very important for signal detection and mask alignment in the Lithography tools
Lithography	Photoresist coating and develop	Combined with exposure energy it allows to reach the critical dimensions in small size features
	Exposure energy	Exposure energy and alignment conditions are key parts of accurate overlapping and feature size of different processing steps

Self-alignment	Layer deposition and dry-etch	Proper self-alignment for screening channel region during source implantation. Critical for channel length definition
Gate Platforms	Gate Oxide surface pre-conditioning	For reducing density of electrically active defects, primary at the interface
	Dielectric material and thickness	Integration of dielectric materials with a large permittivity and large band gap
	Gate metal contact selection	Low Gate resistivity
	Post-depo annealing steps	Improving interplay between Gate metal and Gate dielectric
Insulation	Insulation layer stack selection	To ensure proper source-gate insulation
	Post deposition treatment	Densification of insulation materials
	Layer stack etching	Proper contact opening
Ohmic Contact Formation	Metal layer selection and etch	Appropriate source contact region covering while preventing damage of the gate during post deposition anneal
	Rapid thermal processing	Formation of ohmic contacts with low resistivity according to proposed specifications
Metallization	Metal contact filling	Complete filling of voids at the source contact regions
	Wafer Backside metallization	Good adhesion between the SiC ohmic layer and the metallization layer stack
Passivation	Layer selection and deposition	Suitable protection of the transition and termination area mainly from humidity and particles

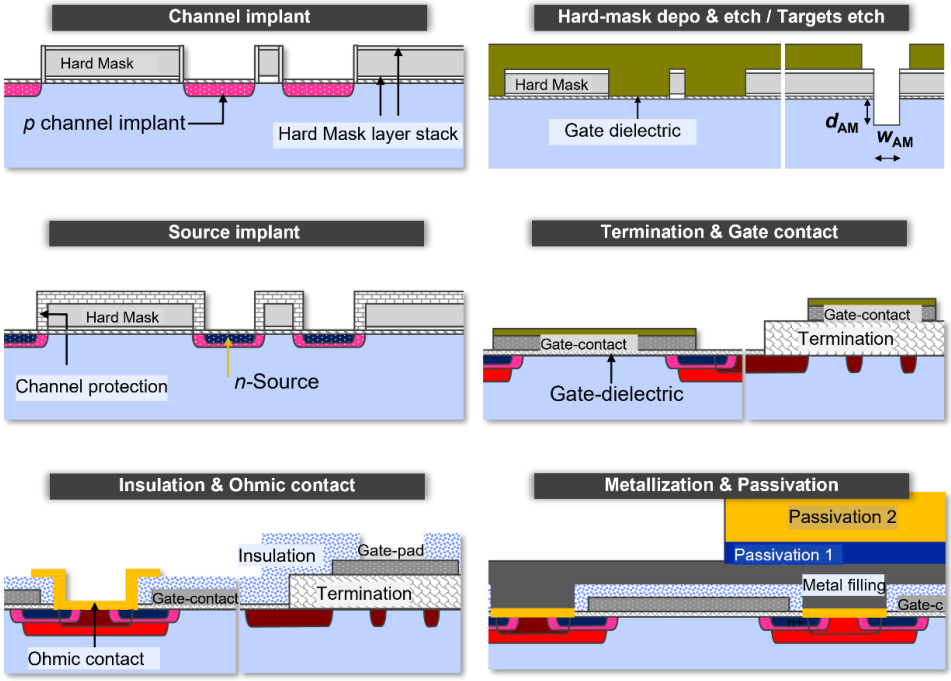


Figure: 6: General overview of most relevant integration steps in the development and manufacturing of SiC MOSFET devices. The different integration steps require several cycles of testing processing conditions and development platforms. The final fabrication router for prototype manufacturing contains about 284 steps.

Development of fab processes

As mentioned in the proposal, the MOSFET fabrication processes developed in Hitachi Energy Research laboratory have been transferred to the Hitachi Energy Semiconductor Si production line. The active MOSFET cell design is typically defined by implantation and self-aligned processes, which ultimately control the minimum feature size that could be achieved in a controllable and repeatable fashion. Here, we have run many short loops experiments where we mostly verified the following critical steps (as schematically described in Figure: 7: ion implantation, self-aligned processing methods, termination are mask etching, gate oxide processing and silicidation of ohmic contacts (both front- and back-side).

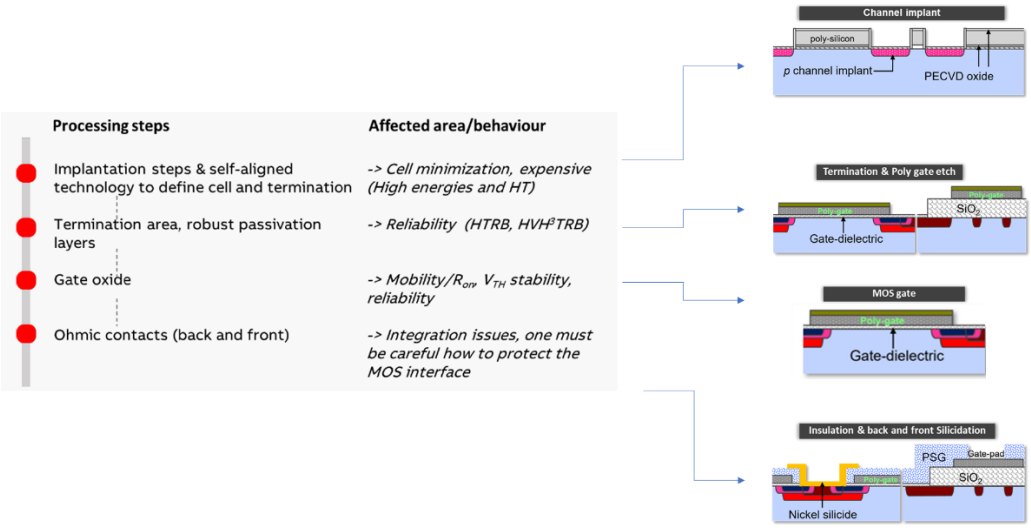


Figure: 7: Schematic chart showing some of the crucial processes needed for the fabrication of a high power SiC MOSFET; schematic cross-sections of a MOSFET during various stages of fabrication are also shown.

To illustrate the gate oxide fabrication and integration aspects, Figure: 8 shows the evolution of the gate dielectric from the first demonstrators to the ones we currently have. As can be noted, the first samples showed increased gate leakage current values and were failing before reaching the nominal gate voltage of VGS=15V. Through improved processing, the last gate dielectric demonstrators show very low leakage current levels and can support VGS=15V. This is an important steppingstone towards the fabrication of reliable high power SiC MOSFETs.

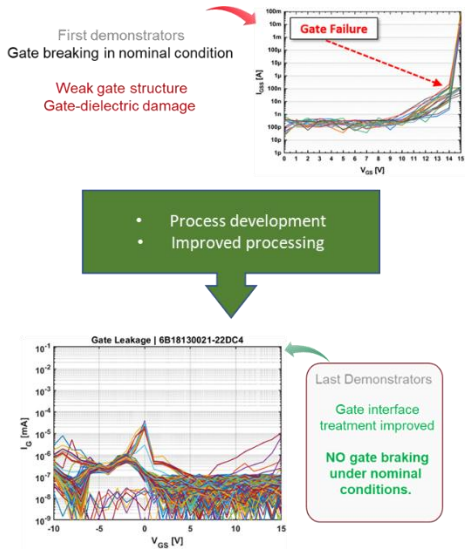


Figure: 8: Evolution of the gate dielectric performance - from the first to the current demonstrators.

2.1.2. Design of the 3.3kV MOSFET

The schematic cross-section of 3.3kV MOSFET active cell is shown in Figure: 9 (a). The 350um of substrate has been modelled by using a resistance (lumped and function of the temperature), which has been added at the drain contact.

To confirm the choice of the epitaxial layer specifications, Ron vs VBR simulations have been run (Figure: 10). This is an important step towards the final MOSFET design as it dictates the performance vs. cost trade-off. Based on these results, the epitaxial layer thickness was confirmed at 30um.

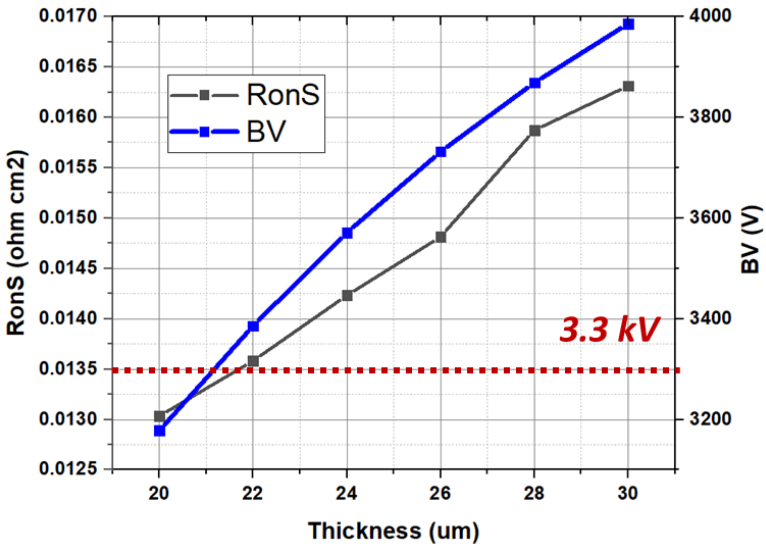
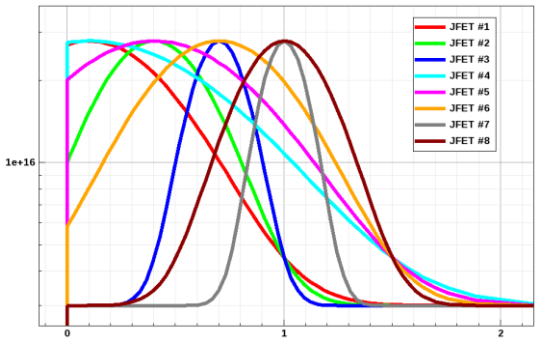


Figure: 9: R_{on} and VBR dependence on epitaxial layer thickness for a 3.3kV-rated MOSFET.

To analyze the influence of the JFET region on the MOSFET performance (Ron vs long term reliability), several JFET profiles have been investigated through extensive TCAD simulations. For the JFET profile,

a Gaussian doping distribution has been used (as shown in Figure: 11). For this investigation, a stripe cell design has been considered. The variation of Ron and field oxide (Eox) for cell pitches of 12 and 14um, respectively, is shown in Figure: 11b. As can be seen, there is clear trade-off between Ron and Eox. This means that the cell pitch dimensions must be carefully chosen towards an optimum on-state/reliability trade-off.

a



b

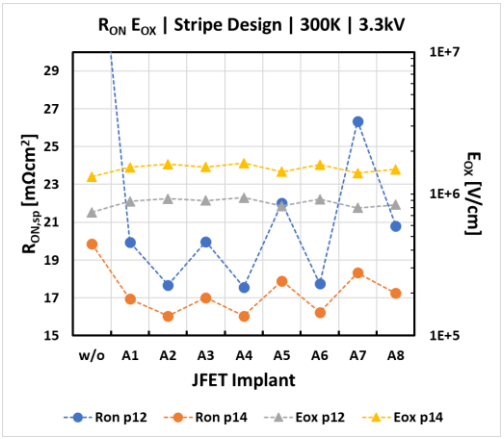
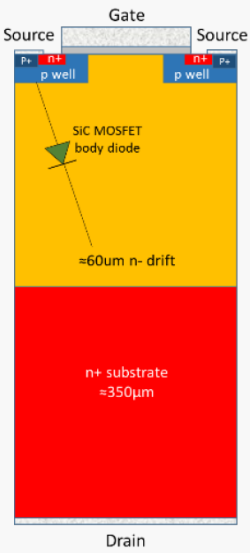


Figure: 10: JFET region profiles investigated (a) and variation if Ron and Eox with JFET region profile, for 12and 14um cell pitches (b).

2.1.3.Design of the 6.5kV MOSFET

The schematic cross-section of 6.5kV MOSFET active cell is shown in Figure: 12 (a). Like the 3.3kV MOSFET case, the SiC substrate has been modelled using a lumped resistance added at the drain contact.

a



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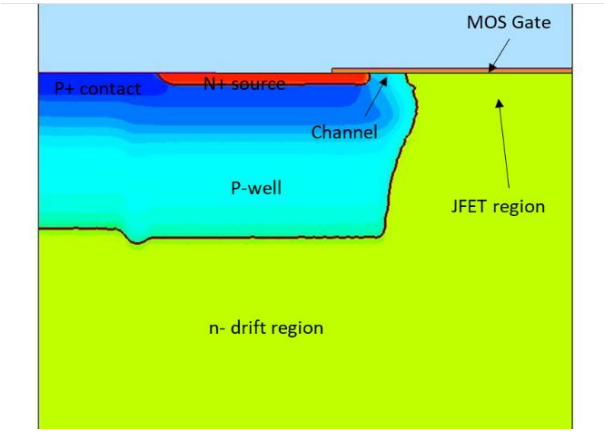
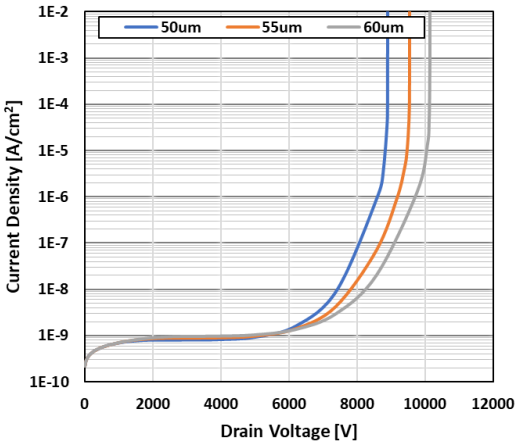


Figure: 11: Schematic cross-section of a 6.5kV MOSFET (a) and TCAD cross-section of the simulated 3.3kV MOSFET active cell (b).

The variation of VBR and Ron values with the thickness of the epitaxial layer is shown in Figure: 13. Based on the simulations results, an epitaxial layer thickness of 55um has been selected.

a



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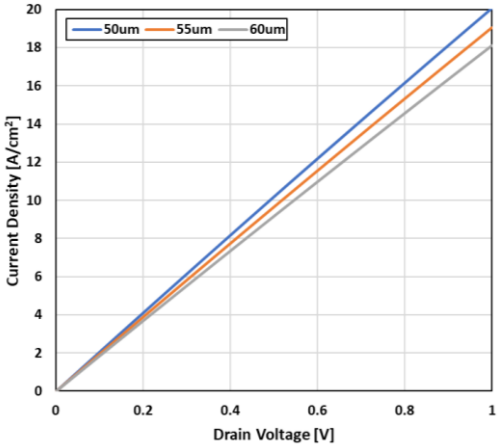


Figure: 12: VBR and Ron dependence on the thickness of the epitaxial layer for a 6.5kV-rated MOSFET.

Starting with the work done and results obtained in the framework of the AMPERE project, we have simulated a JTE-based edge termination for 6.5kV SiC MOSFET. The voltage blocking curves for three different JTE charge doses are plotted in Figure: 14. All three JTE doses give blocking voltages more than 8kV, which demonstrates more than 90% edge termination efficiency.

a

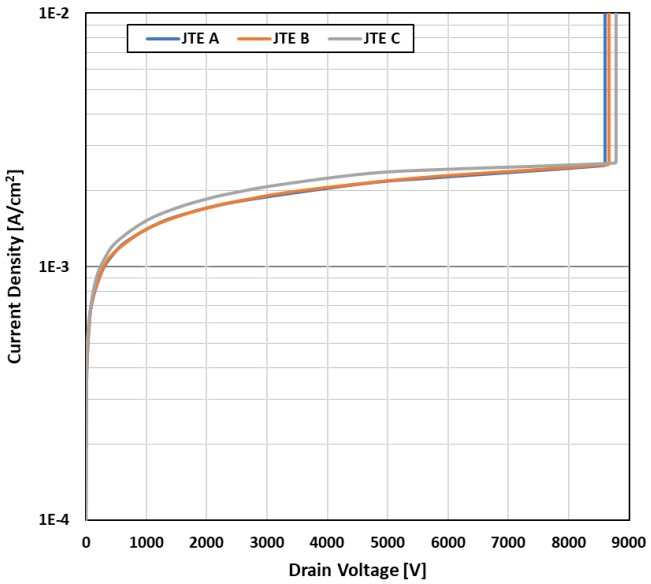


Figure: 13: Blocking curves for a 6.5kV-rated JTE-based edge termination; three different doses have been simulated.

2.2 3.3kV and 6.5kV MOSFET processing of the SiC MOSFETs

2.2.1.3.3kV MOSFET fabrication

In the first lot, we have evaluated the effect of different channel implantation profiles vs the channel length. Typical channel length in literature ranges from 500nm to 1.2um. The channel length we used in the first splits are similar length than the short channel from literature. The implantation profiles for channel and source were chosen based on our TCAD simulations (Figure: 15).

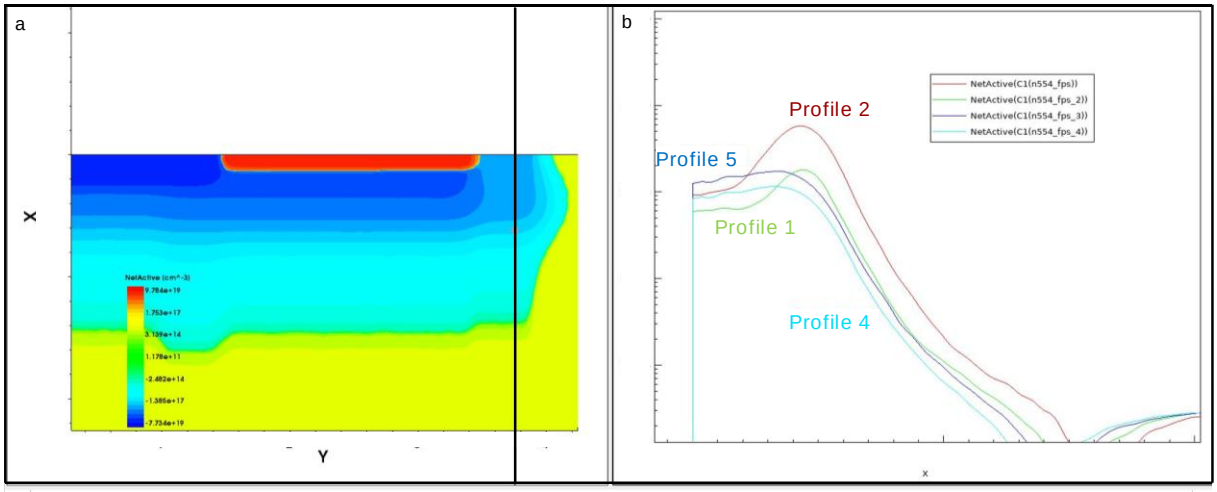


Figure: 14: TCAD simulation of some implantation profiles used during the MOSFET processing.

In the first lot, we were comparing channel length (channel length 1 < channel length 2 (25% longer than channel length 1)) vs different channel implantation profiles in the first step (Table 2).

Table 2: Split table of first 3.3kV lot

Split Number	Channel Profile	Channel length	Source	p-well	JTE
1	Profile 1	Channel length 1	Source 2	p-well 1	1.85x
2	Profile 2	Channel length 1	Source 2	p-well 1	1.85x
3	Profile 3	Channel length 1	Source 2	p-well 1	1.85x
4	Profile 1	Channel length 2	Source 2	p-well 1	1.85x
5	Profile 2	Channel length 2	Source 2	p-well 1	1.85x
6	Profile 3	Channel length 2	Source 2	p-well 1	1.85x

Figure 16 shows the static wafer-level characteristics of the 3.3kV MOSFET at room temperature. The V_{th} for the splits with channel length 1 is slightly higher than the V_{th} value for channel length 2. The biggest difference between the longer and the shorter channel can be observed for channel profile 2. Channel profile 2 for the longer channel length is around 2.5V whereas for the shorter channel decreases to 1.5V. For channel profile 4 the trend is similar, but less pronounced. For channel length the V_{th} value is 1.8 V and for channel length 1 the V_{th} value is 1.4V. For channel profile 1 the opposite trend can be observed. Channel profile 1 vs channel length 1 gives a V_{th} value around 2.1 V whereas channel profile 1 and the longer channel length is yielding in a V_{th} value of 1.6V (Figure: 16a). The Rds,on value is for the shorter channel lower for all channel profiles between 130 mOhm-200 mOhm in comparison to 130 mOhm to 220 mOhm) (Figure: 16b). The results hinted that a longer channel in relation to channel profile 1 or 2 could be interesting for our final split.

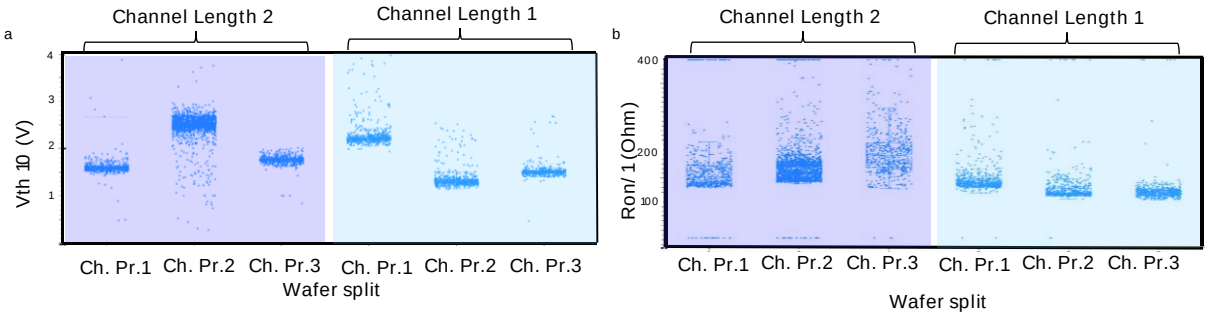


Figure: 15: Static wafer level characteristics at RT for 3.3kV MOSFET with changing channel profile split. (a) V_{th} (b) Ron.

Table 3:Split table of second 3.3kV lots

Split	Channel Profile	Channel length	Source	p-well	JTE
1	Profile 1	Channel length 3	Source 2	p-well 1	1.75x
2	Profile 1	Channel length 3	Source 2	p-well 1	1.95x
3	Profile 2	Channel length 3	Source 2	p-well 1	1.75x
4	Profile 2	Channel length 3	Source 2	p-well 1	1.85x
5	Profile 2	Channel length3	Source 2	p-well 1	1.95x

From the evaluation of the first lot, we found an interesting channel length to channel profile relation. To ensure that we can find the best optimal split, we continued our investigation by increasing the channel length by 20% (channel length 2< channel length 3)(Table 3). We therefore evaluated in the next batch channel profile 1 and 2 in relation to higher JTE implant does vs the longer channel (Table 3). Therefore, one channel length was fixed, and the two best performing channel profiles from Lot 1 were analyzed in comparison to the JTE dose.

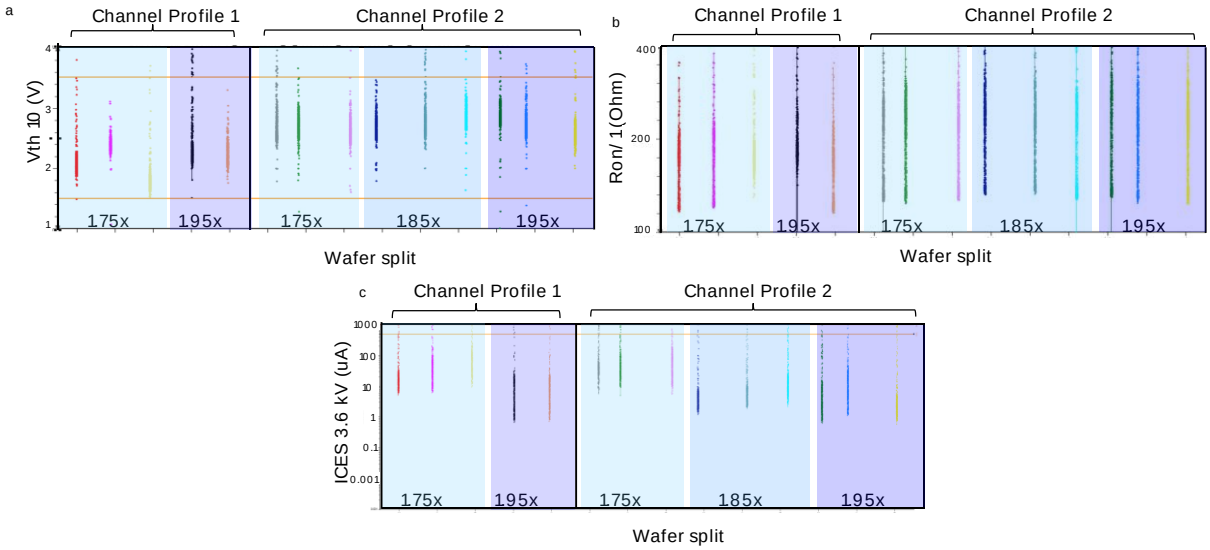


Figure: 16: Static wafer level characteristics at RT for 3.3kV MOSFETs alternating the JTE implantation. (a) V_{th}, (b) Ron/1, (c) ICES.

Figure 17 displays the static room-temperature wafer level characteristics for the different 3.3kV splits. The V_{th} is between 2V and 3V for all the lots, but with higher variation of the lots with channel implantation profile 1 than 2. Additionally, channel implantation profile 2 is leading to lower V_{th} values (1.8V-2.5V) than channel implantation profile 3 (2.5V-3.0V) (Figure: 17a). Considering the Rds,on values we see a similar trend than for the V_{th} values. We have higher spread but lower Rds,on values for channel profile 1 (110-210mOhm) compared to channel profile 2 (110mOhm-300mOhm) (Figure: 17b). The leakage current was the highest among the samples being implanted with JTE 1.75x and decrease for the higher implantations The JTE implantation 1.85x and channel profile 2 is the one with the lowest spread (Figure: 17c). These parameters are selected for the final batch (Table 4).

Table 4: Final split table

Split Number	Channel profile	Channel length	Source	p-well	JTE
Description X	Profile 2	Channel length 3	Source 2	p-well 1	1.85x

In the third lot we then focused on fabricating enough MOSFETs for our module deliveries. We found that channel profile 2 with channel length 3 at a JTE implantation of 1.85x is sufficient to ensure the MOSFET performance needed to build the HV LinPaks for the demonstrator. The V_{th} values are slightly dispersed between 2.0V-3.0V. The Ron values are between 150mOhm-250mOhm, and the leakage is for all devices between 1-10 uA.

2.2.2.6.5 kV MOSFET fabrication

The 6.5kV MOSFETs were based on our 3.3kV MOSFET platform in this project. We choose the same channel length and source implantation than in the 3.3kV platform. In our first lot we cross-examined

some of the parameters that gave promising results in the TCAD simulations. We investigated two different termination designs in correlation to different JTE implantations (Table 5).

Table 5: Split table of second 6.5kV MOSFET lot

Split	Channel Profile	Channel length	Source	Termination design	P plus rings	JTE
1	Profile 3	Channel length 2	Source 2	p-well 1	5	1.30x
2	Profile 3	Channel length 2	Source 2	p-well 1	5	1.65x
3	Profile 3	Channel length 2	Source 2	p-well 1	5	1.75x
4	Profile 3	Channel length 2	Source 2	p-well 1	4	1.75x
5	Profile 3	Channel length 2	Source 2	p-well 1	5	1.85x

Figure 19 displays the static wafer-level results for the 6.5kV MOSFET split at room temperature focusing on the impact of JTE implantations, specifically alternating between termination 1 and termination 2.

The V_{th} is similar for all JTE implantations ranging from 2.0V-3.2V. (Figure: 18a). The smallest Rds,on spread with the highest Rds,on value 500-600 mOhm can be observed for the JTE 1.85x. The Rds,on value is similar for split 2,3 and 4 exhibiting a larger spread in Rds,on values, with main population around 400-500 mOhm. For the JTE split 1.3x is the Rds,on value 490-520 mOhm (Figure: 18b).

The lowest leakage current at 6.5kV (Figure: 18c) can be achieved for the devices with JTE 1.65x 10-100 uA indicating a strong blocking capability. The leakage slightly increases for the JTE 1.65x and is at the limit of 1000 mA for the JTE 1.75x implantation. The split with termination design T2 is unfortunately not giving the necessary blocking capabilities. The chips leakage current is already too high at 2.0 kV, therefore the split 1.75x JTE with termination 2 (T2) are excluded from the next round. The split 5 with a JTE implantation of 1.85x and termination T1, will also not be considered further, as the leakage current is too high already at 2.0kV as well. The leakage current at 6.5kV with the lowest spread can be achieved for the devices with JTE 1.3x T2 ICES= 50uA. The leakage slightly increases for the JTE 1.75x and is at the limit of 1000 mA for the JTE 1.75x implantation (Figure: 18c)

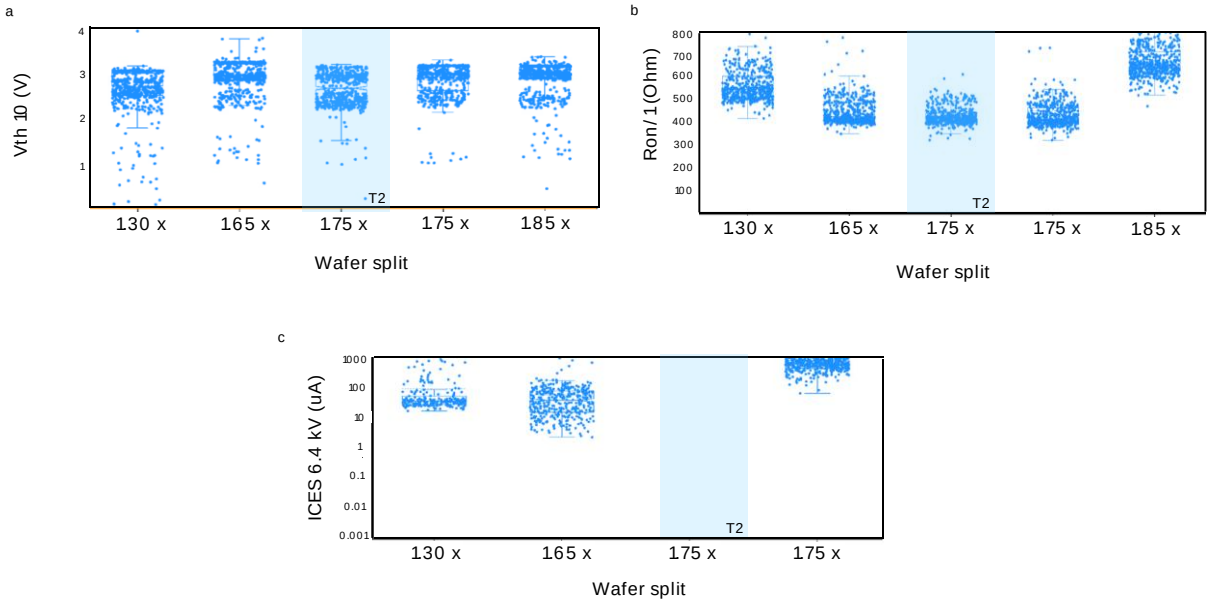


Figure: 17: Static wafers level characteristic at RT for 6.5kV MOSFET. JTE implantations were alternated for termination 1 T1 and termination 2 (T2). (a) V_{th}, (b) Ron/1, (c) ICES.

For the final lot the best performing conditions were chosen (Table 6). The lot was electrically characterized and the MOSFETs were used in the module assembly.

Table 6: Final split table of most optimized 6.5kV MOSFET lot

Split	Channel Profile	Channel length	Source	P plus rings	JTE
1	Profile 3	Channel length 2	Source 2	5	1.20x
2	Profile 3	Channel length 2	Source 2	5	1.30x
3	Profile 3	Channel length 2	Source 2	5	1.40x
4	Profile 3	Channel length 2	Source 2	4	1.50x

In the previous lot we found that channel length 2 in combination with channel profile 3 and five p+ rings are the optimal combination, for achieving low Rds,on and a high blocking value. In the final lot we therefore refined the JTE implantation dose to optimize further.

The V_{th} distribution is tight and very stable over the different JTE implantation multipliers. The V_{th} distribution is the lowest for the JTE 1.40x between 2.8V-3.0V, the V_{th} for the other JTE implantations is slightly higher between 2.8V-3.1V (Figure: 19a). The smallest Rds,on spread is found for the JTE multiplier 1.30x and 1.40x, whereas JTE 1.40x has the lowest Rds,on value for all splits ranging from 400 mOhm to 500 mOhm (Figure: 19b). The Rds,on value for JTE 1.3x is between 480-520 mOhm. For the highest JTE multiplier (1.5x) the Rds,on value is higher than 600 mOhm and for the twin wafer of JTE

1.3x a higher Rds,on value spread can be observed. The lowest leakage current at 6.5kV blocking voltage (Figure 19c) can be observed for the devices with JTE 1.5x of 10-100 uA indicating a strong blocking capability. The leakage at 6.5kV for JTE 1.3x and 1.4x is between 100-1 mA. The best dies were selected for the module assembly.

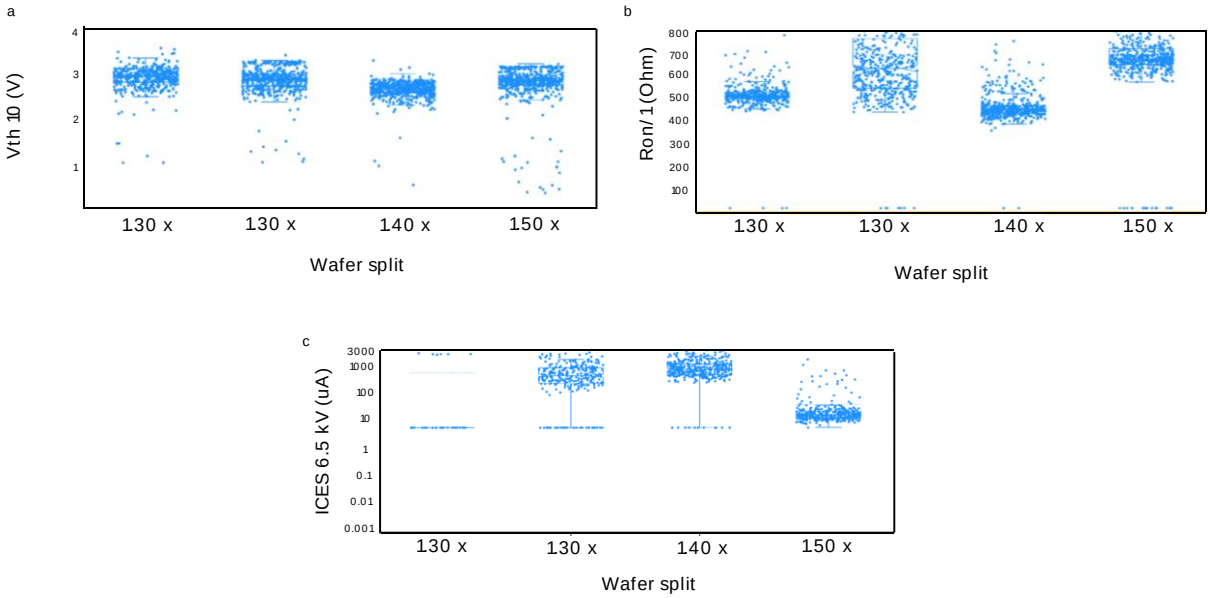


Figure: 18: Wafer level electrical characterization of the best 6.5kV splits. (a) V_{th} (b) Ron/1 (c) ICES.

2.3 Chip and packaging characterization

The on-state performance from the first 3.3kV SiC MOSFETs lots are shown in Figure: 29, for VGS=15V and T=25C. For comparison reasons, the IV curves for similarly rated SiC MOSFETs using SiO2 as gate dielectric are also shown. As can be seen, the use SiO2/SiN stack leads to an improvement of ~14% in Ron values, for same pitch size and active area (Figure: 20).

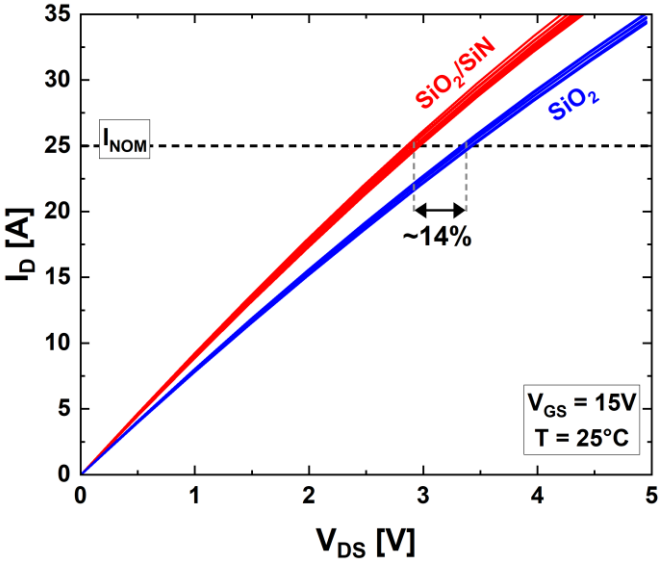


Figure: 19:Forward IV of 3.3kV SiC MOSFET using a SiO2/SiN as gate dielectric; for reference, IV curves for similarly rated SiC MOSFETs with SiO2 gate are also shown.

Once the wafer level static measurements mapping was finished, wafers have been diced, good chips have been picked up and sent for LinPak substrates assembly. Pictures of 1x MOSFET and 4x SiC MOSFETs bonded onto LinPak substrates are shown in Figure: 21.

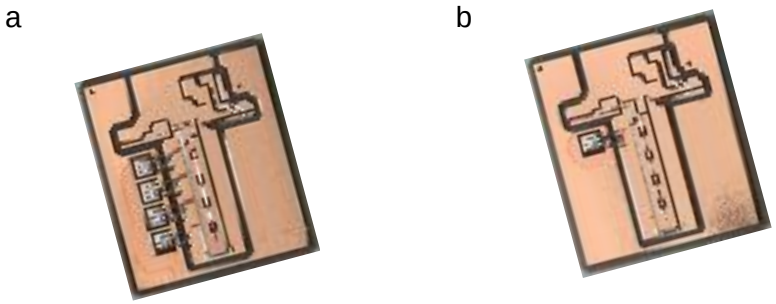


Figure: 20: (a) 1x MOSFET and (b) 4xSiC 3.3kV MOSFETs bonded onto LinPak substrates.

The substrates have been tested under nominal conditions, meaning $V_{nominal}$=1.8kV and $I_{nominal}$=25A/device. For all the tests the temperature has been set to T=150°C. The double–pulse tester had a fixed stray inductance of Lσ~90–100nH. For all the results reported here, a Si–like driving gate voltage of VGS=±15V was used.

The turn-on and turn-off waveforms for 1x MOSFET substrate are shown in Figure: 22. Three different external R_g values have been used. The expected influence of the gate resistor on the switching speed dV⁄dt can be clearly observed, demonstrating good control of the dV/dt values. The more pronounced oscillations observed on the current waveforms are not chip–related, they are a result of the experiments.

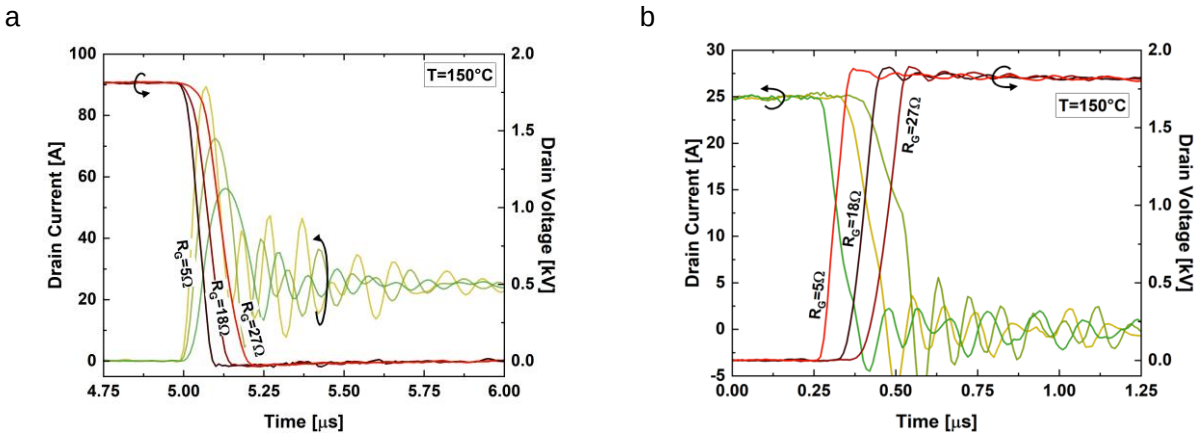


Figure: 21: (a) Turn-on (b) turn-off waveforms for substrates with 1x devices, at different RG values ($V_{Nominal}$=1.8kV, $I_{Nominal}$=25A/die, V_{GS}=±15V, T=150°C)

The turn-on and turn-off waveforms for 4x MOSFETs substrate are shown in Figure: 23, for 3 different external RG values. Here, the gate resistor and the stray inductance were not scaled for parallel devices, implying that the RG/chip and Lσ/chip are higher for the substrates with four MOSFETs. This is reflected in the larger overshoot for the drain voltage in Figure: 23(b) due to the higher parasitic inductance. Nevertheless, the substrates successfully passed the switching tests under nominal conditions.

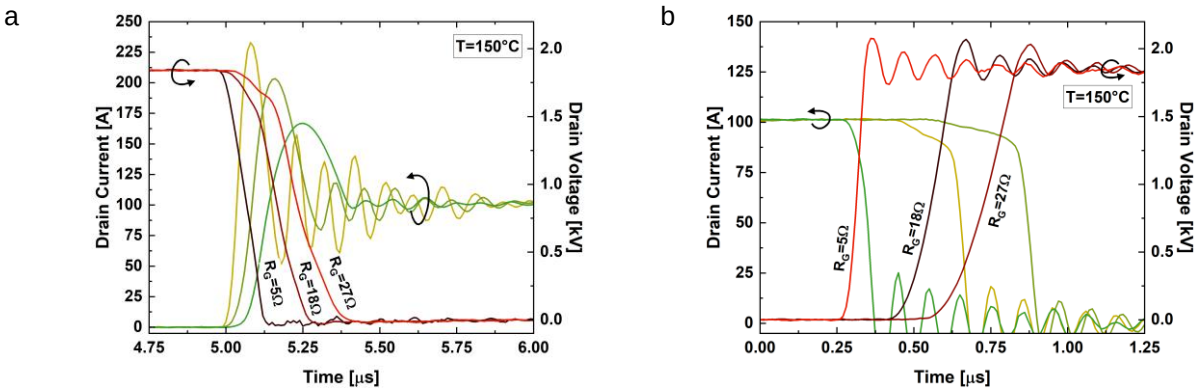


Figure: 22: Turn-on (a) and turn–off (b) waveforms for substrates with 4× devices, at different RG values ($V_{nominal}$=1.8kV, $I_{nominal}$=25A/die, V_{GS}=±15V, T=150°C)

The RBSOA capability of a 4x MOSFETs substrate is depicted in Figure: 24. Here, the turn-off waveforms are shown for DC link voltage of 2.6kV. The current load has gradually increased from 100A ($I_{nominal}$=25A/chip) to 200A, which corresponds to 2x$I_{nominal}$. It is worth mentioning that, even though both

voltage and current are beyond nominal values, the substrates with 4x parallel chips still show rather clean waveforms and acceptable voltage oscillations. This proves a reasonably well-balanced current sharing between devices, thanks to a substrate design engineered towards the minimization of parasitic components.

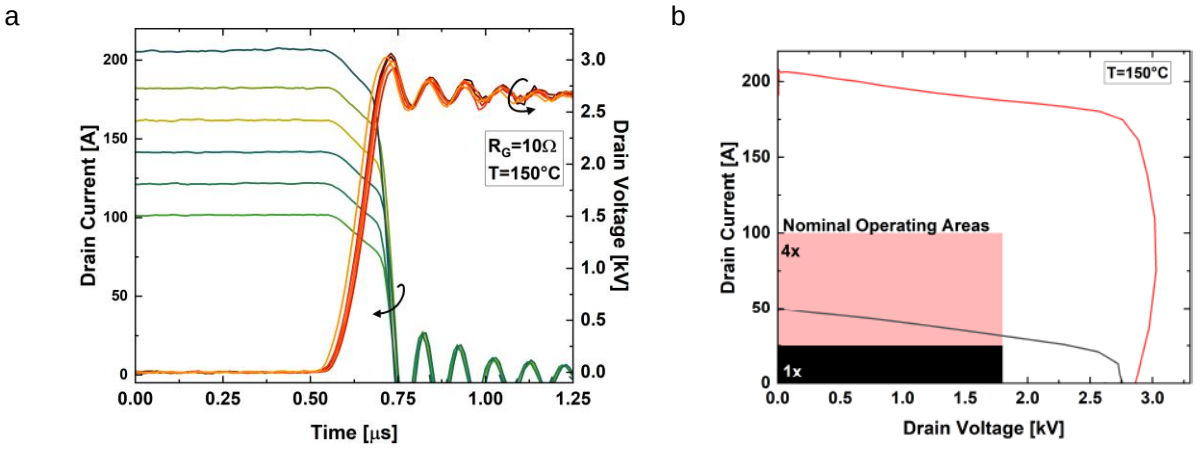


Figure: 23: Turn–off waveforms for substrates 4× devices (a), at different current values; RBSOA extracted from the switching I–V (b) (V_{SOA}=2.6kV, I_{SOA}=50A/die, V_{GS}=±15V, T=150°C)

For a more comprehensive investigation, the switching behavior of MOSFETs with the proposed SiO2/SiN structure has been compared to devices with same design but fabricated with our standard SiO2 gate dielectric. In Figure: 25, the total switching energy E_{ON} + E*OFF* per chip, calculated under nominal conditions ($V_{Nominal}$ = 1.8kV, $I_{Nominal}$ = 25A), is reported for different values of R_G. As could be expected, the SiO2/SiN–based devices exhibit marginally higher energy losses (this is due to the somewhat increased values of the input capacitance). Nevertheless, the increase in energy for the considered case is still moderately small (~12% max). If needed, as already demonstrated above, the energy losses could be adjusted using lower gate resistor values.

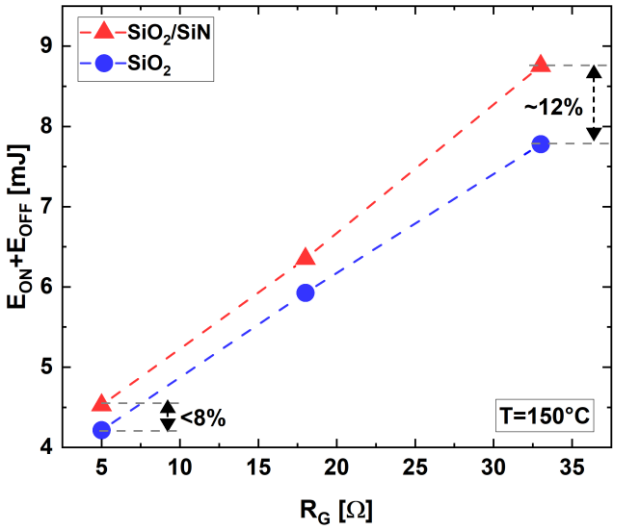


Figure: 24: Comparison of switching energy values for SiO_2 and SiO_2/SiN stack as gate dielectrics (V_N=1.8kV, I_N=25A, V_{GS}=±15V, T=150°C)

Working towards a fully operational SiC LinPak module (see Figure: 26), 10x SiC MOSFETs substrates have been assembled and dynamically tested.

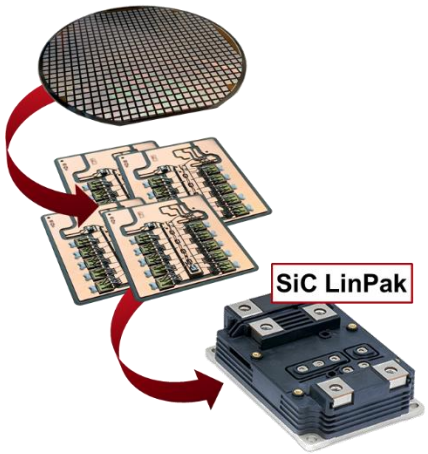
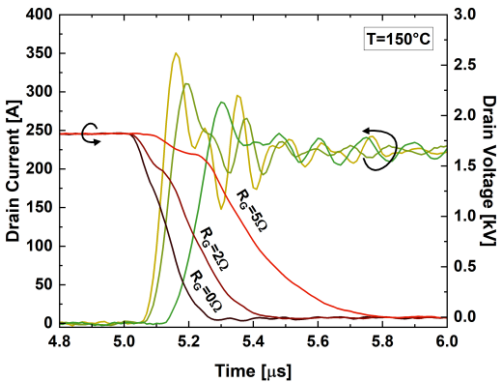


Figure: 25: SiC MOSFETs wafers towards LinPak substrates towards LinPak module chart.

Preliminary turn-on and turn-off waveforms, under nominal conditions, are shown in Figure: 27. While some current (turn-on) and voltage (turn-off) overshoots and oscillations are observed, it is important to mention that all substrates under test passed nominal conditions testing without failure.

a



b

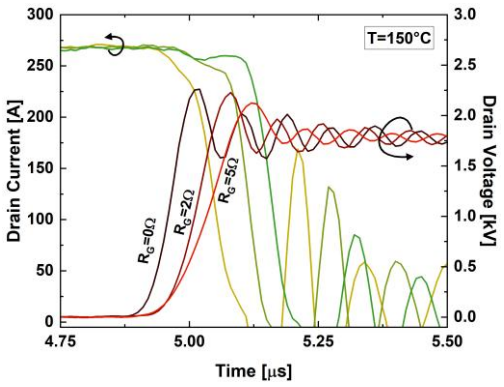


Figure: 26: Turn-on (a) and turn–off (b) waveforms for substrates with 10× devices, for different RG values ($V_{Nominal}$=1.8kV, $I_{Nominal}$=250A, V_{GS}=±15V, T=150°C).

As mentioned in section 2.1, the module demonstrator is developed in the LinPak platform. The packaging technologies in the current project are shown below (Figure: 26). The chip top-side connection is established by heavy Aluminum wire-bonding. Soldering is selected for chip-substrate connection. The selected substrates are with high-performance aluminum nitride and with thick copper on both sides ensure electrical conduction and thermal radiation. For connection between substrate and baseplate, soldering is used. Ultrasonic welding is used for the terminal connection to the substrate. Gel is used as encapsulation.

The same kind of analysis was performed for the 6.5kV MOSFET devices. In this case only single chip substrates as shown in Figure: 21a were assembled. The static and dynamic characterization was carried out for the single chip substrates to analyze the MOSFET performance also on substrate level. For this investigation we have selected devices that have higher and lower V_{th} values. Therefore, the V_{th} of our selection is at RT is between 1.93-3.81V and at high temperature between 1.43-3.78V and an Rds,on value at nominal conditions at RT is for the devices between 665-713 mOhm. The devices were found to be switched best at a V_{gs}=-5V. An external R_g of 10 Ohm was found best for the switching of the devices at a DC-Link of 3.8kV. The chip rating of the devices was found to be 7.5 A, lower than expected. As we are limited in the multi-chip assembly on substrate level by 10 dies, the final module rating was reduced to 150A. The multi-chip samples were switched with different external R_g= 1 Ohm and R_g=10Ohm. The turn-on of the module is depending on the applied R_g value. Faster turn-on can be achieved with low R_g, slower turn-on with the higher external R_g. Using a higher external R_g is therefore recommended to reduce the oscillations of the substrates.

2.3.1. Electro-magnetic design of the SiC LinPak

In the scope of this project, a High Voltage (HV) Silicon Carbide (SiC) LinPak module was developed. Due to strategic reasons, the housing block for this new module is chosen to be the same as the HV Si LinPak module under development. This fact is defining critical things such as terminal position and size

for main and auxiliary potentials. As a result, the design optimization phase was limited to substrate design, including chip and wire bond layout optimization.

One of the critical aspects of a power semiconductor module is the electromagnetic (EM) behavior. A good EM behavior will help towards current balance, resulting in lower thermal losses and improved reliability. Along the design optimization phase, each proposed iteration was verified electromagnetically by the means of EM simulations using ANSYS Q3D package. Figure: 28 shows the coupling inductance ranges for both High Side (HS), in blue and Low Side (LS), in green, switches. The red rhomb represents the average value. The optimization goal is to obtain a design which provides a small range, similar average values for HS and LS, and slightly negative (between -0.2 and -1 nH).

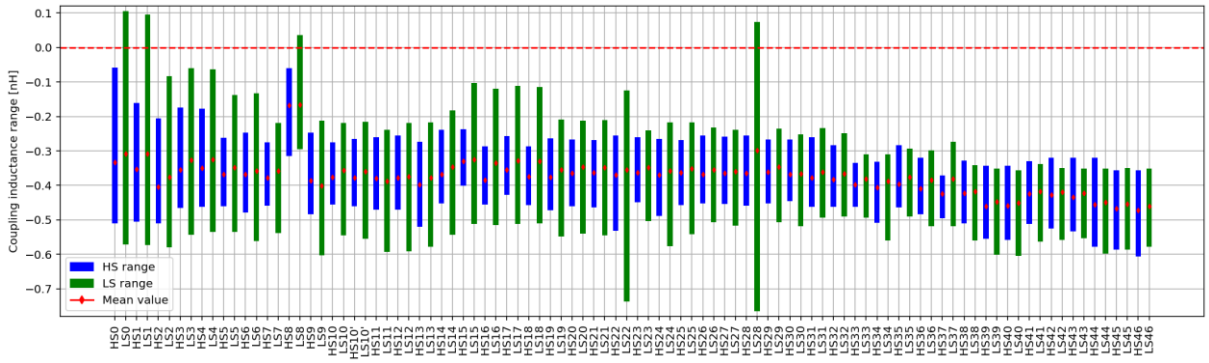


Figure: 27: Coupling inductance ranges of different design iterations for HV SiC LinPak module.

All design iterations were built on fully populated substrates, i.e. 20 SiC devices per substrate. It was observed that half populated substrates, i.e. 10 SiC devices per substrate, presented similar EM behavior.

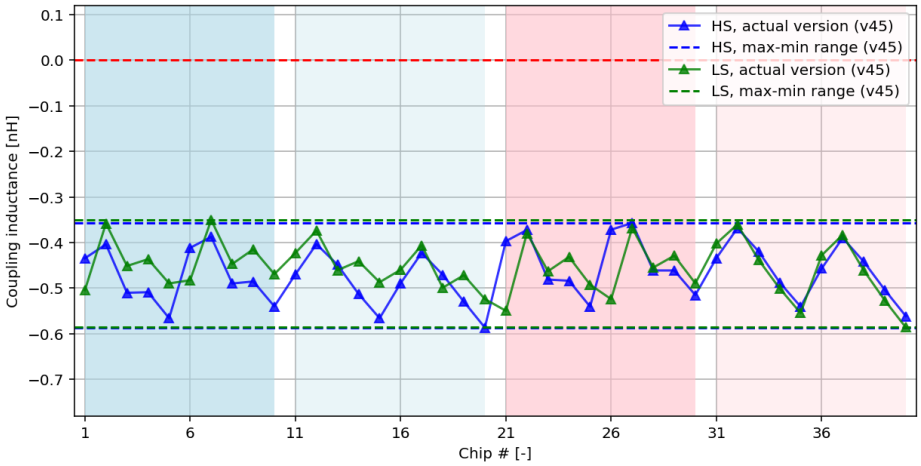


Figure: 28: Coupling inductance values of v45, for HS (blue) and LS (green) switches, per chip.

The best compromise between thermal and EM results was achieved in v45. The resulting EM behavior can be observed in Figure: 29. Note that the x axis represents the chip number, per switch (i.e. two fully populated substrates correspond to a total of 40 chips per switch) Additionally, the simulated stray inductance was 29.7 nH, meeting the target specification of <30 nH.

These EM results compare well from coupling inductance range to other LinPak modules in the product portfolio, as shown in Figure 30 and Figure 31 below.

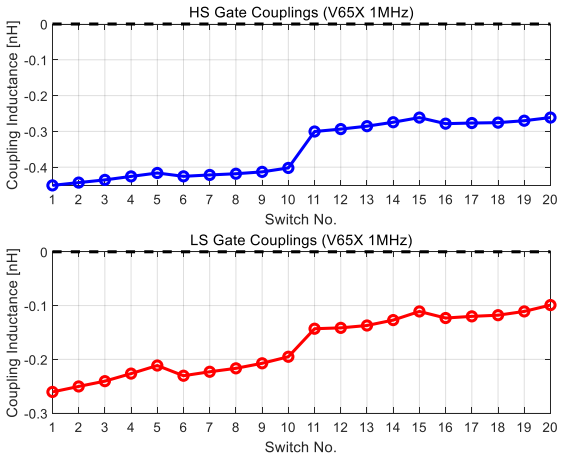


Figure: 29: Coupling inductance values for LV SiC LinPak for 20 chips per side configuration.

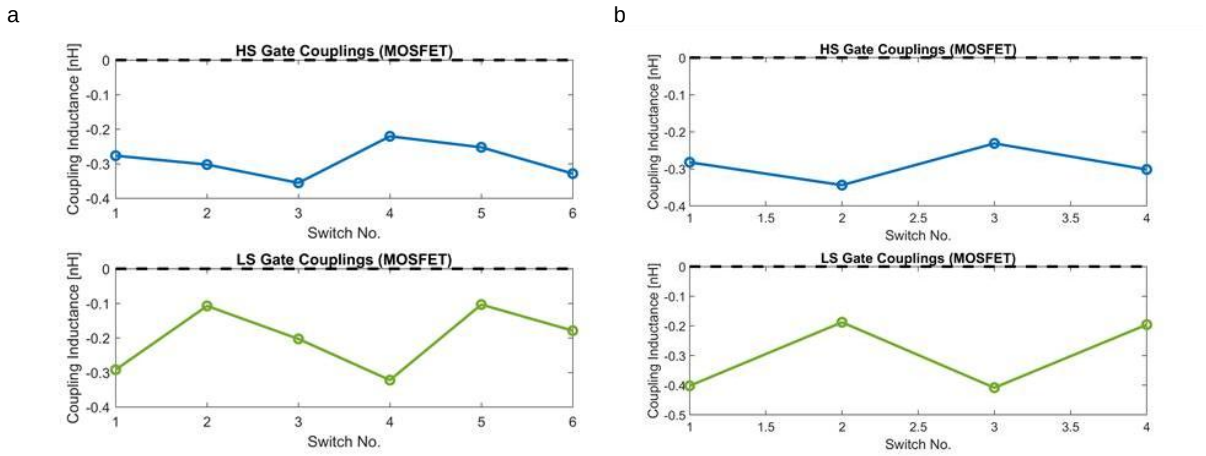


Figure: 30: Coupling inductance values for HV Si LinPak, for 3 IGBT+ 2 diode configuration (a) and 2 IGBT + 2 diode configurations (b).

2.3.2.Selection of joining technologies for the SiC Devices in the module

As mentioned in section 2.1, the module demonstrator is developed in the LinPak platform. The packaging technologies in the current project is shown in below (Figure: 32). The chip top-side connection is established by heavy Aluminum wire-bonding. Chip soldering is selected for chip-substrate connection. The selected substrates are with high-performance aluminum nitride and with thick copper on both sides ensure electrical conduction and thermal radiation. For connection between substrate and baseplate, soldering is used. Ultrasonic welding is used for the terminal connection to the substrate. Gel is used as encapsulation.

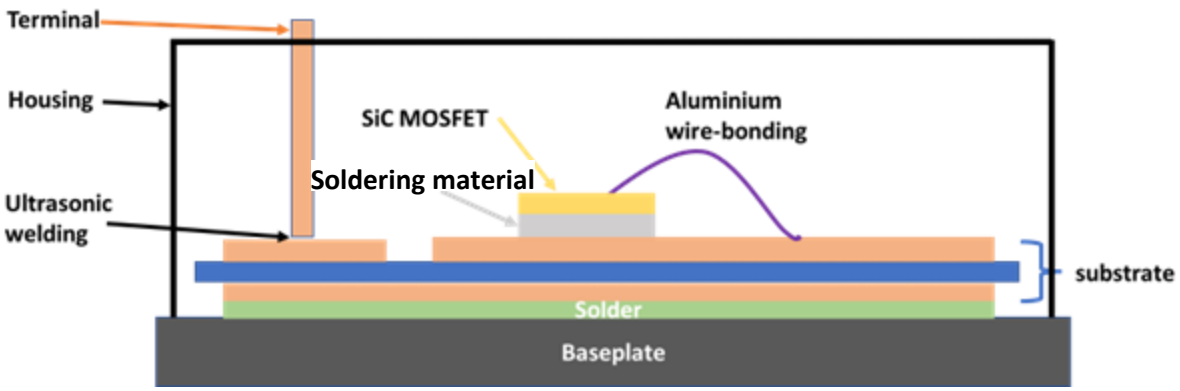


Figure: 31: Schematic cross-section of the LinPak demonstrator. The dimensions are not to scale.

Most technologies take the synergy with on-development high-voltage Si-based LinPak product platform. Silver sintering vs soldering for chip-substrate connection is explored in the project and the reliability will be tested during power cycling. Compared to Si devices, SiC-based devices have much smaller

size while having the same power ratings, thus having much higher power density. Their intrinsic material advantages also bring the junction temperature much higher than that of Si devices. We will investigate the die-attach methods soldering vs sintering. Both materials have their advantages and disadvantages.

High-temperature solder materials have as a melting point around 300 °C (573.15 K). The rating temperatures of many SiC MOSFETs have reached 175 °C (448.15 K), so solder's homologous temperature easily goes beyond 0.75. Such high homologous temperature can bring the material into exponentially higher creep deformation and therefore limited lifetime.

Silver sintering has its melting point similar as pure silver (969 °C /1242.15 K) means 0.36 as homologous temperature at 175 °C operation, in such region the temperature-related creep is far less critical. Moreover, the thermal conductivity of silver sintering is much better, ranging from 120 W/mK to 330W/mK, depending on the porosity and filler. Die-attach solder materials used in standard LinPak have thermal conductivity in the range of 60 W/mK. Figure: 33 shows the silver sintering joint established in Hitachi Energy Semiconductors.

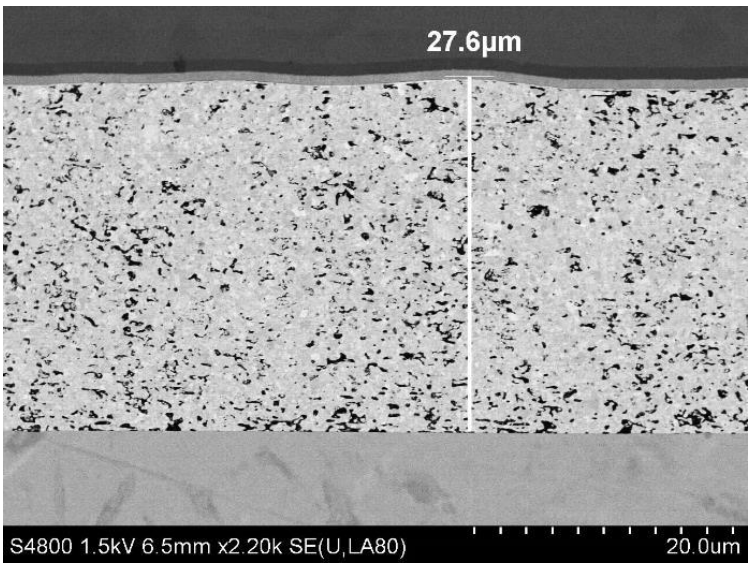


Figure: 32: Silver sintering joint. From top to bottom: chip, silver sintering (27.6 µm), substrate.

During the development, scanning acoustic microscope is used as the main method to characterize the interconnections. With the reflection mode, black contrast indicates good interconnections where the sound signal transmits fully without reflection. Light contrast means reflection of the sound signals, indicating voids or delamination. Here shows SAM images of the interconnection of the different layers (Figure 34).

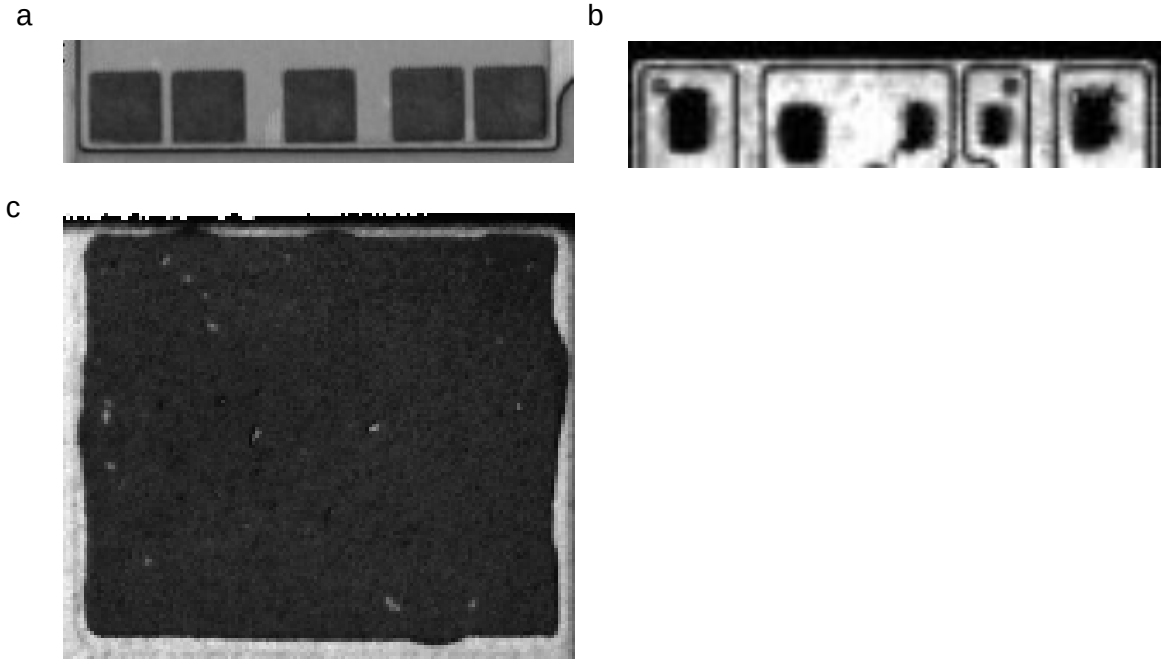


Figure: 33: SAM image of (a) sintered chip-substrate attachment, interconnections of 5 chips are shown; (b) ultrasonic welded terminal connection, interconnections of 5 terminal feet are shown; (c) soldered substrate-baseplate connection, 1 substrate is shown.

As shown in the SAM images, the established connections are good quality which have good contact area and contrast. In the later stage of development, the processes will be further investigated via fine characterization and possibly reliability tests. Based on the characterization results and reliability failure modes, process optimization and improvement can be done.

For Wire-bonding connections, the criteria are high mechanical strength however no damage especially on chips. Current prototype wire-bonding focuses on achieving low gate-source rate; therefore, a relatively soft wire-bonding process is used. Future development on improving the mechanical strength can be done. The silver sintering of the dies was only explored on an experimental level for the reliability evaluation of the modules, the LinPak assembly was done with the established soldering process.

A general process flow can be seen in Figure: 34 below.

Figure: 34: Process flow of module assembly.

2.4 Module static & dynamic characterization

2.4.1.3.3kV Si and SiC modules characterization

We assembled the 450 A Si and SiC 3.3kV modules from the best performing dies produced in the front-end. The chips were binned and picked according to the Rds,on and V_{th} values.

The 3.3kV SiC modules were tested static and dynamic at RT and 150°C to evaluate their performance. The V_{th} was measured using the constant current method with Id= 200 mA. The hysteresis of the V_{th} was investigated after pre-biasing the gate to Vgs=-5V and Vgs=15V. It was slightly lower for the high side (HS) than for the low side (LS) (HS=1.7V, LS 1.75-1.8V, after gate bias of Vgs=-5V) and at Vgs=15V (HS=1.8V and LS=1.8V-2.0V). The V_{th} value for the modules at 150°C is between 1.6V-2.0V (Figure: 36). The Rds,on value was measured for HS and LS for the different modules. There was a slightly difference in Rds,on between HS and LS, but for all modules the Rds,on was between 15-16 mOhm.

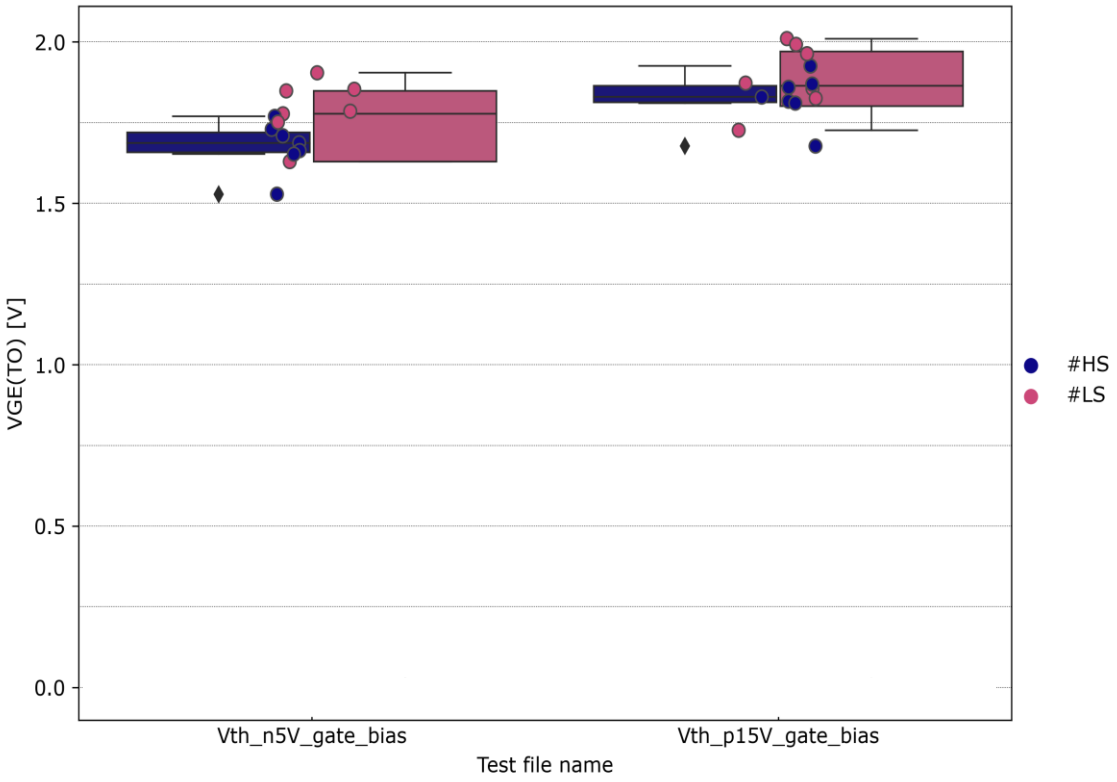


Figure: 35: Static (a) V_{th} evaluation of the 3.3kV SiC modules using the constant current method and pre-biasing the gate to V_{gs}=-5V and V_{gs}=15V

The drain leakage current was tested by applying a drain to source voltage of 2.2kV. The drain leakage current was below 0.5 mA for 2.2kV blocking voltage (Figure: 37 a, b). When measuring the drain leakage current, it is possible that the current initially overshoots way above the static leakage current. This behavior is due to the combined behavior of the voltage source and the capacitive behavior of the semiconductor. To obtain the correct measurement, the result is the average of the measurements within a time frame of the overall test time, which is after the initial transient of the current has settled.

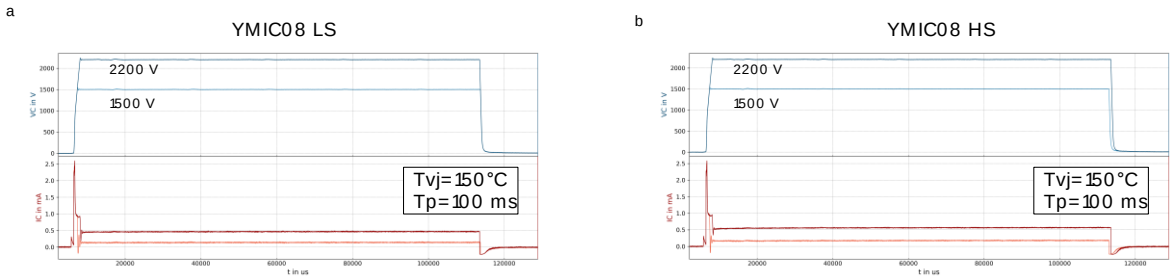


Figure: 36: Example for leakage current test of the SiC 3.3kV module (a) for the LS at 150°C (b) and the HS at 150°C.

Figure 38 displays the dynamic switching of a 500A SiC 3.3kV module for turn-on, turn-off and diode turn-on comparing the HS with the LS at 150°C at DC-link 1.8kV at nominal condition (R_g=2 Ohm, L_σ =ca 120 nH and Tv_j= 150°C). The HS for the turn-on indicated a faster voltage rise and a sharper current onset, indicating a quicker turn-on. The LS is displaying slightly delayed switching, possible due to parasitic inductance or gate drive differences. For both HS and LS, initial current spikes are followed by stabilization and a difference in switching speed is observed.

For the turn-off we observe that the HS shows a steeper drop in the current, suggesting a faster turn-off than the LS where we observe a more gradual behavior. For the reverse recovery of the diode the HS shows higher reverse recovery current indicating higher losses, the LS diode has faster recovery with reduced switching losses.

No overvoltage could be observed but slightly higher oscillations could be observed on the high side of the modules. At nominal condition DC-link 1.8kV 500A (Rg=2 Ohm, L_σ =ca 120 nH and Tv_j= 150°C) the losses are E_{off}=90-100 mJ, E_{on}= 75-190 mJ and E_{rec}= 21-27 mJ.

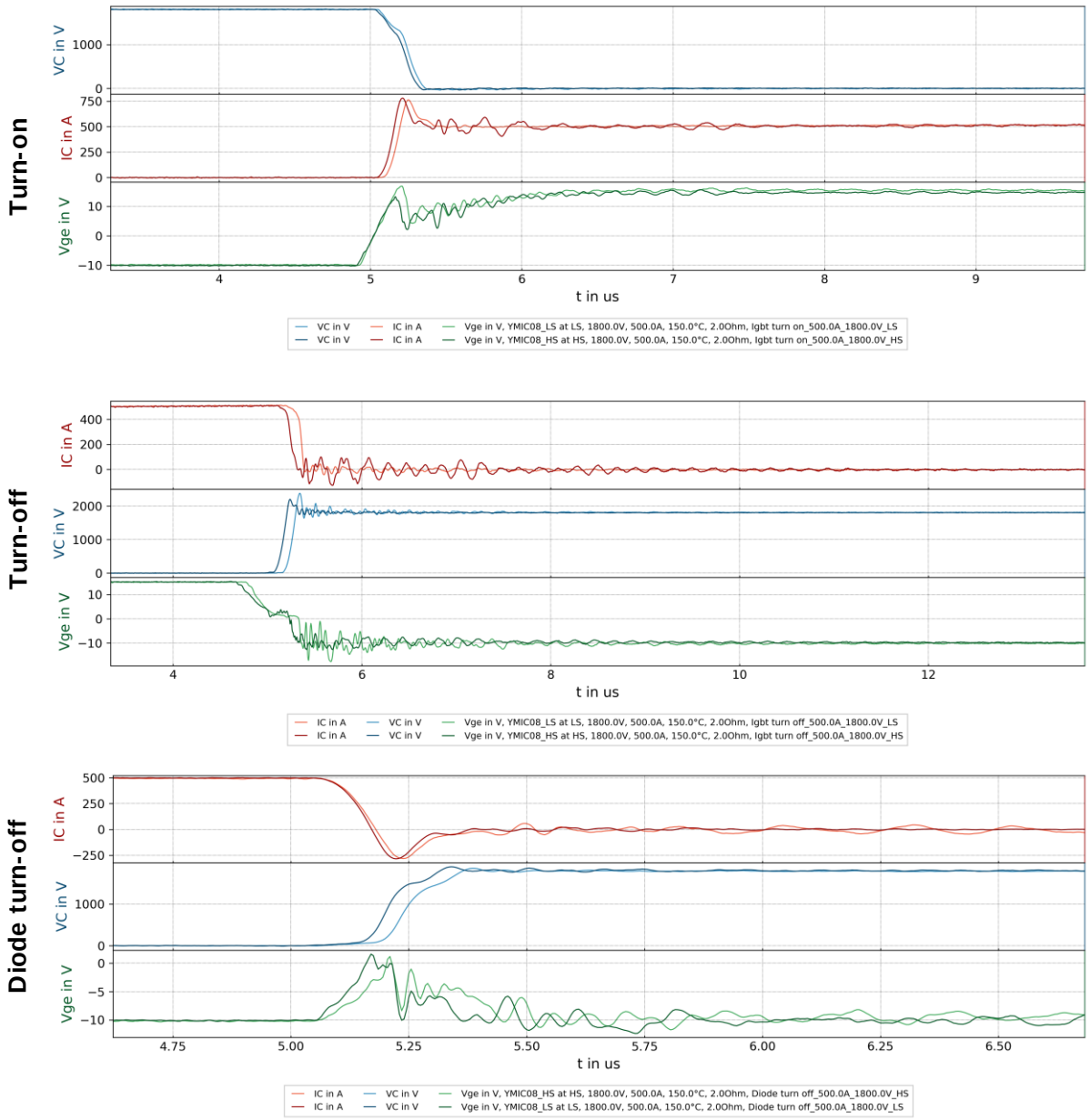


Figure: 37: Example for 500A 3.3kV SiC module turn-on, turn-off and diode turn-off during dynamic switching. DC-link 1.8kV, 500A, R_g=2 Ohm, L_σ =ca 120 nH and Tv_j= 150°C.

The 450A Si modules were also analyzed statically and dynamically and the results were compared with the SiC results. Figure: 39 a is showing the results for the V_{th} at 150°C. For the Si module V_{th}= 4.4V, which is much higher in comparison to the SiC module (SiC V_{th}=1.8V). The Rds,on values for the modules at V_{gs}= 15V and 150°C. The Rds,on value is symmetric for high side and LS of the module, demonstrating a good balancing. At 450 A the Rds,on is approximately 5 mOhm for the Si module and at 550A 15 mOhm for the SiC module.

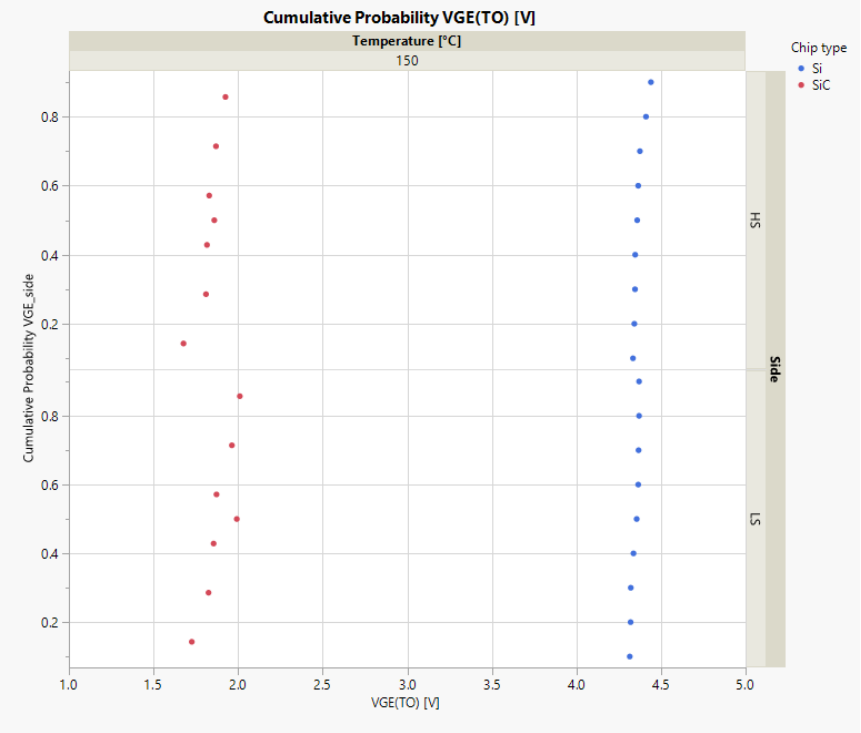


Figure: 38: (a) V_{th} probability plot Si vs SiC for high side and low side

The drain leakage current of the Si modules was measured for the different blocking voltages BV= 1.0kV, 2.0kV, 3.0kV and 3.3kV (Figure: 40). A linear increase for the leakage current can be observed for the modules. The drain leakage current is ICES=7.5 mA at 1kV, ICES= 10 mA at 2kV, ICES=12 mA at 3kV and ICES=12.5mA at 3.3kV. The drain leakage current for the SiC modules was measured at 1.5kV and 1.8kV and is substantially lower than for the Si modules.

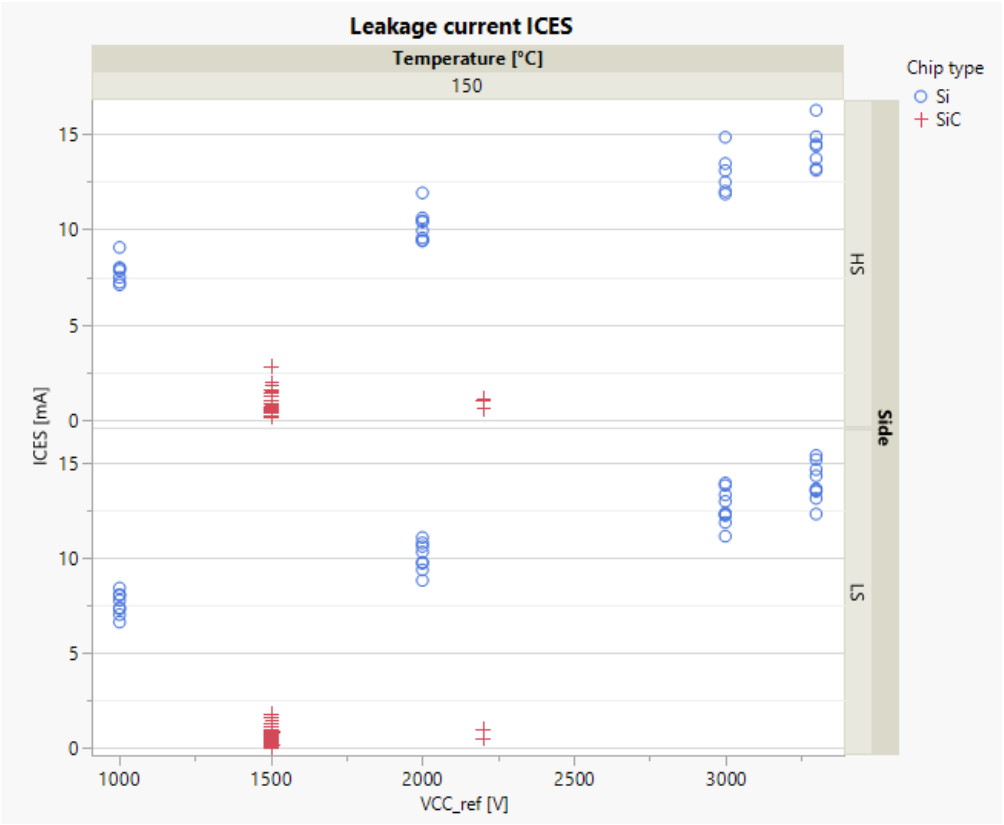


Figure: 39: Drain leakage current ICES for different voltages at 150°C, Si vs SiC modules.

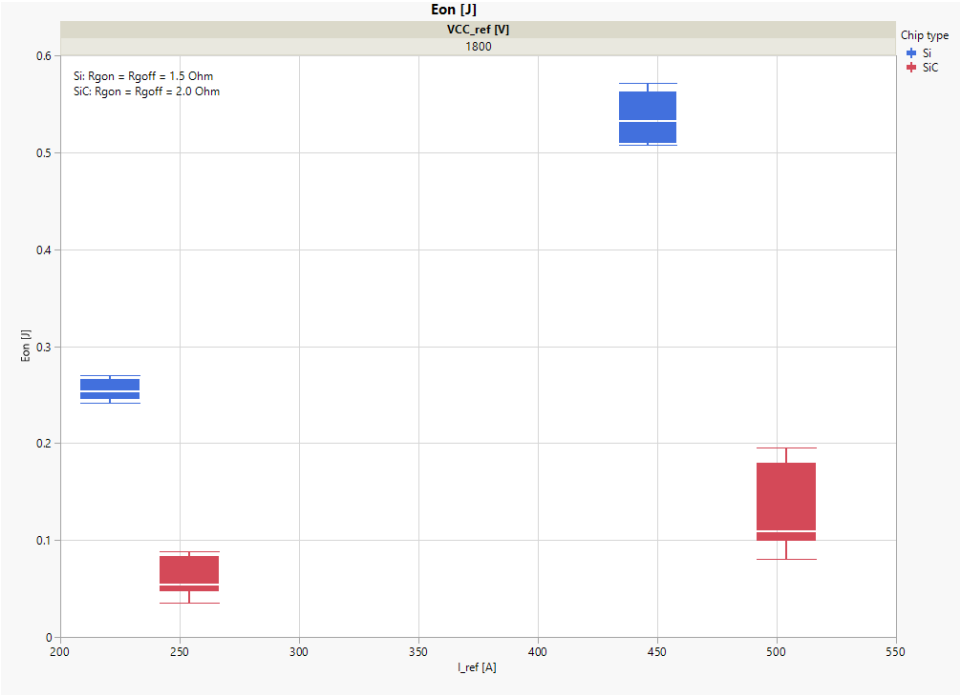


Figure: 40: Switching turn on losses E_{on} for Si and SiC modules. For the Si modules the external R_{gon}= 1.5 Ohm and for SiC R_{gonf}=2.0 Ohm.

Figure 41 describes the turn-on losses of the Si vs SiC module. The SiC module losses for the turn-on are in general lower than for the Si modules. The E_{on} for Si modules (Rgon=1.5 Ohm) at 225 A is 250 mJ and at 450A is 550 mJ and for SiC, Eon is 50 mJ at (Rgon=2.0 Ohm) 250A and 150 mJ at 500A. In Figure 42 the turn-off losses are described. For SiC they are lower than for Si.

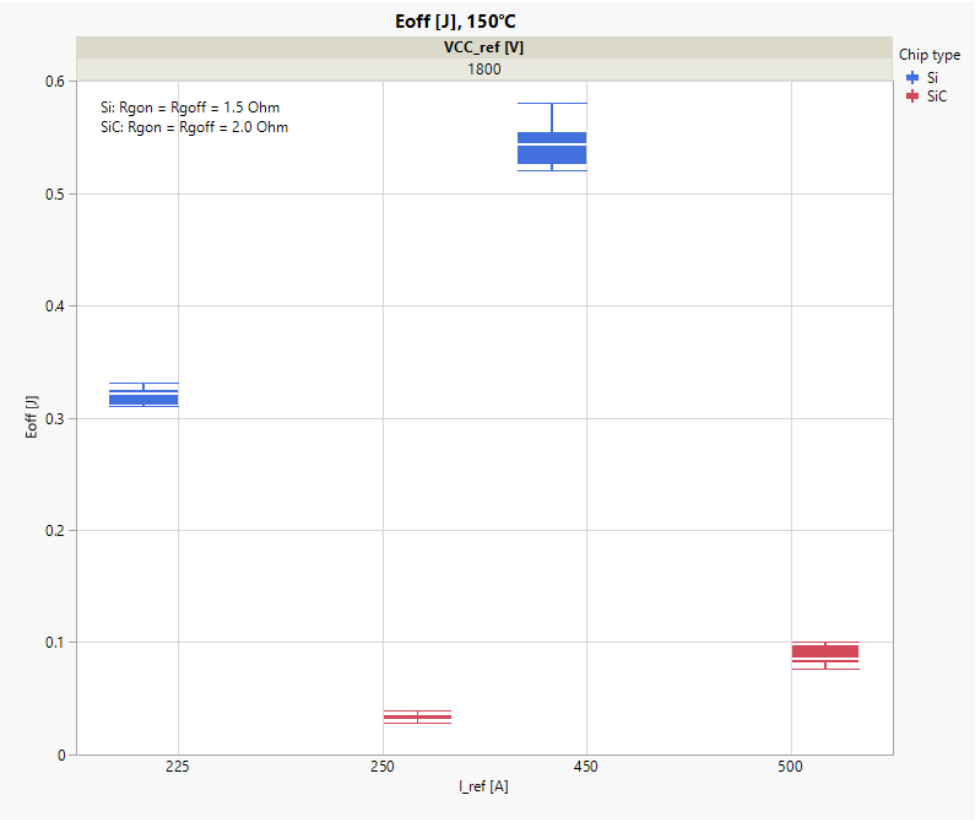


Figure: 41: Switching turn off losses E_{off} for Si and SiC modules. For the Si modules the external Rg_{off}= 1.5 Ohm and for SiC Rg_{off}=2.0 Ohm.

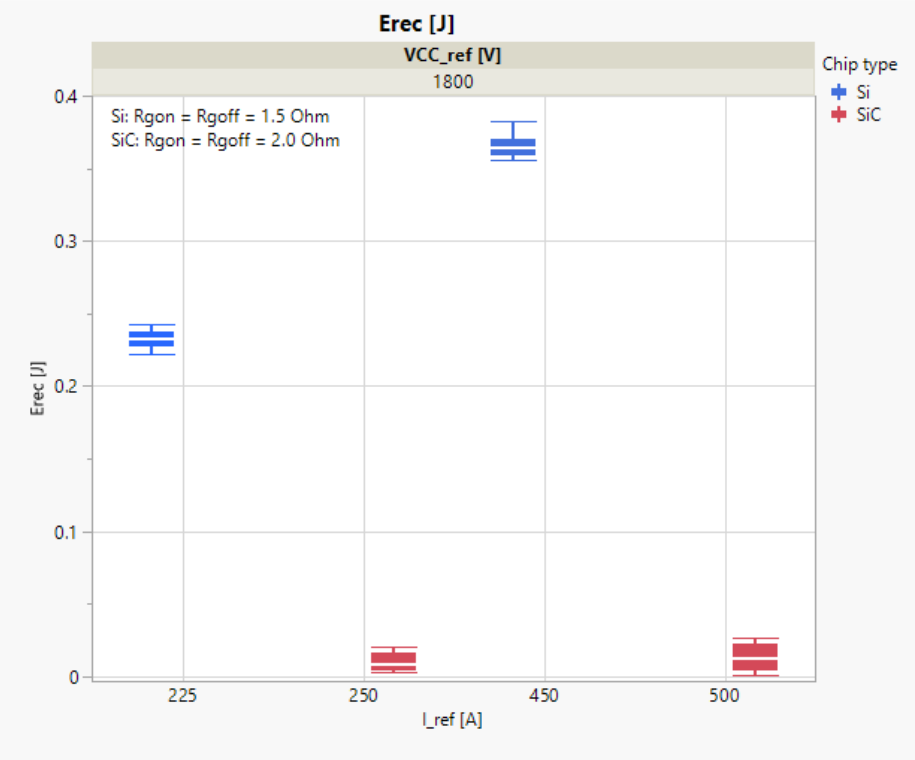


Figure: 42: Switching diode turn-off losses of the diode E_{rec} for Si and SiC modules. For the Si modules the external Rg_{on}= 1.5 Ohm and for SiC Rg_{on}=2.0 Ohm.

Figure 43 describes the diode turn-off of the 3.3kV Si vs SiC module. The losses are one magnitude lower for the SiC modules than for the Si modules. The SiC diode demonstrates significant lower switching losses, making it more suitable for high-speed and high-efficiency applications. Faster turn-off, turn-on, and diode turn-off are typical advantages of the SiC technology.

2.4.2.6.5kV Module data Si and SiC

The 6.5kV 150A Si and SiC modules were assembled in our production line according to the assembly flow shown in Figure: 35. The chips were binned and picked according to the Rds,on and V_{th} values.

The modules were first analyzed statically. The drain leakage current analysis (Figure: 44) was measured at V_{gs}=0V, V_{ds}= 4.2kV, t_{on}=100 ms and T_{vj}=150°C. The drain leakage current is higher for the Si modules vs the SiC modules (0.4 mA vs 6 mA).

The SiC modules have a V_{th} of 1.71V and the Si modules of 5.27V. The Rds,on value of the SiC modules is twice as high as the Si modules (50 mOhm vs 28 mOhm) (Table 1).

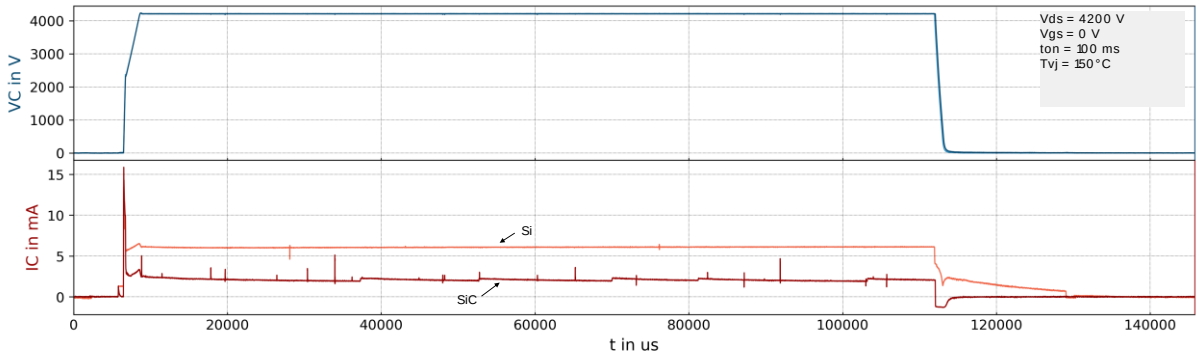


Figure: 43: Static characterization of leakage current during blocking test comparing Si vs SiC modules

Table 7: Summary table with the static characterization of the 150 A Si and SiC 6.5kV modules comparing the most relevant parameters

Module		Threshold Voltage [V]	Onstate voltage Rds,on at V_{gs}=15V I_{ds} = [mOhm] 150 A [V]		Drain Leakage current I_{ds} [mA]	
					3800 V	4200 V
SiC 01	LS	1.635	7.756	51.36	0.1006	0.1584
	HS	1.611	8.487	56.21	0.2568	0.4895
SiC 02	LS	1.665	7.019	46.48	0.1425	0.206
	HS	1.483	7.135	47.25	0.1247	0.1377
Si 01	LS	5.193	4.220	27.95	5.801	6.003
	HS	5.289	4.312	28.56	5.896	6.215
Si 02	LS	5.286	4.307	28.52	5.877	6.137
	HS	5.193	4.220	27.95	5.801	6.003
Si 03	LS	5.308	4.293	28.43	5.669	5.962
	HS	5.288	4.298	28.46	5.982	6.245
Si 04	LS	5.304	4.100	27.15	3.795	4.014
	HS	5.262	4.172	27.63	4.784	5.003

The modules were characterized dynamic at R_g=2 Ohm, L_σ= ca. 120 nH, V_{cc}=3.8kV, Inom=150A and Tvj=150°C. The SiC modules are switching faster than the Si modules with the same gate resistor. The switching losses are lower for the SiC modules in comparison to the Si modules (Table 7). The turn-on losses for the SiC modules are max 240 mJ and for Si are 900 mJ. The turn-off losses are for SiC 95 mJ and for Si 911 mJ and the diode turn-off losses are for SiC 130 mJ and for Si 700 mJ.

Figure 45 describes the turn-on and turn-off behavior of the Si vs SiC module. For the turn-on behavior (Figure 45a), the SiC device shows a faster rise in the collector current (IC) and a sharper drop in the

collector emitter voltage (V_{CE}) compared to the Si device. The gate emitter voltage (V_{GE}) increases similar for both, but the SiC device responds more quickly in terms of switching. In the turn-off behavior the SiC device demonstrates faster switching with a quicker drop in I_C and a more abrupt rise in V_{CE}. The Si device shows a more gradual transition, indicating slower switching performance (Figure: 45b).

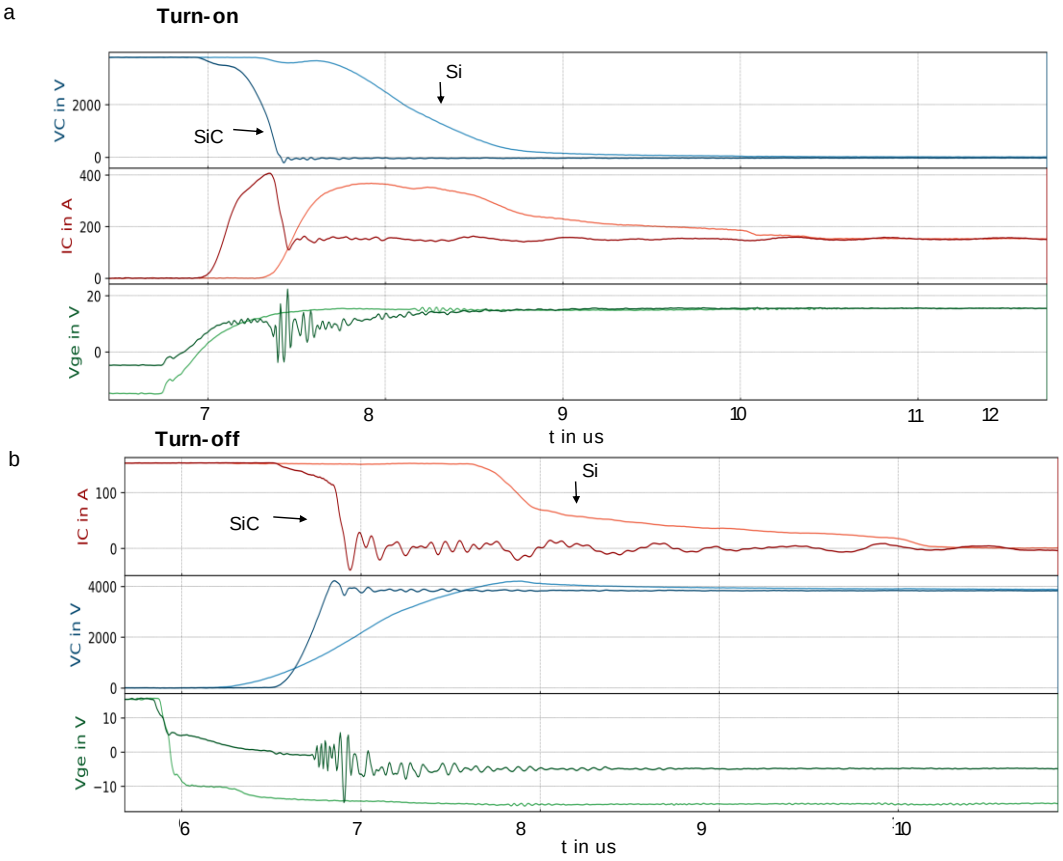


Figure: 44: Turn-on and turn-off switching waveforms of the 150A 6.5kV Si vs SiC modules at DC-link 3.8kV, 150A, R_g=2 Ohm, L_σ =ca 120 nH and Tv_j= 150°C.

Figure 46 describes the diode turn-off of the 6.5kV Si module vs the SiC module. The SiC diode exhibits a rapid drop in current at approximately -200A around 6.8 us and shows strong oscillations immediately after the drop, which then stabilizes near 0A at 8 us indicating a fast-switching response. The Si module displays a more gradual decrease in current, and oscillations are less pronounced. It stabilizes at 0A around 9us, indicating a slower switching response. The voltage curve (VC) rises sharply to around 4000A at 7 us for both diodes. After the initial spike, it remains stable with minor fluctuations up to 12 us. This suggests that the voltage stress during diode turn-off is similar for both diode types, but the current dynamics differ significantly. The SiC diode demonstrates significant superior switching performance, making it more suitable for high-speed and high-efficiency applications. The faster turn-off and sharper current transition are typical advantages of SiC technology.

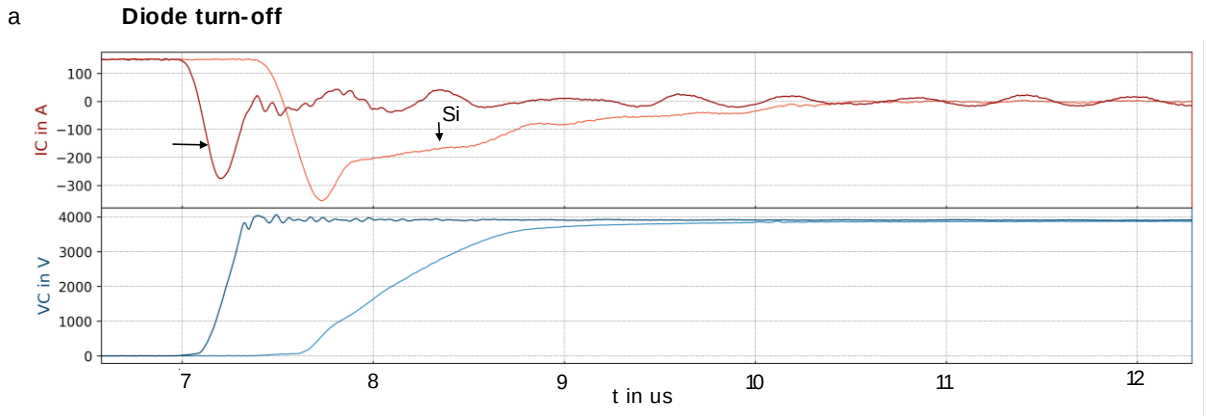


Figure: 45: Diode turn-off switching waveforms of the 150A 6.5kV Si vs SiC modules at at DC-link 3.8kV, 150A, R_g=2 Ohm, L_σ =ca 120 nH and Tv_j= 150°C.

Table 8: Dynamic characterization parameters comparing 6.5kV Si vs SiC modules.

Module		Turn-on losses[mJ]	Turn-off losses [mJ]	Diode turn-off losses[mJ]
		3800 V	3800 V	3800 V
		150 A	150 A	150 A
SiC 01	LS	239.4	94.9	67.5
	HS	171.6	92	129
SiC 02	LS	180.1	85.9	58.5
	HS	141.2	81.3	90.5
Si 03	LS	927.0	909.9	724.5
	HS	857.4	869.7	696.4
Si 04	LS	906.7	963.1	732.1
	HS	849.5	911.4	699.5

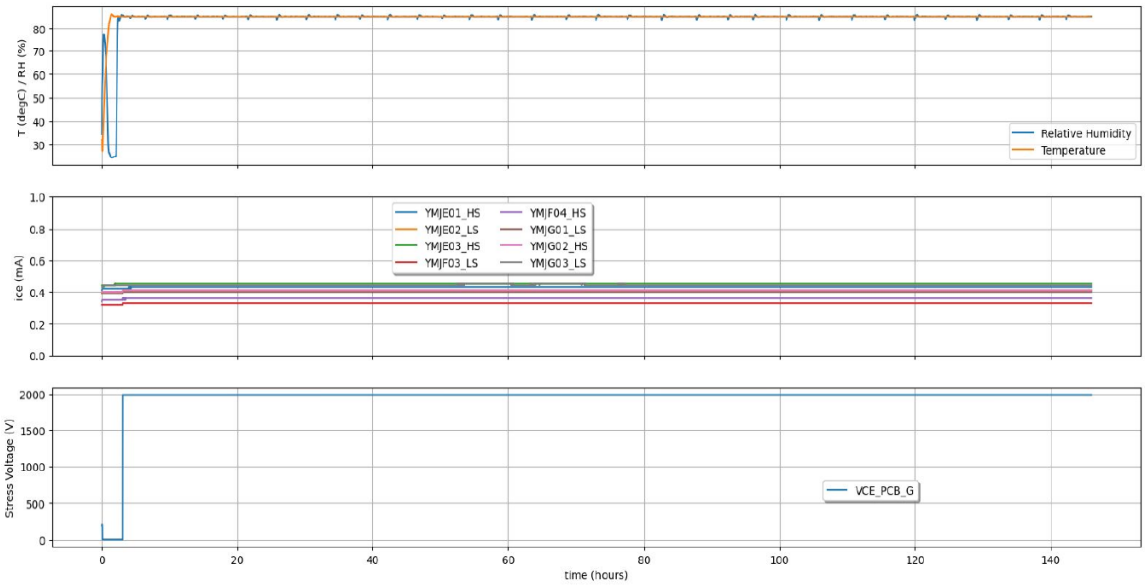
3 3.3kV und 6.5kV SiC MOSFET module reliability

3.1 HV-H_3TRB test of Si and SiC modules

The HV LinPak modules prepared during this project were also tested for their reliability in H_3TRB tests.

We first tested the 3.3kV Si LinPaks at 85% humidity, 85°C and 60% V_{ds}. The Si modules were stressed at V_{gs}=0V. Figure: 47 displays the results of the H3TRB test of the 3.3 kV Si LinPaks test. Alle modules passed the 1000h testing. After 140h the test had to be restarted, therefore two graphs are displayed in Figure: 34. The restarting of the test did not do any harm to the modules. The blocking curves and the V_{th} was recorded of the 3.3kV Si LinPak modules before and after the testing (Figure: 48). All modules

stressed and none-stressed sides do not show any drift before and after the HV-H_3TRB test. The modules were not harmed during humidity testing.



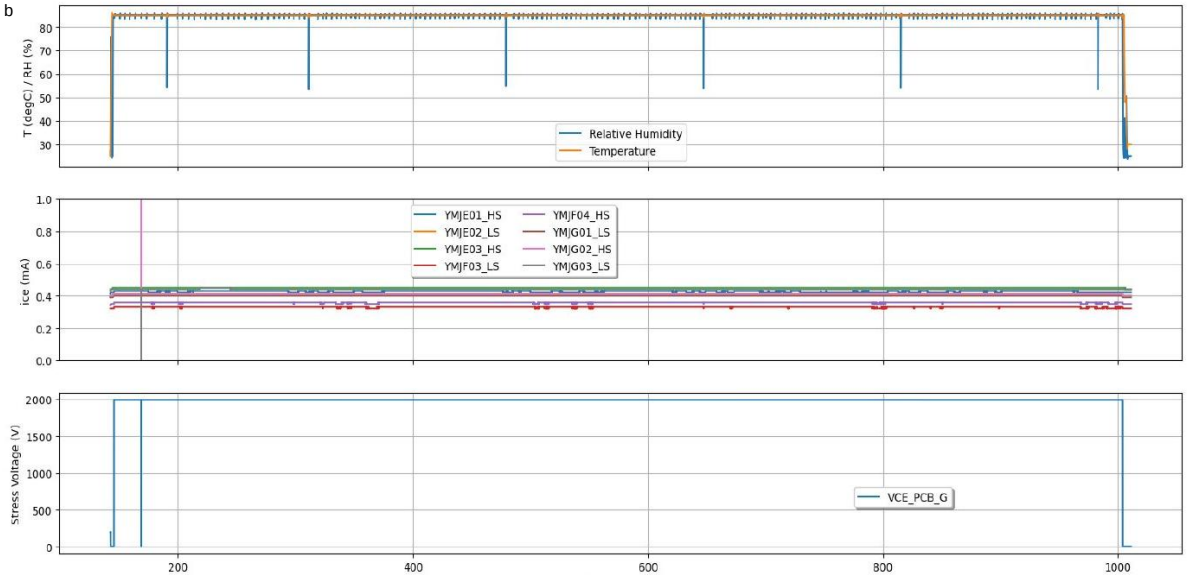


Figure: 46: H_3TRB of the 3.3kV Si LinPak. Ambient temperature, relative humidity monitors over time are shown in the first (top) plot. Collector emitter leakage currents over time for all modules (mid-plot). Applied V_{CE} voltage (bottom plot). For the full test the I_{CE} was within system noise level.

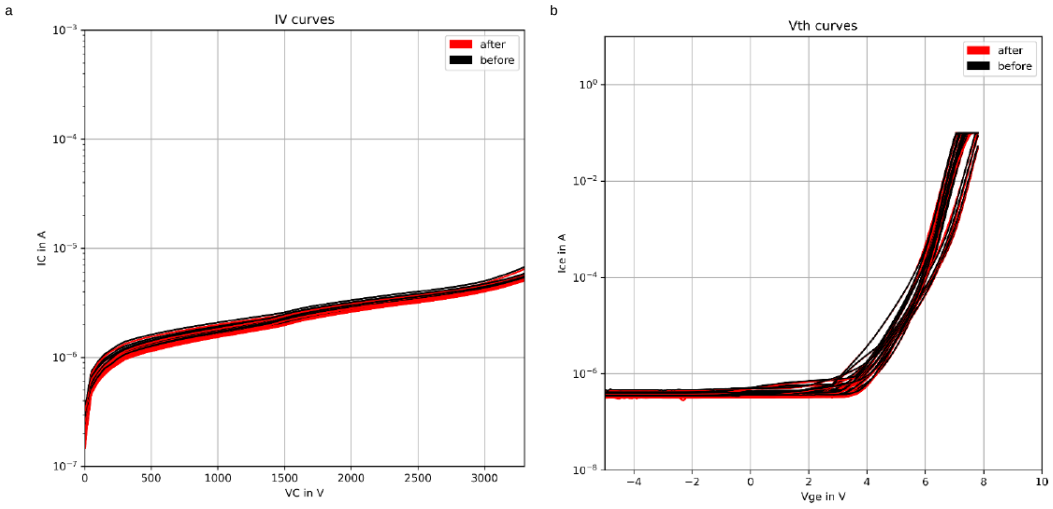


Figure: 47: Electrical characterization of the modules before and after the H_3TRB testing. a) Blocking curve comparison. b) V_{th} curve for all H_3TRB modules including references.

Figure 49 displays the H_3TRB testing of the 3.3kV SiC modules. The Hitachi Energy internal chip modules were stressed at V_{gs}=-5V and the external chip modules were stressed at V_{gs}=0V. All the modules have an I_{CE} within the noise level of the system (ca. 500 uA). All 3.3kV modules passed more than 800h in testing successfully.

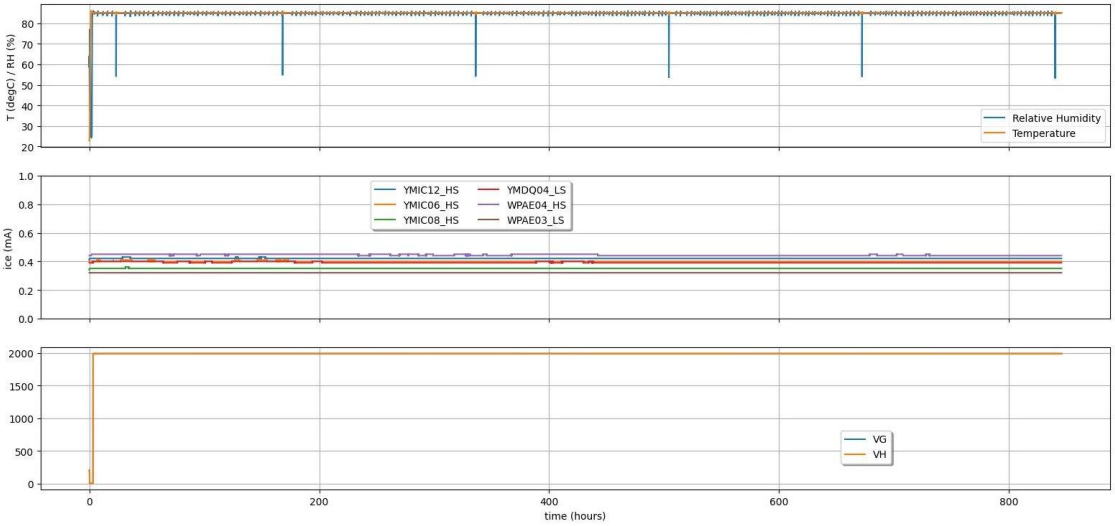


Figure: 48: H_3TRB of the 3.3kV SiC LinPak modules HE internal modules, WPAE modules external chip modules. Ambient temperature, relative humidity monitors over time are shown in the first (top) plot. Collector emitter leakage currents over time for all modules (mid-plot). Applied V_{CE} voltage (bottom plot). For the full test the I_{CE} was within system noise level.

The 6.5kV Si and SiC HV LinPaks were also tested under the same conditions as mentioned above for the H_3TRB test. The Si LinPaks passed the test up to 800h. The first SiC LinPak was failing with a drain to source short at 300h and 500h (Figure: 50). It must be noted that this failure is not impacting on the operation of the modules in converter applications and that it will be interesting to investigate further the long-time reliability of the module in high humidity application.

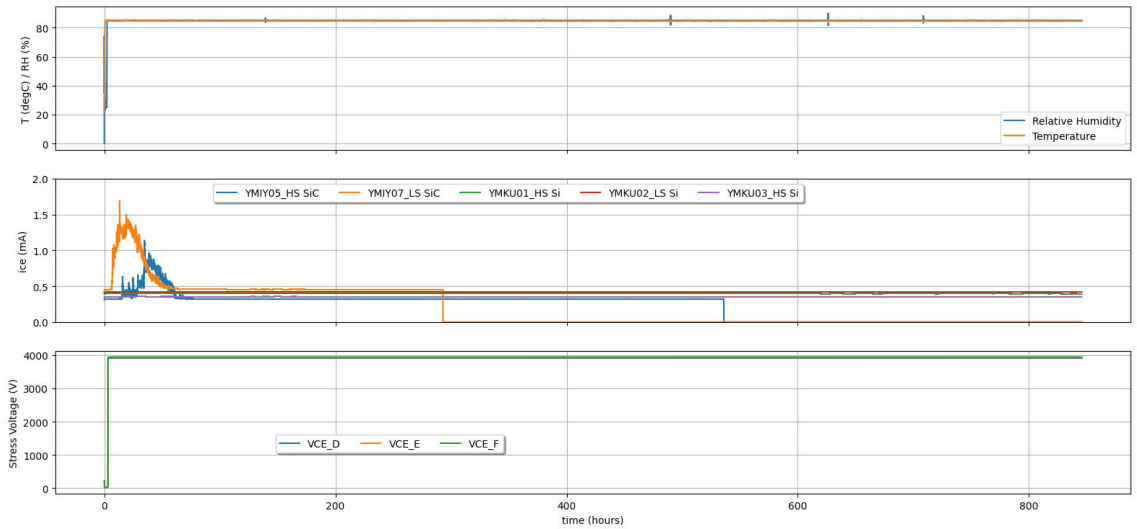


Figure: 49: H_3TRB test of 6.5kV Si vs SiC LinPak. Ambient temperature, relative humidity monitors over time are shown in the first (top) plot. Collector emitter leakage currents over time for all modules (mid-plot). Applied V_{CE} voltage (bottom plot). For the full test the ice was within system noise level.

3.2 Power Cycling Results

In power cycling the modules are repeatedly switched on and off to simulate thermal and electrical stress as close as possible to application-related conditions. It is widely used in reliability testing of power semiconductors, to evaluate how the interfaces from chip towards substrate, bond-wires to chips and substrate to baseplate are robust towards thermo-mechanical stress propagation. The failure mechanisms can have internal reasons linked to the design, material selection and degradation of the thermal path within the semiconductor module itself and can also be linked to external reasons given by the outer thermal interfaces and cooling physics.

We have carried out power cycling on the Si and SiC LinPaks to understand the behavior of the two different interfaces substrate to baseplate and chip to substrate. In our first power cycling experiment we focused on investigating the interface substrate to baseplate with the Si LinPaks. The solder used is the same in Si and SiC LinPaks.

The power cycling test was carried out on the 600A version of the 3.3kV LinPak which design is compatible with the 6.5kV 300 A version. The modules have the same termination design, same chips size and same internal layers such as chip solder material and substrate solder.

For the testing of the Si modules, we were interested in understanding the solder quality between the substrate and the base plate. Therefore, we choose as test conditions the PC_{min} conditions. We tested 10 modules and kept two reference modules.

3.2.1. Test conditions and failure criteria

The PC_{min} test was done with the test conditions:

- t_{cycle} = 60s (t_{on} = t_{off} = 30s)
- Current level 650A
- T_{jmax} = 130°C, dTj = 90..105K
- Expectation: B50% = 53.70k cycles
- Final number of cycles 64400 cycles

The number of cycles until failure is achieved if one of the following applies:

1) Vce increase higher than 5%
2) Thermal resistance junction to case (Rth_{jc}) increases higher than 16%
3) Thermal resistance junctions to ambient (Rth_{ja}) increase higher than 20%
4) Catastrophic failure, mainly due to gate short and steep increase of V_{ce}

The test was run as long as possible to determine the lifetime due to solder degradation. All devices were evaluated with respect to the thermal resistance junction to case (Rth_{jc} > 16%) failure criteria indicating solder degradation.

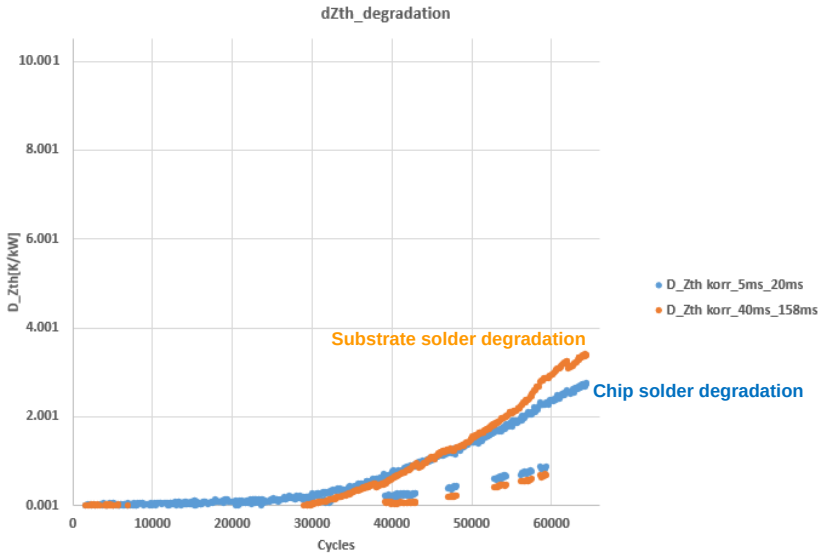


Figure: 50: dZ_{th} degradation curves-chip/substrate/thermal interface.

In Figure 51 the results of the power cycling results are displayed. The D_Z_{th} (transient) value was calculated for the different interfaces in correspondence to the cycle numbers. It describes the change of the thermal interface in the thermal resistance by an absolute value in K/kW over the cycles. After 30000 cycles the solder degradation is slowly starting between chip solder and substrate solder. After 60000 cycles the R_{th} increased more than 16% therefore the test was stopped. Figure: 52 describes the number of cycles until failure (lifetime) over the stress parameter dT_j. For example, at a dT_j of approximately 108 K the maximum possible lifetime is 40000 cycles for the Si LinPak device. We see a clear dominant failure mechanism and the typical degradation patterns. We can therefore assess the final result as a “passed”, the modules fulfill the application note.

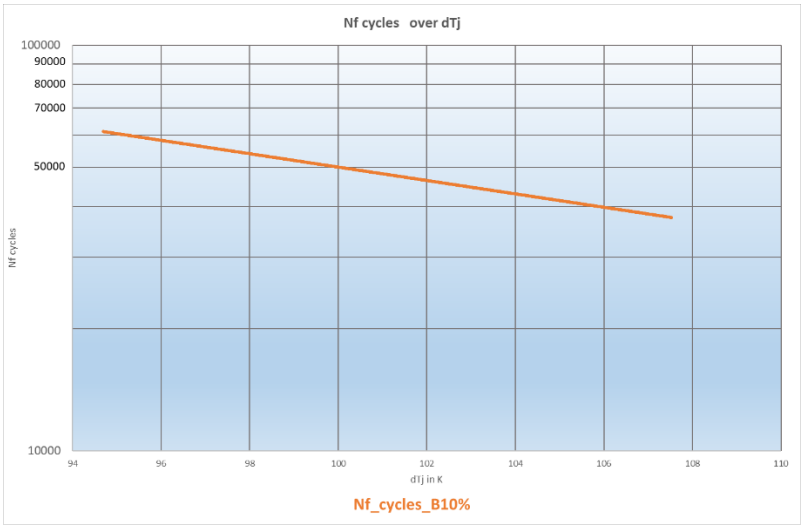


Figure: 51: dZ_{th} degradation curves-chip/substrate/thermal interface (N_f= final cycles until failure)

3.2.2.SAM pictures- typical examples

The SAM pictures of the PC_{min} test show the substrate solder (first row) and chip solder degradation (2^{nd} row) interfaces, the last shows also the condition of the emitter surface including the wire bonds.

From the pictures of the substrate solder and emitter /chip solder interface we see the high degradation effect on the chip solder, see red arrows (Figure: 53). The substrate solder seems to be more homogeneous affected by a general coarsening effect; the number of small voids increases very strongly resulting in a bright grey color. There are no typical void patterns at the substrate edges visible. The ultrasonic welded terminal feet look also very robust after the PC testing, see blue arrows.

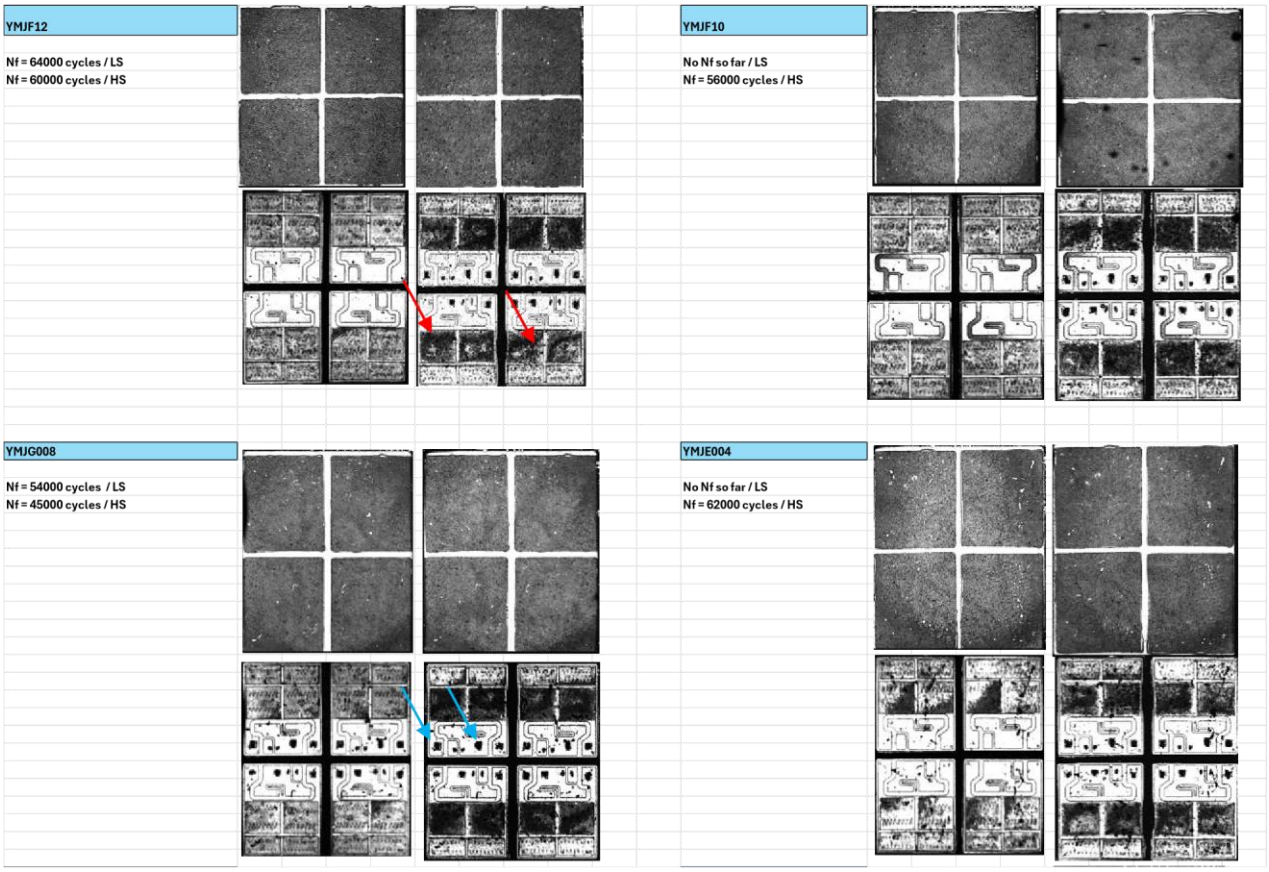


Figure: 52: SAM analysis of the first four Si LinPaks at different final cycles until failure.

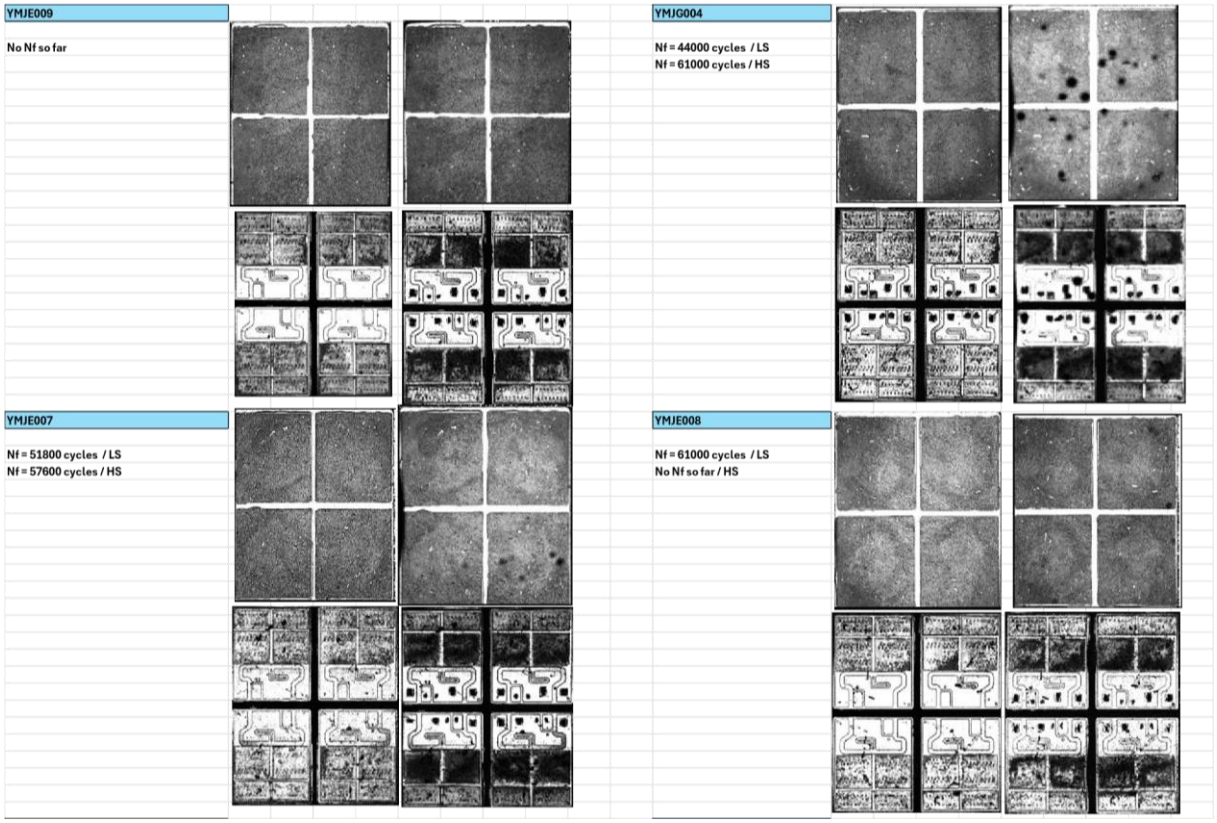


Figure: 53: SAM analysis of the other four Si LinPaks at different final cycles until failure.

3.3 Power cycling of the SiC 3.3kV LinPaks

The goal of the power cycling was to investigate the performance of soldering vs sintering of the SiC chips on the substrate. We have decided to test power cycling with the 3.3kV SiC LinPak which is compatible in design with the 6.5kV SiC LinPak. The modules have the same termination design, same chips size and same internal layers such as chip solder material and substrate solder. The power cycling was tested on the internal chip modules as well as the external chip modules. The test conditions can be found in Table 9.

Table 9: Variations of the SiC DUT tested in power cycling

Variation	Wire bonding	Die attach	Chip	Result
1	Al wire (12.5 A/wire)	soldering	3.3kV HE chips	<10% lifetime fulfillment, early failure
2	Al wire (12.5 A/wire)	sintering	3.3kV HE chips	<10% lifetime fulfillment, early failure
3	Al wire (3.3 A/wire)	soldering	3.3kV external chip	85%-110% lifetime fulfilment. Failure due to solder degradation, observed wire degradation
4	Al wire (3.3 A/wire)	sintering	3.3kV external chip	95%-135% lifetime fulfilment. Failure due to wire-lift off and chip alu degradation, no sinter degradation

The modules are subjected to a static hot and static cold test prior to power cycling to evaluate the baseline values of V_{on}, R_{on} and V_{th}. The cooling is carried out with water flow of 7 l/min, with an inlet temperature of 35°C. The test conditions have been selected considering the main key points of the PC_{sec} test provided in the AQG324 guideline. The VSD_{on}, dT_j, Z_{th}, R_{on} and V_{th} are monitored during the tests for every module. The failure is identified with an increase of Von of more than 5% or of Z_{th} of more than 20%.

Table 10: Power cycling conditions for modules comparing soldering vs sintering

Parameter	Variant 1	Variant 2
Cycle time, T_{cycle}	5s	5s
Heating/cooling time, T_{on}/T_{off}	2.5s	2.5s
Temperature rise, dT	85-90K	85-90K
Temperature current	21A	21A

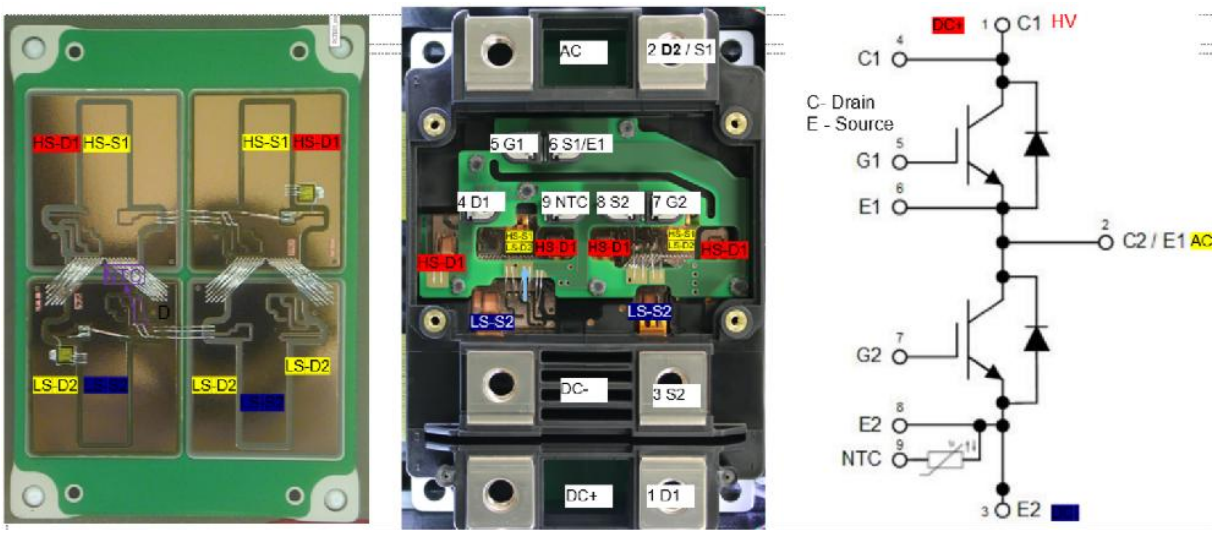


Figure: 54:Variant 1 and Variant 2 module assembly

3.3.1.Test results Variant 1

Table 11:Results of power cycling of Variant 1

DUT	Tn max start	Tn min start	VDS_{on} hot start	dT start	Cycles VDS_{on} hot 105%
1 LS	136	52	5.37	85	10.35k
1 HS	126	53	4.76	73	27.4k
2 LS	138	54	5.36	84	10k
2 HS	129	50	5.06	79	17k
3 HS	146	60	5.35	85	9.6k
3LS	129	51	4.94	78	17.5k
4 HS	140	51	5.30	90	11.1k
4 LS	127	46	4.99	81	18k

Table 12: Results of power cycling Variant 2

DUT	Tn max start	Tn min start	VDS_{on} hot start	dT start	Cycles VDS_{on} hot 105%
1 LS	124	51	5.32	73	7.9k
1 HS	119	49	5.10	70	11.4k
2 HS	141	59	5.88	83	7.97k
2 LS	130	51	5.78	79	9.96k

In the post cycling electrical tests V_{th} has a positive shift (+2 V) and Rds,on (+5-10%) increase.

In conclusion, the modules show an early failure due to 5% increase $V_{onstate}$, the fulfilment of lifetime is <10%. All modules are assembled with internal chips, this test, the chip was identified as the lifetime limiting factor.

Reasons could be:

- Charge trapping in the gate oxide or interface states, leading to a threshold voltage increase.
- Aging effects or degradation in the semiconductor material.
- Increased gate resistance, affecting switching characteristics.
- Thermal stress causing permanent shifts in device parameters.

3.4 Testing of Variant 3 and 4

These modules are built with 3.3 kV external chips and Ag sintering vs soldering of the chip was compared.

Table 13: Test conditions for power cycling of Variant 3 and Variant 4

Parameter	Variant 3/4
Cycle time, T_{cycle}	5s
Heating/cooling time, T_{on}/T_{off}	2.5s
Temperature rise, dT	85
Test current	21A
Calibration current	33 mA
V_g	8V
Z_{th}	interval 720 cycles (1h); 30s delay, 120s heating (at 20 A), 120s cooling
T_{jmax}	150°C

3.4.1. Test results

Table 14: Summary of test results of 3.3kV external chip modules Variant 3 and Variant 4

DUT	type	N_f	dTj	T_{jmax}	failure	life-time-ex-pected B10%	DF
1	solder	142000	91.75	132.12	Vds > 5%	126061	112.64%
2	solder	135000	88.83	129.29	Vds > 5%	152268	88.66%
3	Ag sinter	173168	89	144	Vds > 5%	98608	175.61%
4	Ag sinter	144994	83	143	Vds > 5%	119268	121.57%
5	solder	106214	77.98	153.23	Rth>20%	116546	91.13%
6	solder	110554	75.87	150.69	Rth>20%	130262	84.87%
7	solder	154692	74.09	149.24	Rth>20%	142709	108.40%
8	solder	130990	73.07	148.01	Rth>20%	152144	86.10%
9	solder	111454	77.67	152.34	Rth>20%	119294	93.43%
10	solder	132761	75.75	150.86	Rth>20%	130438	101.78%
11	solder	117552	74.78	149.71	Rth>20%	137857	85.27%
12	solder	75000	109	149.88	Rth>20%	81145	124.00%
13	solder	77000	93	148	Rth>20%	94339	92.00%

For the sintered samples, the power cycling failure mechanism is Vds_{on} increase which was caused most probably by wire-lift-off/wire degradation/fusing. In the failure analysis a lift-off of the wires from the LS chip can be observed, furthermore the colour changes of the top of the chip shows degradation of the Al layer on top. The cross-section images show a good soldering and sintering adhesion of the chip to the substrate and the remaining on the chips of Al coming from the lifted wires.

In the test the solder degradation was the root cause of failure as well as wire-lift-off could be observed. The R_{th} >20% and Von < 5%. The chip topside and the die-attach are known from literature as competing mechanisms. The die-attach with the solder reaches end-of life whereas the die-attach of the silver sinter does not pose a lifetime limitation. Nevertheless, when comparing the lifetime performance of the solder die-attach is comparable to the silver sintering system.

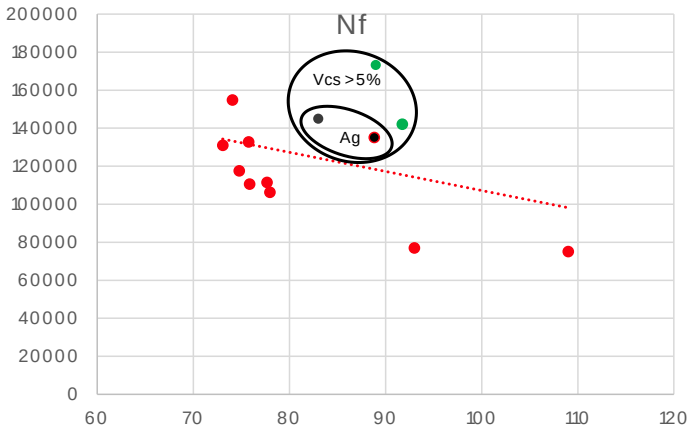


Figure: 55: Graph displays on the y-axis the number of cycles until failure and on the y-axis the dT_j value.

For the power cycling results we can conclude that the packaging is withstanding the power cycling test without any question. In the SiC modules we have investigated the interface between the substrate and the baseplate and could find that solder material chosen is a good candidate also in future assemblies. Our investigation soldering vs sintering of the chip dies is giving a comparable lifetime performance (Figure: 56), which is the reason why soldering was chosen for the overall die-attach in this project (see section

4 Half-Bridge converter, 3.3 and 6.5kV

Due to the increasing efficiency of power electronic systems, the exact determination of power losses becomes increasingly important. Whereas the characterization of the SiC modules provides the basic information necessary for the design of power converters such as static and switching losses as well as SOA, reliability and ruggedness, it does not assess its behavior in real applications. In order to address those features, we will test the technology demonstrators into 3.3 and 6.5 kV half-bridge single-phase converters, which is the basic building block for most of converter topologies (DC-to-AC converters, most AC/AC converters, the DC-to-DC push–pull converter, isolated DC-to-DC converter), and thus a very flexible and robust platform to evaluate power semiconductor modules in applications. Further, we will build similar Si IGBT H-bridge converters to assess performance improvement of the SiC counter-part. The SiC and Si LinPak modules will be provided by Hitachi Energy to achieve a fair comparison. Based on the literature in SiC converters, we target the converter demonstrator efficiency between 96-98% for the Si IGBT converter and >99% for the SiC MOSFET converter.

The final power specification of the 3.3 and 6.5 kV H-bridge converters is dependent on the current rate of SiC module, but we estimate it to be about 225 kW and 275 kW average single-phase AC power, respectively.

The converter mechanical arrangement and topology of the Si IGBT will be the same as that of the SiC MOSFETs, but in the late case, it will be optimized for low stray inductance. The main difference will be related to the gate drives. Because of the challenge to supply very high current, we will use a power electronics topology that recycles the half-bridge converter current, thereby overcoming power limitations. One traditional technique to characterize high-power inverters losses is based on the opposition method. This technique consists of connecting two identical systems in a back-to-back connection, allowing them to circulate high power between the systems with a low-power electrical source and without the use of dissipative loads. The physical principle is demonstrated in Figure: 57, where the power source provides only power losses ($P_{losses1}$ + $P_{losses2}$). At the same time, a high-power (P1) circulates between the systems. This is possible because there is no dissipative load consuming active power. Consequently, the power supplied by the source is low when the system operates at nominal conditions, presenting a significant reduction in the facility requirements.

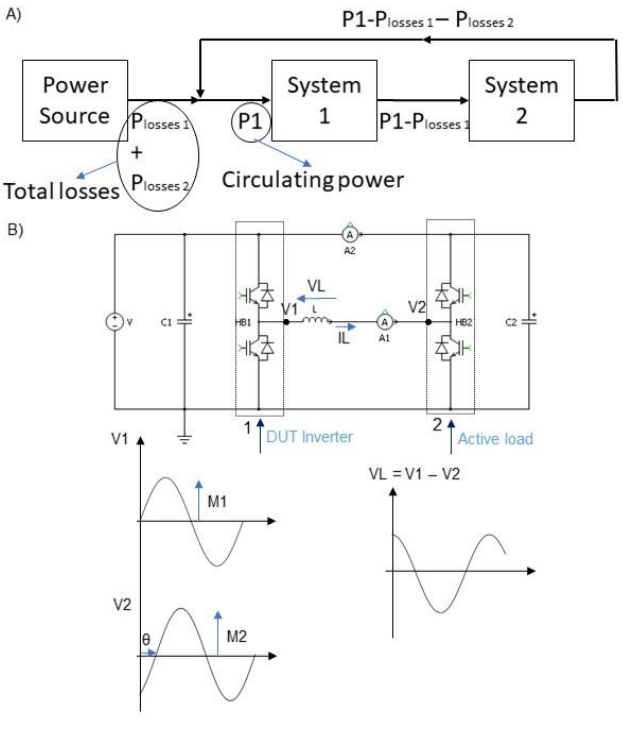


Figure: 56: Single line diagram of Half-bridge converter characterization tester.

Here, the system is composed of two half-bridge legs, identical to a traditional H-bridge inverter. The first leg is the device under test (DUT), and the second one acts as an active load, modulating the AC

voltage at 50Hz. An inductor is connected to limit the current due to the differential voltage between the h-bridge legs. By using a sinusoidal pulse-width-modulation (SPWM) control is possible to adjust the fundamental voltage vectors (V1, V2) of the two legs to control the magnitude and phase angle of the voltage across the inductor L (VL = V1-V2). Such control is performed by changing the modulation factors (M1, M2) that are responsible for the amplitude voltage control from each leg and the phase shift (θ) between V1 and V2 (Figure: 19B). To characterize the inverter losses under a specified operating condition, the inductor voltage (VL) is selected to achieve the desired inductor current (IL = VL/XL). For an inverter designed with the 3.3 kV/450A or 6.5 kV/300A LinPak module from Hitachi Energy, the nominal power of about 200-250 kVA can be easily achieved with the opposition method. Furthermore, the switching frequency can be changed to investigate the losses under a range of operational frequencies. Since the MV Si IGBT modules typically do not operate at frequencies higher than 2kHz because of excessive power losses, and thus heating, we will compare the different semiconductor technologies at frequencies starting at 450 Hz till 2000 Hz. At higher frequencies, the module requires down rating the current to compensate for the switching losses for the conduction losses. Further, at higher frequencies reliability of the motor and bear rings becomes a major issue.

The converter is targeted to operate at 1.8kV for the 3.3kV rated modules, and at 3.6kV for the 6.5kV.

To allow fair comparison between the Si IGBT and SiC MOSFET modules in the converter application, we will build similar heatsinks and electromagnetic components for both semiconductors.

4.1 Converter design

The topology presented in Figure: 57 is implemented for the 3.3 kV Si IGBTs LinPak modules from Hitachi Energy. Each part of the system design is detailed in the following topics.

The rated values for the state-of-the-art Si IGBT modules to be tested are 3.3 kV/450 A and 6.5 kV/300 A. The SiC MOSFET module has a rated value of 3.3kV/500 A. The 3.3 kV voltage class is extensively used in railway traction applications with DC links in the range of 1.5 – 1.8 kV, requiring a 2-level topology. The 6.5 kV voltage class is implemented in 2-level topologies for railway traction applications with DC link voltage of 3 kV. The 3.3 kV voltage class can also be used for 3 kV DC link applications by implementing 3-level inverter topologies. The B2B system was designed to operate at a typical DC-link voltage of railway traction inverters. The maximum load current of about 70 % of the module nominal current is selected, a typical derating condition in real converters to guarantee long-term reliability [83] and safe operation. The range of switching frequencies to be tested is selected according to typical values in industrial traction converters and junction temperature limitations. The modulation factor (M) was fixed at 0.9 for both legs to simplify the selection of test parameters, with the circulated current chosen by the load leg's phase shift (θ). The fundamental frequency (f) is fixed for steady-state operation

at 50 Hz. The design also guarantees a 12 % load current total harmonic distortion (THD) at the worst case for the lowest switching frequency of 500 Hz. The circulated power between legs is calculated based on the selected load current, DC-link voltage and modulation factor. Table I shows the converter operating parameters for each power module.

Table 15: Converter requirement specification

	3.3 kV/450 A Si IGBT converter	6.5 kV/300A Si IGBT converter
DC link voltage (V)	1.5 or 1.8 kV	3 or 3.6 kV
Switching frequency (f_s)	500 – 1250 Hz	500 Hz
Inductor current range (I_L)	0 – 300 A_{rms}	0 – 210 A_{rms}
Circulated power (P_{cir})	0 – 153 kW	0 – 226 kW
Modul. factor (both legs) (M)	0.9	0.9
Fundamental frequency (f)	50 Hz	50 Hz
Current THD at 500 Hz	~ 12 %	~ 12 %

4.1.1.Capacitor and load inductor selection

Based on the current load equation and considering the input DC link voltage (V) as 1.8 kV, fundamental frequency (f) of 50 Hz, fixed modulating parameters from both legs M1 = M2 = 0.9, maximum inductor current (IL) of 280 Arms, and the maximum θ angle (free variable to be controlled) chosen to be smaller than 25 degrees (0.436 rad), an inductance value (L) equal to 2.8 mH is obtained. A value of L = 2.5 mH was chosen in the design.

To determine an analytical equation for the desired capacitance value as a function of the ripple voltage, it was assumed that the capacitor entirely provides all circulating current in the system.

This assumption is an excellent approximation because the power supply provides the power losses (current smaller than 10 Arms and limited by the power supply rating), and the capacitor provides the circulating current to the system (up to 280 Arms). Figure: 58 shows the waveforms from the inductor current (top) and the capacitor voltage (bottom). It can be seen a continuous energy transfer between the inductor and the capacitor, while the power supply provides a small current to the capacitor to re-charge it and keep its voltage fixed around V.

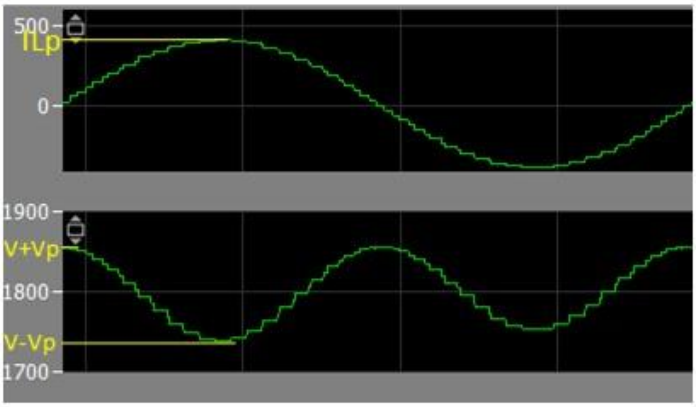


Figure: 57: Simulated inductor current (top) and capacitor voltage (bottom) during operation. V = 1800 V, L = 2.5 mH, M1 = M2 = 0.9, θ = 22º, C = 1mF, fs = 2 kHz, f = 50 Hz.

Using energy conservation (Eq. 1):

$$\frac{1}{2}\mathrm{C}(\mathrm{V}+\mathrm{Vp})^2 = \frac{1}{2}\mathrm{L}\,\mathrm{ILp}^2 + \frac{1}{2}\mathrm{C}(\mathrm{V}-\mathrm{Vp})^2 \quad (1)$$

Where:

C: Dc link capacitance (F); V: Dc link voltage (V); Vp: Half ripple voltage (V); L: Load inductor (H); ILp: Peak inductor current (A).

Since the ripple voltage (Vr) is 2*Vp, we have from Eq. 1:

$$\mathrm{C} = \frac{\mathrm{L}\,\mathrm{ILp}^2}{2\mathrm{V}\,\mathrm{Vr}} \quad (2)$$

Using ILp = sqrt(2) * I_L(rms) in Eq. 2:

$$\mathrm{C} = \mathrm{L}\frac{\mathrm{IL}^2}{\mathrm{V}\,\mathrm{Vr}} \quad (3)$$

Equation 3 is compared to the simulation in Figure: 59 for the worst-case scenario (full load – I_L = 280 A_{rms}). The good agreement validates the proposed model and allows the designer to choose a capacitance value that obey the 10% ripple requirement.

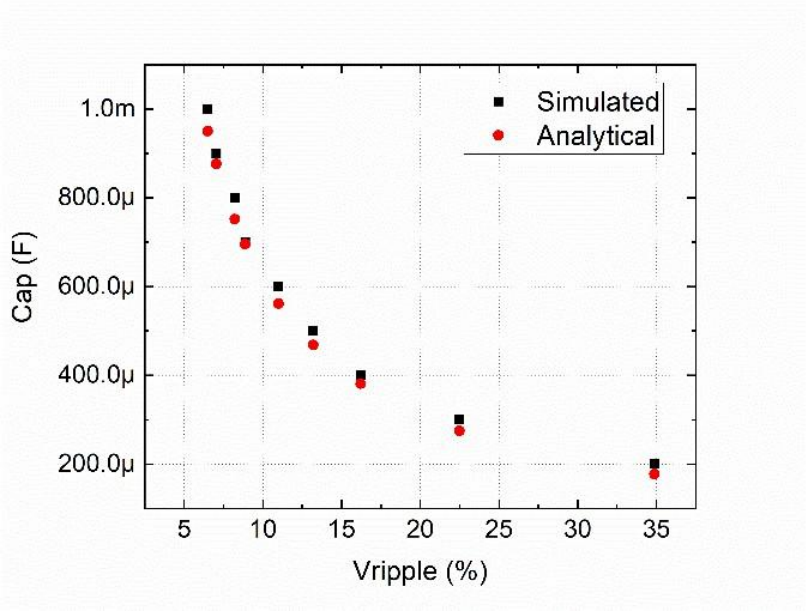


Figure: 58: Capacitance value versus voltage ripple at full load conditions (IL: 300 A, V: 1.8 kV).

The selected capacitor model is the B25645A2677K003 from EPCOS-TDK Electronics, which presents a capacitance of 670 µF, Vmax of 2.3 kV and stray inductance of 14 nH. Performing a series-parallel association of 6 capacitors, an equivalent capacitance of 1 mF that corresponds to a ripple of ~ 7% at full load and an equivalent stray inductance of ~ 10 nH. Such low stray inductance is essential to avoid overvoltage during the semiconductor switching. This design choice guarantees a ripple always smaller than 10 % for any converter combination shown in Table 15.

4.1.2.Busbar design and cooling design

A two-layer laminated copper busbar has been designed to optimize the system's stray inductance. A 15 mil thick Kapton layer has been used for electrical isolation (> 30 kV) between the copper layers and to achieve a low stray inductance busbar (estimated ~ 10 nH). The estimated stray inductance of the power loop considering busbar, power module packaging and capacitors are in the range of 30 nH, which is optimized for ultra-fast switching without creating high overvoltage that could kill the device during turn-off.

For an efficient heat transfer between the power modules and the active cooling, a cold plate from ATS (model ATS-CP-1000-DIY) has been selected. This cold plate can provide a low thermal resistance of around 10 mK/W and is mechanically compatible with the LinPak module dimensions. A thermal paste is used as an interface material between the module case and cold plate to improve heat transfer by reducing the thermal contact resistance.

4.1.3.Gate driver design

The gate driver is a power amplifier circuit that switches on and off the semiconductor. Such a circuit receives low-power signals from the controller and produces a high-current drive input for the semiconductor gate terminal. Furthermore, the gate driver provides system protection under short-circuit events and must be well-designed to provide clean switching waveforms and low switching losses. A gate driver has been designed with Rogowski coil-based short circuit protection [84], optical fiber signal connections to improve noise immunity, 12 kV voltage isolation and creepage distances respecting medium voltage standards for safe operation. Two variants were designed due to the different footprints from the 3.3 and 6.5 kV modules. The gate driver specifications for the 3.3 and 6.5 kV modules are shown in Table 16.

Table 16: Gate driver requirements for each power module

	3.3kV/450A Si	3.3kV/500A SiC
Gate Voltage	-10 / +15 V	-10/ +15 V
Immunity	~25 V/ns	~50 V/ns
Gate resistor	1.5 Ω (on and off)	2.4 Ω (on and off)*
Max Gate current[1]	35 A	35 A
Max frequency[2]	10 kHz	10 kHz
Operating voltage	1.8 kV	1.8 kV
Power gate[3]	3 W	3 W

[1]Calculated from Imax=ΔVg/Rg; A gate voltage sweep (-10 to +20 V) and Rg = 1.5 Ω was considered. A margin of + 15 A has been added.

[2]The maximum operating switching frequency is not larger than 5 kHz for SiC and 2 kHz for Si due to thermal limitations. 10 kHz is considered to add a design margin.

[3]Calculated from Pg=Qg*f*ΔVg; frequency was considered 10 kHz, ΔVg was considered 30 V and gate charge of ~ 5 µC. 1.5W of margin has been added.

*It was also tested the case of RG = 24 Ω for slower switching investigation.

The gate driver structure and PCB plane connections are shown in Figure: 60. A 12 kV DC-DC converter isolates the power supply connected to the grid from the circuit. A low 4 pF coupling capacitance is required to avoid common mode signal coupling. A current booster is implemented to achieve the desired peak current. Isolated power supplies were used to feed the optical fibers and Rogowski processing circuit. Protections like UVLO, OVLO, and soft turn-off were considered in the gate drive chip choice.

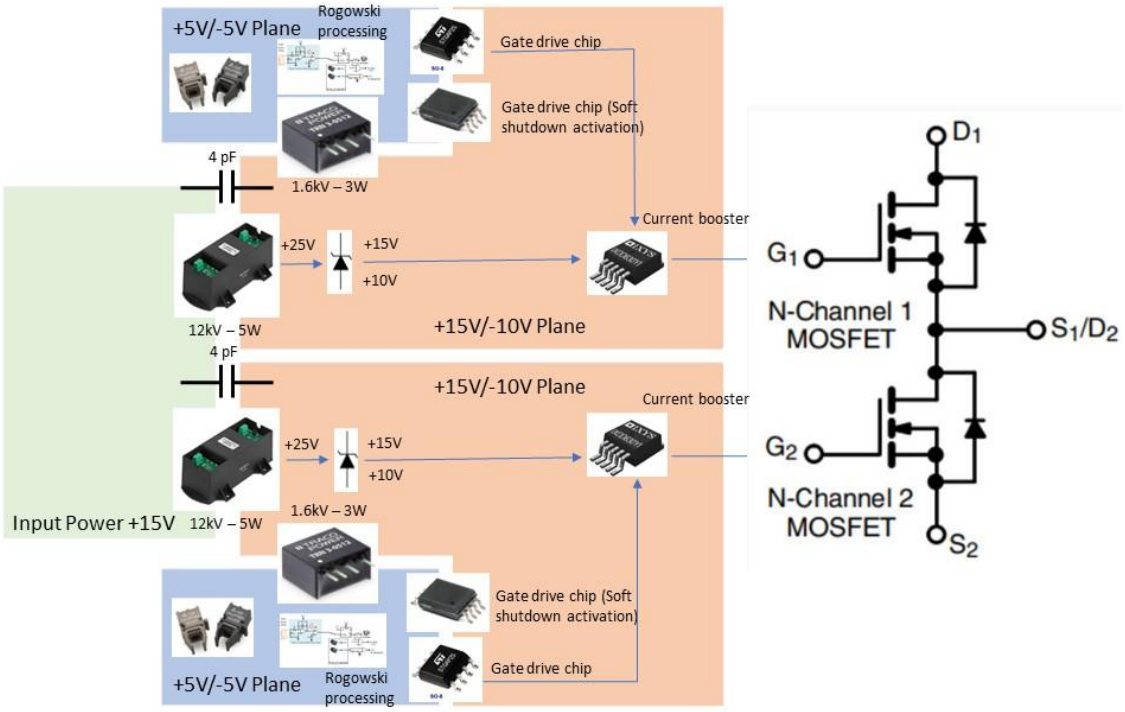


Figure: 59: Gate driver main components and power plane connections.

4.1.4.Controller design

A TMS320F28379D microcontroller from Texas Instruments performs the angle control and PWM generation. A dedicated PCB, shown in Figure: 61, has been designed to integrate the microcontroller board, optical fiber connections and current sensor. Two different control strategies have been performed: one operating at open feedback loop and a second one at a closed feedback loop. In the closed feedback loop option, the load current is measured by a current sensor, and the controller automatically sets the phase shift. For the open loop control method, the user sets the phase shift according to a look-up table, and no current sensor is required.

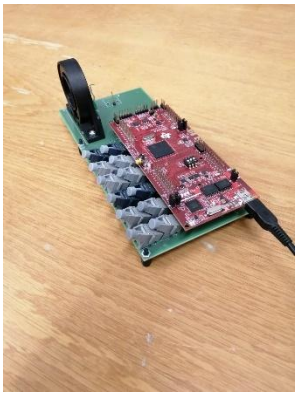


Figure: 60: Microcontroller board with integrated optical connectors and current sensor.

4.1.5.Converter test bench

The final assembled of the converter test bench is shown in Figure: 62. The system is built on a grounded aluminium plate, and acrylic protection is added for additional safety.

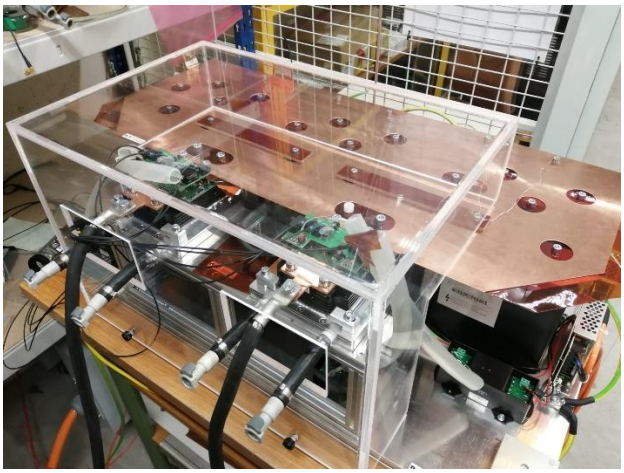


Figure: 61: Back-to-back converter.

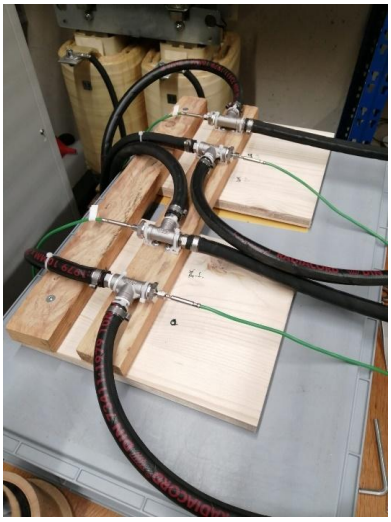
4.2 3.5. Thermal system and characterization method

In this section, we initially describe the power converter cooling system and sensors used in the temperature and flow measurements to characterize the converter losses during steady-state operation. We later discuss the power loss characterization protocol based on this initial description.

The cooling system comprises one cold plate for each Linpak module (2 modules in total) responsible for the convection heat transfer between the power module and the water flow. Rubber pipes connect the cold plates to an air-colled 6.5kW chiller unit responsible for removing the heat to the environment. A Coriolis flow meter is then used to accurately measure the water flow with an accuracy of 0.1%. Four thermocouples (K type – 1 mm thick) were placed in the inlet and outlet of each cold plate to measure the fluid temperatures. The thermocouples have been calibrated in oil bath to achieve an accuracy of ± 0.1 ^{o}K. Figure: 63 shows the chiller unit, the thermocouples placed in the pipes to measure the inlet and outlet temperatures and the power converter integrated with the cooling system.

a

b



c

Figure: 62: (Top-left) Chiller unit. (Top-right) Thermocouples placed in the inlet and outlet of each coldplate. (Bottom) Power converter with cooling system.

Our main goal is to determine the power module's individual losses and converter efficiency. Two methods will be used to characterize the H-bridge converter losses. All measurements will be performed once the converters are ready for safe operation and after 30 min of continuous operation to avoid any transient behavior. Systematic uncertainties will be determined for each measurement technique individually.

1) The first characterization is based on the water flow exchanger method [2]. Here, the semiconductor power losses can be directly obtained using a water-cooled system for the power modules. The principle is based on the heat exchange between the coolant and the semiconductors. Therefore, the coolant flow rate and the inlet and outlet differential temperature must be properly measured (see Figure: 63). Equation (1) shows the relation between semiconductor power losses, the input and output differential temperature and the coolant flow rate.

$$P_{loss} = \Delta T * c * \rho * Q \qquad (1)$$

where P_{loss} is the semiconductor losses (W), ΔT is the inlet and outlet water differential temperature (K), c is the water-specific heat capacity (J/kg.K), ρ is the water mass density (kg/m^3), and Q is the water volume flow rate (m^3/s).

An estimation of the expected measurement error is shown below, considering typical parameter values.

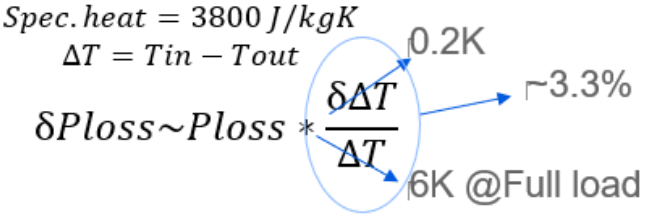
$$Flow = 8.33 * 10^{-5} \pm 0.09 * 10^{-5}\ m^3/s$$

$$density = 1028 \pm 2\ \frac{kg}{m^3}$$

$$Spec.heat = 3800\ J/kgK$$

$$\Delta T = Tin - Tout$$

$$\delta Ploss \sim Ploss * \frac{\delta \Delta T}{\Delta T}$$



This method consists of a simplified version of the calorimetric method. It presents relative errors of around 3 % at full load with a decrease in accuracy for low power losses due to the smaller differential temperature (reaching up to around 10% at sub load conditions). A possible solution for this problem is reducing the coolant flow rate to increase the differential temperature [2].

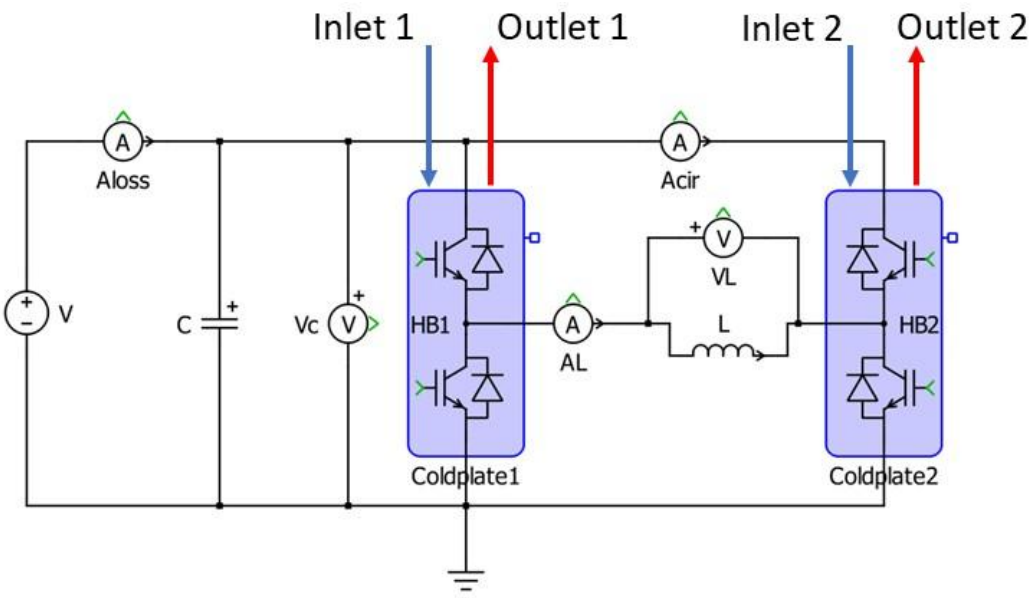


Figure: 63: Back-to-back monophase converter with thermal system inlet-outlet indications for each coldplate and electrical measurement points.

2) The second characterization is based on the opposition method [2]. Here, we electrically measure the voltage and currents using a power analyzer (Model: Hioki PW8001). The overall losses are measured directly from the power supply. To obtain the semiconductor power losses, the inductor losses must be estimated. Therefore, we aim to measure the inductor losses (PL = VL * AL), total power losses (Ploss = Vc * Aloss) and circulated power (Pcir = Vc * Acir). The measuring points are indicated in Figure: 64.

The converter efficiency can be obtained from Eq. (2) for the back-to-back converter [3]:

$$\eta = 1 - \frac{Ploss}{Pcir + Ploss} \quad (2)$$

An error propagation method will be applied to each voltage and current harmonics to estimate the measurement accuracy.

Both methods constitute state-of-the-art power losses and efficiency measurements in medium voltage power converters. Their results will be compared to provide a consistent and reliable analysis.

For further investigation of the thermal characteristics of the modules, one essential parameter is the semiconductor junction temperature (T_j). Such parameter is directly related to the thermal stress the semiconductor is subjected to under an operation point and to the semiconductor/packaging operating

limits. Here, we propose using micro thermocouples placed directly underneath the power semiconductor substrates, also known as the power module case, and the average temperature measured (T_{case}). By knowing the junction-to-case thermal resistance of the module (R_{thjc}) and the characterized power loss (P_{loss}), we can estimate the temperature of the chip (Tj) [3], as shown in Eq. (3).

$$Tj = T_{case} + R_{thjc} * P_{loss} \qquad (3)$$

Where Tj is the junction temperature (K), T_{case} is the case temperature (K), R_{thjc} is the junction to case thermal resistance (K/W) and P_{loss} is the semiconductor loss (W).

By measuring the junction temperature, we can investigate the operational limits of the power modules for each switching frequency and load current.

It is essential to have an accurate calibration procedure to perform accurate loss measurements employing the thermal method. Initially, the four K-type thermocouples were calibrated with the measuring tip (hot junction) immersed in an oil bath at a controlled temperature (error of ± 0.1 ºC), and the cold junction was placed into an ice bath (0 ºC). Such measuring procedure avoids the use of look-up tables and cold junction compensation algorithms that may add errors and loss of accuracy of the measurement. Figure: 65A shows the thermocouple output voltages in a temperature range of 15 up to 35 ºC. All thermocouples presented a slope of 39.8 ± 0.1 µV/ºC, which agrees with the datasheet of K-type thermocouples.

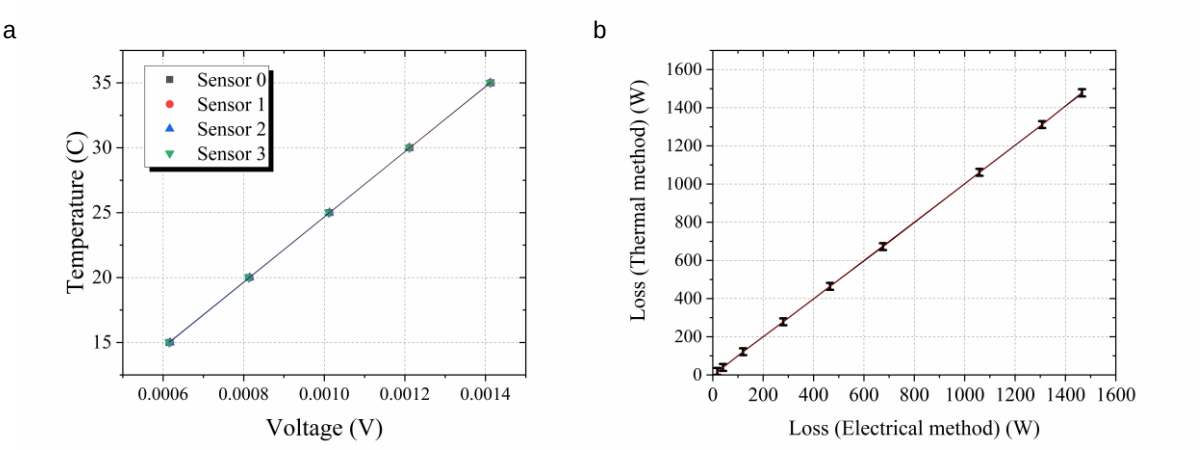


Figure: 64: K-type thermocouples calibration curves performed in an oil bath with the cold junction in the ice bath reference (0 ºC). The error bars are very small. The temperature error is ± 0.1 ºC, and the voltage error is ± 2 µV. All thermocouples presented a slope of 39.8 ± 0.1 µV/ºC, which agrees with the datasheet of K-type thermocouples, B. Comparison between electrical and thermal measuring methods. The electrical method is used as the reference since the error is extremely small for DC measurements (~ 0.05 %). The curve slope is 1.005 ± 0.002, presenting an excellent match between thermal and electrical characterization methods, with an error smaller than 1 % at high power loads.

After the thermocouples calibration, possible systematic errors were evaluated in the water flow exchanger method that may be caused by uncertainties in the coolant density and specific heat-capacity values (see Eq. 4). We have employed Antifrogen N – 30 % [86] as coolant fluid. Based on datasheet

values at 25 ºC, a mass density of 1035 kg/m3 and a specific heat capacity of 3750 J/kg.K were used. To verify possible systematic errors, different DC currents were passed through the IGBT LinPak module placed on top of a cold plate. Such configuration is the same used in the final back-to-back converter. Thus, the power losses could be compared using the power analyzer and thermal method. The electrical method in such case is used as the reference since, at DC parameters, the power loss measurement accuracy is very high (~ 0.05 %). A comparison between the electrical and thermal method measurement values is shown in Figure: 65B. The curve slope is 1.005 ± 0.002, presenting an excellent match between thermal and electrical characterization methods, with an error smaller than 1 % at high power loads and 3 % at sub load conditions.

4.2.1. Converter characterization

The first part of this chapter demonstrates the experimental power loss characterization of the Si and SiC-based power converters in the B2B configuration. The electrical curves are indicated, and the converters' power losses and efficiency under distinct operating conditions are compared. In the second part of the chapter, an electro thermal simulation model is developed to accurately simulate the power losses of a traction inverter. The model's accuracy is validated based on experimental data.

4.2.2. Losses and efficiency characterization

This section focuses on the power losses and efficiency characterization of the Si and SiC power modules operating in a B2B configuration. The test conditions are indicated in Table 17 for the 3.3 and 6.5 kV device-based converters. The 6.5kV SiC modules have not been analyzed in the converter, due to module failure during operation which led to damaging of the converter. The root cause of this failure is still under investigation at Hitachi Energy and FHNW. We nevertheless have performed the assessment of energy potential saving in 6.5kV based traction converters using such modules based directly on the semiconductor characteristics, instead of converter measurements. The nominal current of the 3.3 and 6.5 kV Si and the 3.3 kV SiC power modules are 450 A, 300 A and 500 A, respectively. The system was designed to operate at a maximum load current of about 70 % of the module nominal current, a typical condition in real converters to guarantee long-term reliability during operation. Figure: 66 shows typical curves from one test at 270 A_{rms} inductor current, circulated power of 120 kW, with the inductor current presenting a sinusoidal current behavior with a THD of 10 %, the DC link voltage presenting a ripple smaller than 10 % as previewed in the design phase and all curves in agreement to the expected behavior. A typical curve of the thermocouples output voltages is shown in Figure: 67, with an initial transient behavior caused by the chiller temperature stabilization and a constant output voltage (or temperature) after about 15 min of test duration. Such stabilization is essential to perform accurate measurements at a steady state. The mismatch between outlet temperatures is expected since the operation of the single-phase back-to-back converter is not symmetrical [4].

Table 17: Converter test parameters

	3.3 kV/450 A Si IGBT converter	6.5 kV/300A Si IGBT converter
DC link voltage (V)	1.5 and 1.8 kV	3 and 3.6 kV
Switching frequency (f_s)	500 – 1250 Hz	500 Hz
Current range (I_L)	0 – 300 A_{rms}	0 – 210 A_{rms}
Circulated power (P_{cir})	0 – 153 kW	0 – 226 kW
Modul. factor (both legs) (M)	0.9	0.9
Fundamental frequency (f)	50 Hz	50 Hz
Gate resistance (Ω)	1.5	7.5

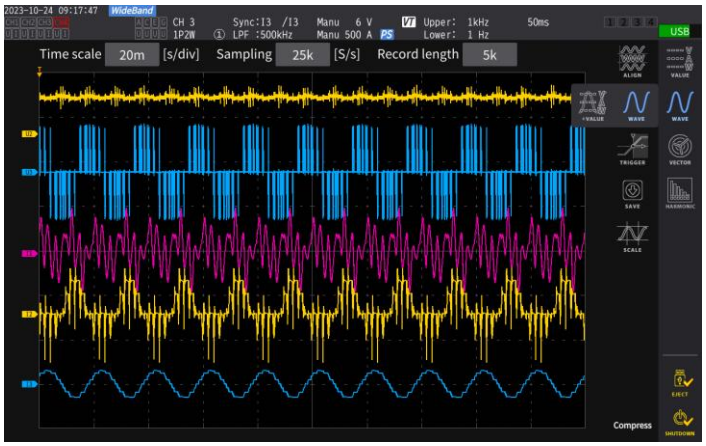


Figure 65: Back-to-back single-phase converter curves during steady state-run test. V: 1.5 kV, I_L: 270 A_{rms}, fs: 500 Hz, f: 50 Hz. U2: DC link voltage (V), U3: Inductor voltage (V_L), I1: Input current (I_{loss}), I2: Circulated current (I_{cir}), and I3: Inductor current (I_L).

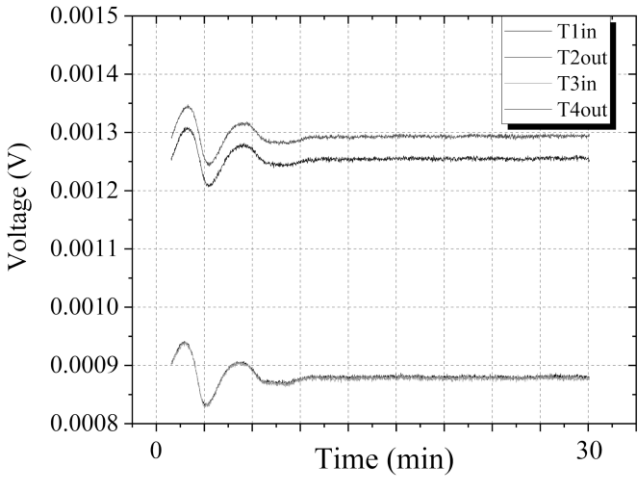


Figure 66: Thermocouples output voltage in a 30 min run test. Initially, a transient state occurs mainly due to the chiller temperature stabilization. After ~ 15 min, the system presents a stable temperature. This test was performed at V: 1.8 kV, I_L: 233 A_{rms}, fs: 1250 Hz, f: 50 Hz with 3.3 kV Si IGBTs.

Figure 68 A, B, and C show the semiconductor power loss characterization from the 3.3 kV Si IGBT-based converter for four switching frequencies in a current load range of up to 300 A_{rms}, the 3.3 kV SiC MOSFET-based converter (R_G: 24 Ω) at 1500 Hz in a current load range of up to 300 A_{rms}, and the 6.5 kV Si IGBT-based converter at 500 Hz and two DC link voltages in a current load range of up to 210 A_{rms}, respectively. The electrical and thermal characterization methods show similar power losses, proving the equivalence of the methods and the high accuracy of the designed testbed setup.

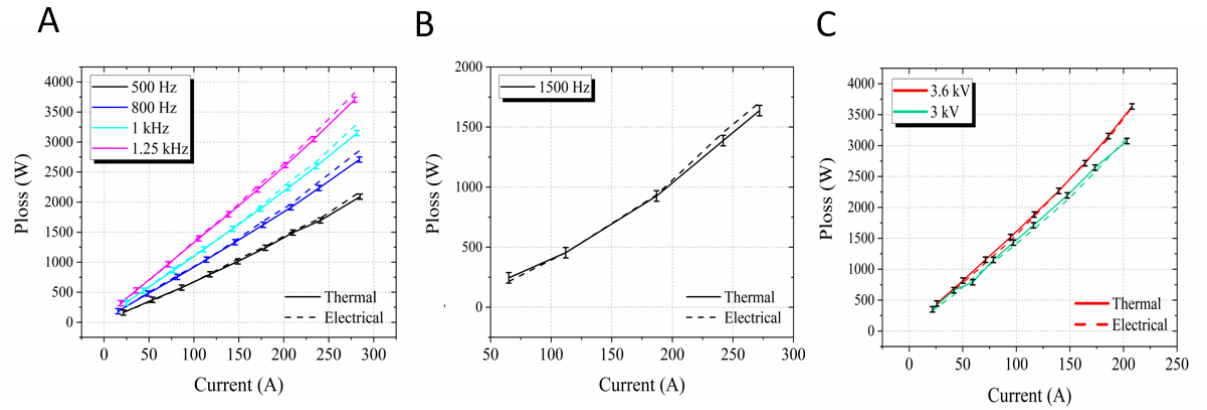


Figure 67: Semiconductor losses from the B2B 3.3 kV Si-based single-phase converter during steady state-run test for different currents. The test conditions are: V: 1.8 kV, I_L: 0 – 300 A_{rms}, fs: 500, 800, 1 kHz, 1250 Hz, f: 50 Hz, M: 0.9, B. Semiconductor losses from the B2B 3.3 kV SiC-based single-phase converter (R_G: 24 Ω) during steady state-run test for different currents. The test conditions are: V: 1.5 kV, I_L: 0 – 300 A_{rms}, fs: 1500 Hz, f: 50 Hz, M: 0.9, C. Semiconductor losses from the B2B 6.5 kV Si-based single-phase converter during steady state-run test for different currents. The test conditions are: V: 3.6 kV and 3 kV, I_L: 0 – 210 A_{rms}, fs: 500 Hz, f: 50 Hz, M: 0.9.

A comparison between the 3.3 kV Si and SiC-based power converter systems is presented in Figure: 69. The SiC technology presents significantly lower power losses, reaching a maximum value of around 1500 W at a high switching frequency of 3000 Hz. On the other hand, the Si IGBT technology presented up to 46% (~ 2200 W) higher power loss values than the SiC system operating at a six times lower switching frequency of 500 Hz. Another characteristic is the switching frequency's strong influence on the Si technology's power losses, with almost doubling the losses at 300 A_{rms} from 500 to 1250 Hz switching frequency variation. On the other hand, the SiC technology presented a less significant increase in the losses (~ 800 up to 1300 W) at 280 A_{rms} with a larger delta switching frequency variation from 500 up to 3000 Hz. Such behavior was expected from the switching losses characterization, where SiC technology presents an optimized design for low switching losses. These comparisons were performed with the Si IGBT system operating at a slightly higher DC Link voltage of 1.8 kV compared to the 1.5 kV of the SiC system. Consequently, the Si IGBT-based system would have slightly lower losses at a reduced DC link voltage of 1.5 kV. As will be shown later, such a slight difference in the DC link voltage influences a reduction in the converter losses smaller than 10 %.

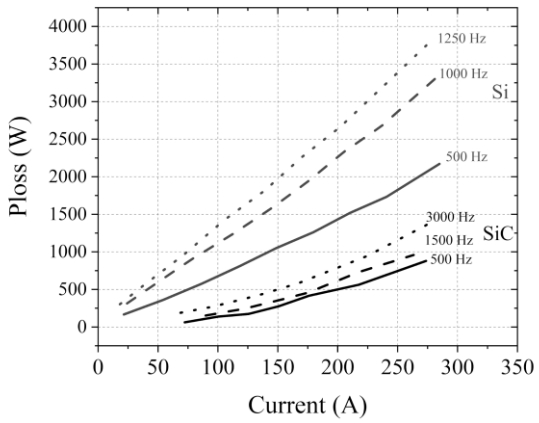


Figure 68: Semiconductor converter losses comparison between Si 3.3 kV Silicon-based single-phase converter operating at V: 1.8 kV, IL: 0 – 300 Arms, fs: 500, 800, 1 kHz, 1250 Hz, f: 50 Hz, M: 0.9 and 3.3 kV SiC-based single-phase converter (RG: 2.4 Ω) operating at V: 1.5 kV,IL: 0 – 300 Arms, fs: 500, 1500, 3000 Hz, f: 50 Hz, M: 0.9.

Finally, the B2B converter efficiency was evaluated and demonstrated in Figure: 70A, 70B and 70C for the 3.3 kV Si IGBT, 3.3 kV SiC and 6.5 kV Si IGBT-based converters, respectively. In the case of the 3.3 Si IGBT-based converter, a peak efficiency of 98.7 % is obtained for a 500 Hz switching frequency. With the switching frequency increase, the efficiency values have been reduced, reaching values lower than 97.5 % at 1250 Hz. Furthermore, we can also observe a flat efficiency curve shape followed by a decay at around 50 Arms, mainly related to the proportionally high conduction losses due to the knee shape in the forward curve. Figure: 70B shows the 3.3 kV SiC-based converter efficiency. The first characteristic observed is the efficiency increase as the current decreases, reaching a peak of 99.8 % at ~ 75 Arms for a 500 Hz switching frequency. This characteristic is expected due to the described unipolar behaviour of SiC that presents excellent low on-state losses at sub-load conditions (due to the

low junction temperature and linear curve behavior) together with low switching losses, outperforming Si IGBT by a large margin in this region (in a range of 1 up to 1.5% efficiency improvement depending on the switching frequency). Thus, SiC is advantageous in mission profiles dominated by sub-load conditions. The efficiency reduction at higher current loads is also observed mainly due to the higher junction temperatures that degrade the on-state resistance. The switching frequency influence on the efficiency is less significant than for the case of the Si IGBT converter, as expected from the previous semiconductor loss analysis from Figure: 69. An average efficiency reduction of around 0.5 % by increasing the switching frequency from 500 up to 3 kHz is observed in the SiC case compared to an average efficiency reduction of around 1.2 % by increasing the switching frequency from 500 up to only 1.25 kHz for the Si case. This characteristic shows the advantage of SiC devices in high-frequency power converters. Finally, the gate resistance increase promotes an almost constant efficiency reduction of about 0.5 % through the investigated current range at a switching frequency of 1.5 kHz for the SiC converter.

The 6.5 kV Si IGBT-based converter behaves similarly to the 3.3 kV case, with an efficiency lower than 98.5 % at a 3 kV DC link and 500 Hz switching frequency. The lower efficiency of higher voltage-rated device converters is mainly related to the intrinsic higher conduction and switching losses.

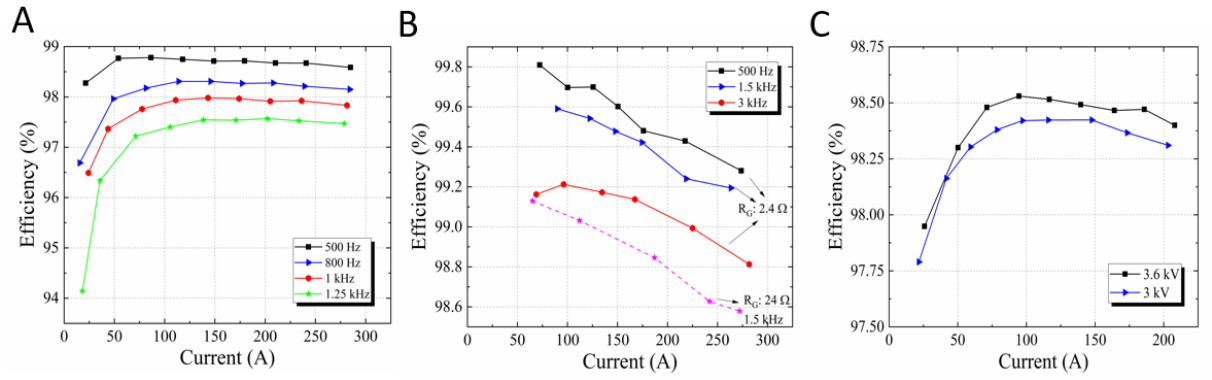


Figure 69: 3.3 kV Si IGBT-based converter efficiency during steady state-run test for different currents. The test conditions are: V: 1.8 kV, I_L: 0 – 300 A_{rms}, fs: 500, 800, 1000, 1250 Hz, f: 50 Hz, M: 0.9, B. 3.3 kV SiC MOSFET-based converter efficiency during steady state-run test for different currents. The test conditions are: V: 1.5 kV, I_L: 0 – 300 A_{rms}, fs: 500, 1500, 3000 Hz, f: 50 Hz, M: 0.9; R_G: 2.4 Ω and V: 1.5 kV, I_L: 0 – 300 A_{rms}, fs: 1500Hz, f: 50 Hz, M: 0.9, R_G: 24 Ω, C. 6.5 kV Si IGBT-based converter efficiency during steady state-run test for different currents. The test conditions are: V: 3.6 kV and 3 kV, I_L: 0 – 210 A_{rms}, fs: 500 Hz, f: 50 Hz, M: 0.9.

4.3 Electro Thermal power converter model

An electro thermal simulation model was developed to accurately perform system simulations and predict the performance of railway traction inverters. A state-of-the-art approach implements a behavioral model based on experimental forward and switching loss curves and power modules' thermal impedance characteristics. Figure: 71 shows the model structure developed in software PLECs. Every simulation step receives the device voltage, current, and junction temperature as input, calculated from the

previous step based on the Kirchhoff circuital laws and the thermal model. The received inputs and the power module's electrical parameters can be used to calculate the device's total losses (conduction + switching losses). The power module's electrical parameters (static and switching loss curves) are obtained from the experimental characterization or the device datasheet. Such parameters should be given at 25 and 125 ºC to allow the interpolation of data to obtain the parameters in the whole operational temperature range. The calculated power losses are the input of the thermal model simulation block. This model is constructed on the association of thermal resistances and capacitances obtained from the device datasheets. The output of this thermal model generates the new junction temperatures that will be used in the next simulation step until the simulation reaches a steady state.

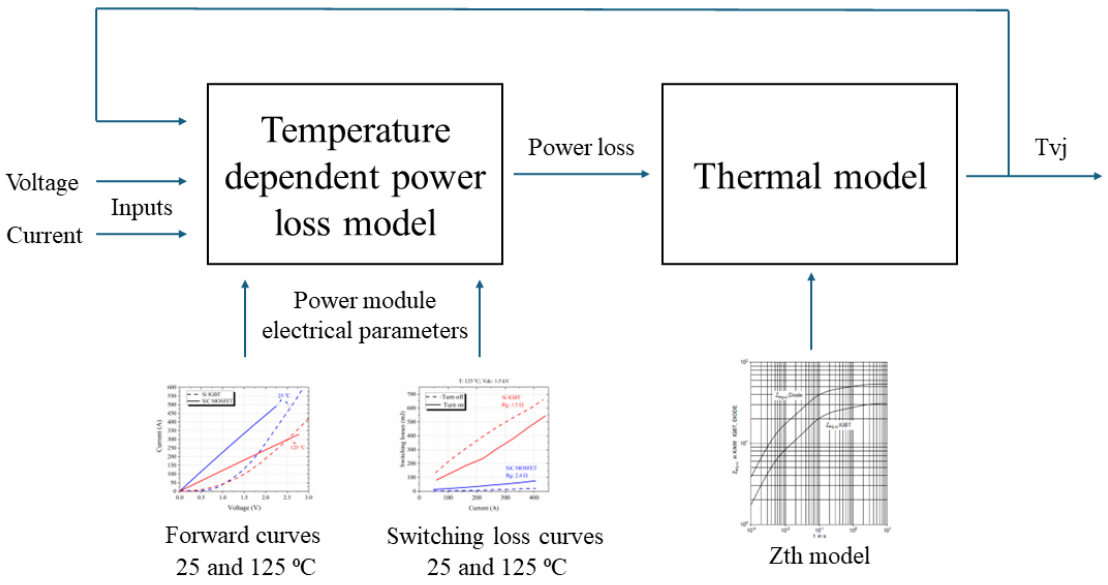


Figure 70: Simulation model structure.

Figure 72 shows the thermal impedance model for the Si and SiC half-bridge power modules. The junction-to-case impedance (Zthj-c) is modelled with the datasheet Foster model. The device and cold plate datasheets provide the case-to-coldplate (considering 1 W/mK grease) and cold plate thermal resistances (Rth), respectively. The used parameters are indicated in Table 18. The case-to-cold plate and cold plate thermal resistances are subjected to a more significant variation due to experimental mounting conditions and thermal paste conductivity and required a slight parameter tuning. It is important to emphasize here that in the selected thermal model, the thermal coupling between the devices happens at the cold plate modelled as an isothermal connection point. Furthermore, the SiC module presents only two devices since no antiparallel diode is present due to the power MOSFET's bidirectional property.

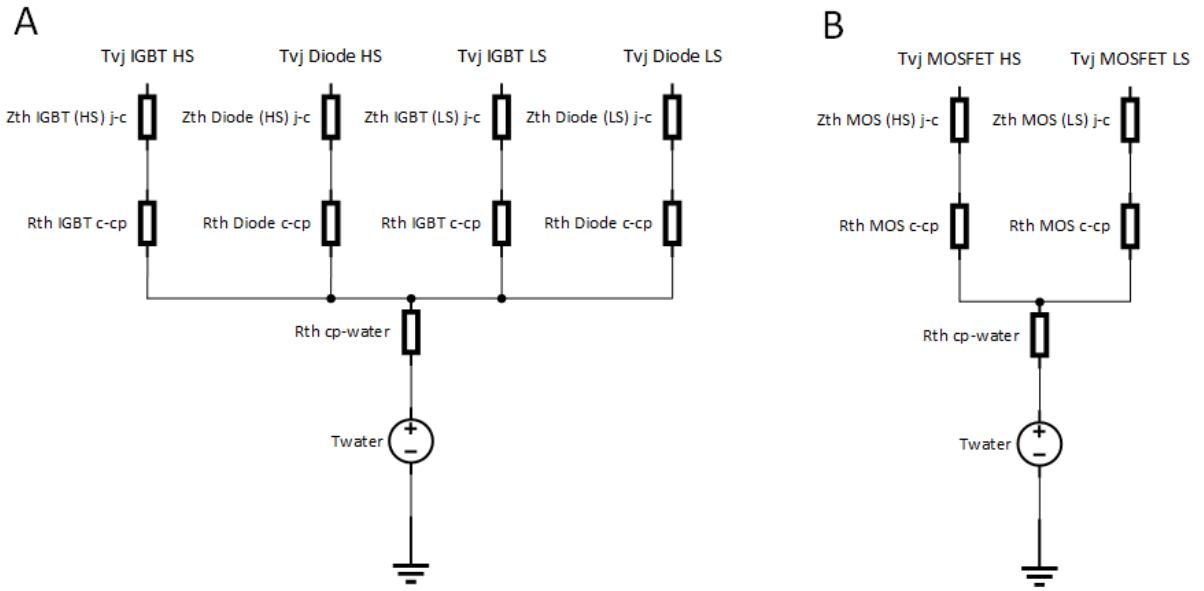


Figure 71: A Thermal impedance model of the Si IGBT half-bridge module on top of the coldplate, B. Thermal impedance model of the SiC MOSFET half-bridge module on top of the coldplate. Abbreviations: Zth: thermal impedance, Rth: thermal resistance, HS: high side, LS: low side, j-c: junction to case, c-cp: case to coldplate, cp-water: coldplate to water, Tvj: junction temperature, Twater: water temperature.

Table 18: Implemented thermal resistance values in simulation

	Si IGBT 3.3 kV/450 A	SiC MOSFET 3.3 kV/500 A
Equivalent $R_{th\ junction\ to\ case}$	IGBT: 31 K/kW Diode: 54 K/kW	46.3 K/kW
$R_{th\ case\text{-}coldplate}$	IGBT: 30 K/kW Diode: 35 K/kW	40 K/kW
$R_{th\ coldplate\text{-}water}$	15 K/kW	10 K/kW
$R_{th\ case\text{-}coldplate}$	IGBT: 30 K/kW Diode: 35 K/kW	40 K/kW

In order to validate the proposed simulation model, each experimental point from the B2B converter was simulated and compared to the experimental results. Figure: 73 compares simulation and experimental data in terms of power losses. The simulation followed the expected behavior for all tested cases with a maximum error from the experimental losses of 200 W for the 3.3 kV Si IGBT-based converter case. For the SiC case, the maximum deviation was 100 W, and for the 6.5 Si IGBT case, it was always smaller than 60 W. It is clear from the curves that the error is mainly systematic through the current range for most cases, with an exception for the 6.5 kV case where the match is close to optimal. The simulation always presents smaller values than the experimental values. Such systematic error provides a predictable simulation behavior for all cases, generating an average error when comparing Si and SiC technologies in the range of about 100 W. The accuracy achieved is excellent for comparison purposes between Si and SiC technologies as the expected power loss differences between both technologies (based on experimental data) is around 300 W at low current (50 Arms) and more than 1000 W at high currents (reaching delta values close to 3000 W depending on the converter operation conditions). It is also essential to remember that the most critical region is at currents higher than 100 A, where the converter operates most of the time, and higher losses are obtained. At regions close to 0 A, the losses are much smaller, and the accuracy (experimental or numerical) is naturally reduced due to the very small values involved.

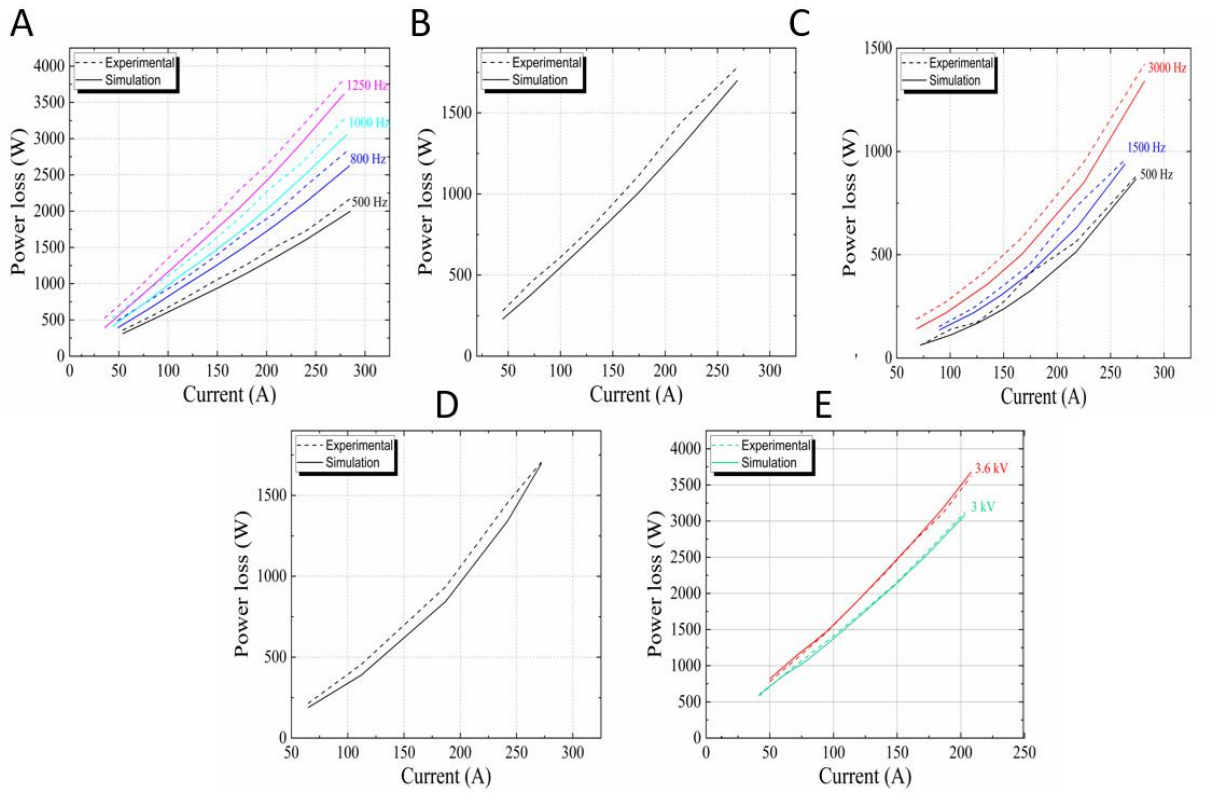


Figure 72: A. 3.3 kV Si IGBT-based converter losses comparison between simulation and experimental data. The test conditions are: V: 1.8 kV, IL: 0 – 300 Arms, fs: 500, 800, 1000, 1250 Hz, f: 50 Hz, M: 0.9, B. 3.3 kV Si IGBT-based converter losses comparison between simulation and experimental data. The test conditions are: V: 1.5 kV,

IL: 0 – 300 Arms, fs: 500 Hz, f: 50 Hz, M: 0.9, C. 3.3 kV SiC MOSFET-based converter (RG: 2.4 Ω) losses comparison between simulation and experimental data. The test conditions are: V: 1.5 kV, IL: 0 – 300 Arms, fs: 500, 1500, 3000 Hz, f: 50 Hz, M: 0.9, D. 3.3 kV SiC MOSFET-based converter (RG: 24 Ω) losses comparison between simulation and experimental data. The test conditions are: V: 1.5 kV, IL: 0 – 300 Arms, fs: 1500 Hz, f: 50 Hz, M: 0.9, E. 6.5 kV Si IGBT-based converter losses comparison between simulation and experimental data. The test conditions are: V: 3 and 3.6 kV, IL: 0 – 210 Arms, fs: 500 Hz, f: 50 Hz, M: 0.9.

Another validation test compared the simulated total harmonic distortion (THD) and circulated power in the B2B topology with the experimental values. Figure: 74A shows the THD comparison for two distinct switching frequencies, with an excellent match between simulation and experimental for higher currents. The improvement of the THD at higher switching frequencies is expected due to improved voltage harmonic content. The THD increase at lower currents is caused by the 10 us dead time implemented, which degrades the sine wave current curve close to the 0 A region. Such behavior is naturally more pronounced at higher switching frequencies, as the simulation and experimental data show. Figure: 74B shows an excellent match between experimental and simulated circulated power for both switching frequencies, demonstrating the high accuracy of the simulation model.

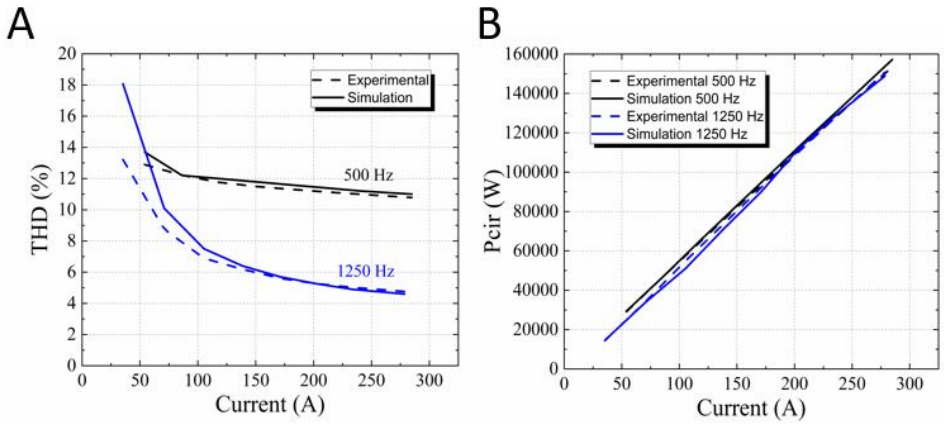


Figure 73: A. THD comparison between experimental data and simulation for the 3.3 kV Si IGBT converter at 500 and 1250 Hz, B. Circulated power comparison between experimental data and simulation for the 3.3 kV Si IGBT converter at 500 and 1250 Hz

This chapter focused on the experimental evaluation of the Si and SiC-based power converter in a B2B configuration. An initial validation of the proposed thermal and electrical power loss characterization methods was provided, showing the equivalence between the methods. Then, the power losses between Si and SiC-based converters were compared, demonstrating the SiC advantage in mission profiles dominated by sub-load conditions, with efficiencies reaching up to 1.5 % higher values than Si IGBT-based converters. Furthermore, the switching frequency influence was also investigated, with SiC converters showing a significant higher efficiency than Si IGBT converters at higher switching frequencies. Such characteristics prove the advantage of SiC devices in high-frequency power converters. Finally, an electro thermal model is developed to simulate power converter systems based on the power

module technologies investigated in this project. Extensive experimental results, performed under distinct operating conditions (distinct DC link voltages, switching frequencies, current loads, gate resistances), were used to validate the simulation results, proving that the developed models have enough accuracy for system comparisons between MV Si and SiC technologies.

4.3.1. Simulations of Si and SiC based railway traction inverters

This chapter focuses on the performance evaluation of Si and SiC-based power inverter topologies with previously validated electrothermal simulations. An initial overview of the main traction topologies used in trains is discussed followed by simulation considerations. The efficiency of selected topology configurations was obtained over the whole current range. Then, the loadability characteristics of these topologies were assessed to provide the maximum output power based on the maximum junction temperature criteria. Finally, drive cycle modelling followed by energy loss evaluation and financial analysis of these topologies during the inverter lifetime is provided.

4.3.2. Railway traction systems

The rail voltages can vary depending on the country, ranging from 750 Vdc to 25 kVac. However, even high AC voltages are reduced using onboard transformers and rectified to a DC link voltage of 750 V up to 3 kV for the traction inverter. It is also common the cases of DC catenaries at 3 kV, not requiring transformers and rectifier circuit. When the rectification is required, it can have unidirectional or bidirectional front-end topology depending on whether regenerative energy is desired to flow back to the catenary system. Additional DC-DC converters may be implemented to add functionalities, like onboard batteries for operation in non-electrified routes. In this report, we focused on traction inverters used in metros, trains and locomotives with a typical DC link voltage of 1500 or 3000 V, which are common cases encountered in applications. The industry standard choice for a 1.5 kV DC link voltage is a three-phase, two-level (2L) inverter topology, as demonstrated in Figure: 75, with 3.3 kV power switches [5]. In the case of the 3 kV DC link, the same topology is used with 6.5 kV switches, and it is also an option to implement 3-level (3L) topologies like the traditional Active Neutral Point Clamped (ANPC) topology [6, 7] with 3.3 kV switches (Figure: 76). The nominal power of these inverters is generally in the range of 150 kW – 1.4 MW [5], depending on the power module rating and design considerations. Each leg of the 3-phase 2-level topology demonstrated in Figure: 75 is a LinPak power module composed of one power switch on the high side and one on the low side. For the 3-level topology case, the positioning of the LinPak modules is indicated in the blue boxes in Figure: 76.

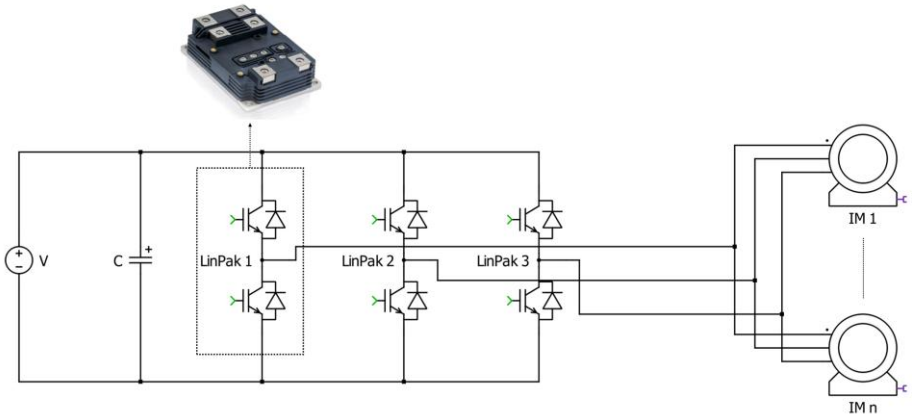


Figure 74: Three-phase two-level inverter topology connected to induction motors in the output. Each Half-bridge leg corresponds to a LinPak power module composed of 2 power switches (high-side switch and low-side switch).

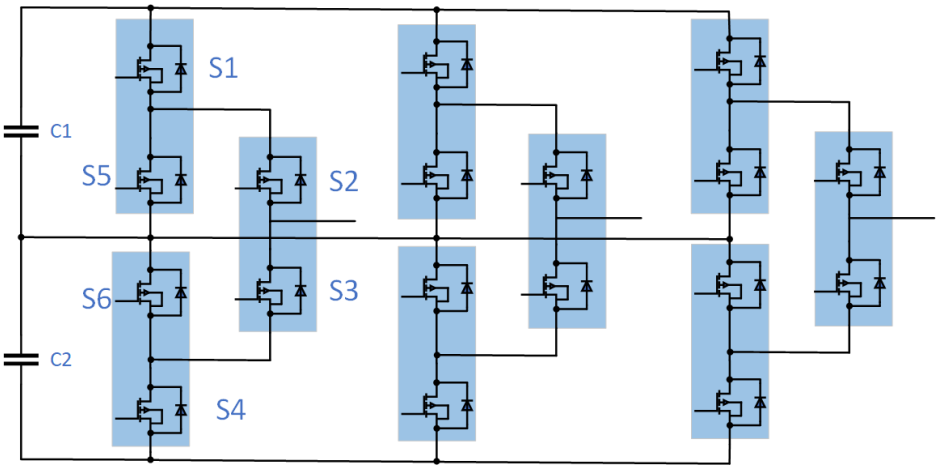


Figure 75: ANPC topology, with the positioning of the Half-bridge power modules indicated inside the blue boxes. These boxes also indicate the positioning of the cold plates and thermal coupling between switches.

Regarding 1.5 kV DC link voltage, 2-level topologies based on 3.3 kV Si and SiC LinPak power modules have been compared. In the case of 3 kV DC link railway systems, a 2-level topology with 6.5 kV Si IGBT LinPak power modules is compared with a 3-level ANPC topology built with 3.3 kV SiC power modules. The comparisons are always performed for the configurations from the same DC Link voltage class. Table 19 and Table 20 shows the simulated topology configurations and the devices used for the 1.5 kV and 3 kV DC link traction systems, respectively. The 2.4 and 24 Ω gate resistance cases were investigated to compare the performance of railway inverters operating with high (~ 38 V/ns) and low speed switching (~7 V/ns). Such cases may influence the requirement of an additional dv/dt filter to

protect the motor insulation. For the 3 kV DC link case, the 3.3 kV switches had their parameters down-rated to 300 A to match the 6.5 kV Si IGBT switch current rating. As a result, a fair comparison between same current rating devices can be performed.

Table 19: Simulated topology configurations for the 1.5 kV DC link traction system

Topology	Device	Gate resistance (Ω)
2 Level	Si IGBT 3.3 kV/450A	1.5
2 Level	SiC MOSFET 3.3 kV/500A	2.4
2 Level	SiC MOSFET 3.3 kV/500A	24
2 Level	SiC MOSFET 3.3 kV/500A	2.4
2 Level	SiC MOSFET 3.3 kV/500A	24

Table 20: Simulated topology configurations for the 3 kV DC link traction system

Topology	Device	Gate resistance (Ω)
2 Level	Si IGBT 6.5 kV/300A	7.5
3 Level ANPC	SiC MOSFET 3.3 kV/300A	2.4*
3 Level ANPC	SiC MOSFET 3.3 kV/300A	24*
3 Level ANPC	SiC MOSFET 3.3 kV/300A	2.4*
3 Level ANPC	SiC MOSFET 3.3 kV/300A	24*

*The indicated gate resistance is from the characterized power module (3.3 kV/500 A SiC MOSFET) that had the current down rated for the 3L topology simulation. In practice, lower current rated devices use higher gate resistances.

The devices were down rated where the thermal resistance, and on-state resistance are linearly scaled according to Equations 4, and 5. For the SiC switching losses case, since the switching losses are small and the variation in switching loss versus die size is small (with a change of about 37% of the switching losses when the device current rating changed by 350%) the same switching loss values from the 500 A module were assumed for the 300 A module.

$$R_{DSon,rated} = R_{DSon,nom} \times I_{nom}/I_{rated} \quad (4)$$

$$R_{thjc,rated} = R_{thjc,nom} \times I_{nom}/I_{rated} \quad (5)$$

Regarding the modulation techniques implemented in commercial traction inverters, several modulation strategies may be used, such as Sinusoidal PWM (SPWM), Space vector modulation (SVM), and Selective harmonic elimination. This work implemented the Sinusoidal PWM (SPWM) for the 2-level topology. In the case of the 3-level ANPC, several other variations based on the described options can be performed due to the redundant states that can be used to balance the power loss between the switches. Here, it was implemented a simple SPWM technique with the commutations cells formed by S1, S3, S5 and S2, S4, and S6 (see Figure:76) alternating between line and switching frequency during negative a half cycles and a single neutral state in order to reduce conduction losses in devices S2, S3, S5 and S6. Such an option presents good results for SiC devices and easy implementation with similar signal generation to an NPC topology.

4.3.3.Railway inverter efficiency

This section evaluates the efficiency of 1.5 and 3 kV DC link-based traction inverters (2-level and 3-level ANPC topologies). The load current was an ideal sine wave current source. The simulation parameters are shown in Table 21. The load power factor (PF) was modelled based on a typical MV motor power factor profile [8]. The full load case (100%) was set for each converter configuration when the junction temperature reached the maximum value of 125 ºC. The selected switching frequencies were based on the following considerations:

- 500 Hz: Typical switching frequency of commercial Si IGBT-based railway traction inverter

- 1500 Hz: With the implementation of SiC devices, due to the high-efficiency operation at higher switching frequencies, an increase in the switching frequency brings advantages to motor efficiency by reducing motor harmonic losses [9]. Additionally, higher frequency operation can reduce the motor noise [10]. The optimum switching frequency determination requires a combined characterization approach of the inverter with the motor [9]. Based on previous railway traction works with 3.3 kV SiC devices [11, 10], an optimum switching frequency may be in the range of 800 – 2000 Hz. Based on these considerations, a switching frequency of 1500 Hz was selected.

Table 21: Inverter efficiency simulation parameters

DC Link voltage	1.5 / 3 kV
Modulation factor	0.9
Switching frequency	500 / 1500 Hz
Fundamental frequency	50 Hz
Load PF	Typ MV motor [106]
Water temperature	40 ºC

4.3.4.1.5 kV DC link system

Figure 77 shows the simulated efficiencies for the 1.5 kV DC link railway inverters. Here, the focus is on the numerical efficiency values of the different topology configurations. The Si IGBT topology presents the lowest efficiency value with a flat behavior of around 99.2 %. The SiC configurations at 500 Hz and 1500 Hz with low gate resistance and at 500 Hz with high gate resistance present a considerable efficiency gain compared to the Si configuration with similar efficiency values between them. The SiC configuration at 1500 kHz and high gate resistance presents a higher efficiency degradation due to the higher frequency and switching losses. Overall, the SiC topologies with low gate resistances at 500 and 1500 Hz and the one with high gate resistance at 500 Hz are promising candidates for efficiency optimization compared to the Si IGBT inverter.

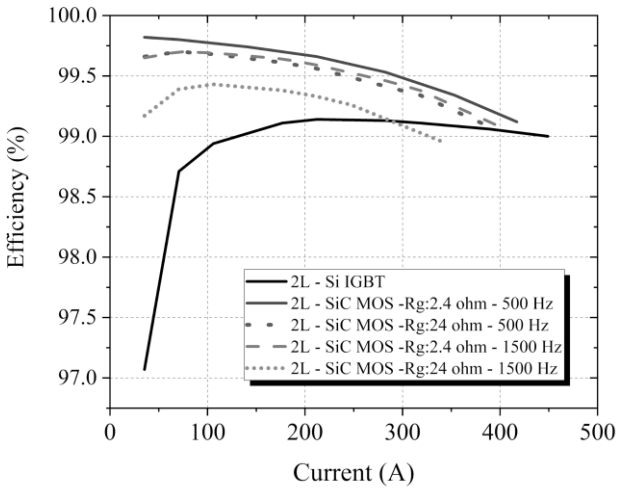


Figure 76: Simulated efficiency curves for 1.5 kV DC link railway inverters.

4.3.5.3 kV DC link system

Figure: 78 shows similar behavior to Figure: 77, with the main difference that the SiC efficiency curves do not cross the 2-level Si IGBT efficiency curve, presenting a flatter behavior. Overall, the SiC topologies with low gate resistances at 500 and 1500 Hz and the one with high gate resistance at 500 Hz are promising for efficiency optimization compared to the 6.5 kV Si IGBT-based inverter.

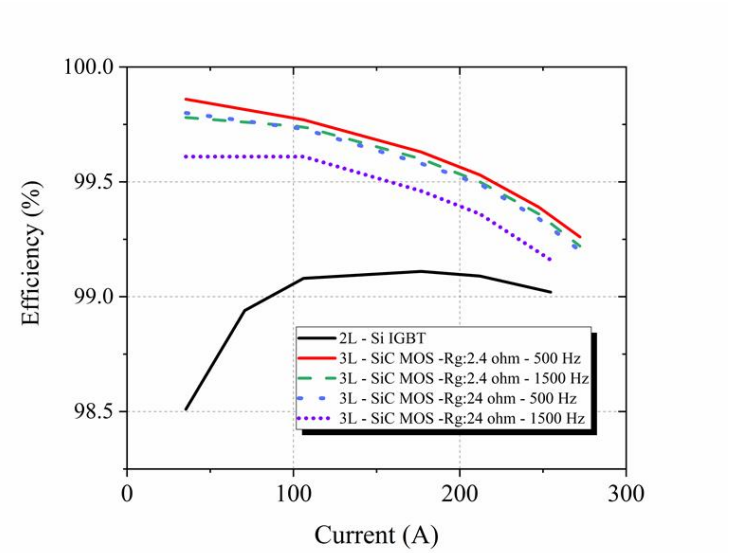


Figure 77: Simulated efficiency curves for 3 kV DC link railway inverters.

4.4 Railway inverter loadability

The loadability analysis evaluates the maximum output power a converter can provide for a certain switching frequency. This assessment is essential to compare the maximum power rating of distinct converter designs and provide essential information to evaluate the converter costs per kWh.

In this section, the simulations were performed considering a maximum junction temperature of 125 ºC, typical of MV power modules. The parameters are similar to the previous section with the following differences:

- Modulation factor of 1 for the 2 and 3-level topologies.
- Power factor of 1

The above conditions may represent a worst-case scenario for the 3-level ANPC topology and were also considered for the 2-level case.

4.5 1.5 kV DC Link System

The loadability analysis from Figure: 79 shows that the SiC at low gate resistances can operate up to 5000 Hz, not aggressively deteriorating the converter power rating. A reduction in the maximum current of about 15 % is observed when operating at 5000 Hz and only about 5 % reduction when operating at 1500 Hz. This characteristic is advantageous for designs where high switching frequency operation can considerably improve power converter density, like grid-tied converters with bulky output sine filters. Additionally, the analysis shows that an increase from 500 to 1500 Hz for railway applications slightly penalizes the converter power rating. In the SiC option with high gate resistance, a reduction of around 40 % when operating at 5000 Hz and around 12 % when operating at 1500 Hz is assessed. The Si IGBT presents a very high degradation of the converter rating with switching frequencies higher than 500 Hz

due to the high Si IGBT switching losses. A reduction of about 36 % is observed with an operation of only 1500 Hz. Such a limitation factor is why these converters operate at low switching frequencies. Thus, the converter cost per kWh is not aggressively increased. Interestingly, at 500 Hz, the Si IGBT presents a slightly better current capability than the SiC at low gate resistance, presenting a power extension of around 10 % over the SiC (low gate resistance) topology. This characteristic comes from the higher on-state losses of the SiC device at high currents and high temperatures.

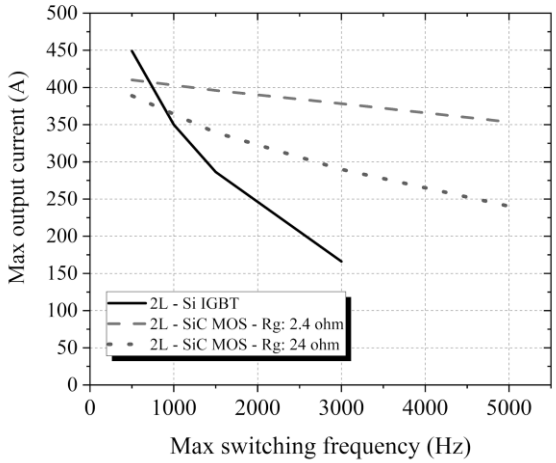


Figure 78: Simulated loadability curves for 1.5 kV DC link railway inverters.

4.5.1.3 kV DC Link System

Figure: 80 shows the 3-level SiC topology at low gate resistance with an almost constant current output capability in the switching frequency range up to 3000 Hz. The same topology with a higher gate resistance shows the current reduction with the increased switching frequency. A current reduction of about 15 % from the 500 Hz operation point is observed at the frequency of 1500 Hz. At 500 Hz, it presents the same current capability as the 3-level SiC topology with low gate resistance. Finally, the 2-level Si IGBT topology presents a very high degradation of the converter rating for frequencies higher than 500 Hz, reaching a current reduction of about 55 % from the 500 Hz point at 1500 Hz. In a nutshell, the 3-level SiC topology with low gate resistance can have an operation point up to 3 kHz, maintaining the converter rating. Such characteristics are good for improving motor losses due to better voltage harmonic content and keeping the converter cost per kWh. A switching frequency of 1500 Hz may be the best choice since the efficiency is still high, as shown in Figure: 78, not negatively affecting the heatsink volume required, energy loss costs and carbon footprint. The 3-level topology with high gate resistance operating at 500 Hz presents the same current capability as the 3-level SiC with low gate resistance at 1500 Hz. The efficiency curve behavior is also quite similar between both combinations. A possible advantage of the 3-level with high gate resistance would be to avoid using an output dv/dt filter depending on the motor connections. The lower voltage harmonic quality due to the lower switching frequency is a disadvantage, which may increase motor losses.

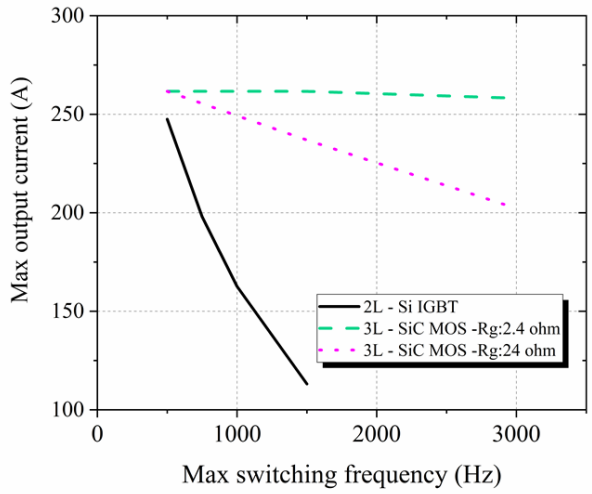


Figure 79: Simulated loadability curves for 3 kV DC link railway inverters.

5 Life cycle energy assessment of traction inverters

5.1.1. Power loss investigation in a drive cycle

In order to make a performance assessment in a realistic operation environment, the energy loss evaluation of the proposed topologies was performed under a realistic drive cycle from a real train for suburban operations in central Europe, as shown in Figure: 81A. The route has a distance of 11 km completed in 384 s (6.4 min). The maximum speed during cruising is 38.89 m/s (140 km/h), and the maximum accelerations are 0.66 m/s2 and 1 m/s2 at the acceleration and brake phases (see Figure: 81B), respectively. It has been assumed that this drive cycle was performed in a flat route without curves. The validated semiconductor electro thermal parameters were used in the simulation. Based on what was found in the previous sections regarding efficiency and loadability, the analyzed topology configurations are shown in Table 23 and Table 24. From all initially proposed topologies, it was ignored the 2-level 3.3 kV SiC configuration with low gate resistance at 500 Hz due to the similar efficiency and current capability compared to the 1500 Hz configuration that can bring further advantages to the motor losses. The 2-level 3.3 kV SiC at high gate resistance and 1500 Hz switching frequency was also discarded due to the significant efficiency and loading capability deterioration observed at this switching frequency.

Regarding the 3kV DC link railway systems, the same strategy was applied, discarding the 3.3 kV 3-level at low gate resistance and 500 Hz as well as the 3.3 kV 3-level at high gate resistance and 1500 Hz (Table 20). MV induction motors formed the load. In the case of the 1.5 kV DC link railway systems, 4 medium voltage induction motors compose the load. This is a typical situation in trains where up to 4 motors can be connected to the same inverter output. The power converters analyzed have a nominal power rating of around 500-700 kW, considering the thermal criteria. The four motors have a nominal

power of 640 kW (each 160 kW) and a nominal voltage of 1287 V. This value is within the range of a typically adopted motor voltage for converters with a DC link of 1500-1800 V. The electrical parameters of the motor used in the simulation are detailed in [12] and indicated in Table 22. For the case of 3 kV DC link railway systems, the same motor parameters were slightly adapted to reach a nominal power of 560 kW, and a nominal voltage of 2400 V, a typical voltage rating used in railway systems at 3 kV DC link [5]. For this case, since the motor power rating is 560 kW and the converters have power ratings in the range of 700-900 kW, two motors were chosen as the load.

Table 22: Motor parameters

	1.2 kV Motor
Rated frequency (Hz)	84
Pole pairs	4
Rated rms voltage (V)	1287
Nominal power (kW)	160
Nominal speed (rpm)	1250
Stator resistance (Ω)	0.223
Stator leakage inductance (H)	0.000158
Magnetization inductance (H)	0.0438
Rotor resistance (Ω)	0.103
Rotor leakage inductance (H)	0.002076
Sigma	0.07849
Rotor inductance (H)	0.045876

The chosen control strategy is the rotor flux-oriented vector control, one traditional technique for the high-performance control of induction motor drives in railway applications [5]. From the chosen drive cycle, based on the speed and acceleration, train mechanical parameters, and opposing force models, it is possible to calculate the equivalent traction force acting in the train. The motor's electromagnetic torque and shaft speed are calculated with additional mechanical considerations of the gear ratio and wheel radius. Based on the motor electromagnetic torque and speed, as well as the electrical motor parameters from Table 22, the criteria for flux reference generation from [5] was implemented. These considerations together with the electromagnetic torque can be used to calculate the direct (id) and quadrature (iq) motor current components. Then, the direct and quadrature motor voltages were obtained. These motor voltages are used as input for the modulator from the simulator to generate the SPWM signal for the inverter. The load is the proposed motors with the modelled opposing torques acting during the drive cycle simulation. This method presents the advantage of comparing the output simulation variables like motor speed, current components (id and iq), motor electromagnetic torque (Tem), and motor magnetic flux with the calculated theoretical values during the voltage components

generation procedure. Such a comparison can be used to check if the model was set correctly in the simulator. Figure: 82 shows a simulation result of the proposed drive cycle at 5 kHz switching frequencies. The simulated values follow the theoretical values as expected, with an additional ripple variation due to the presence of harmonics in the simulation caused by the switching.

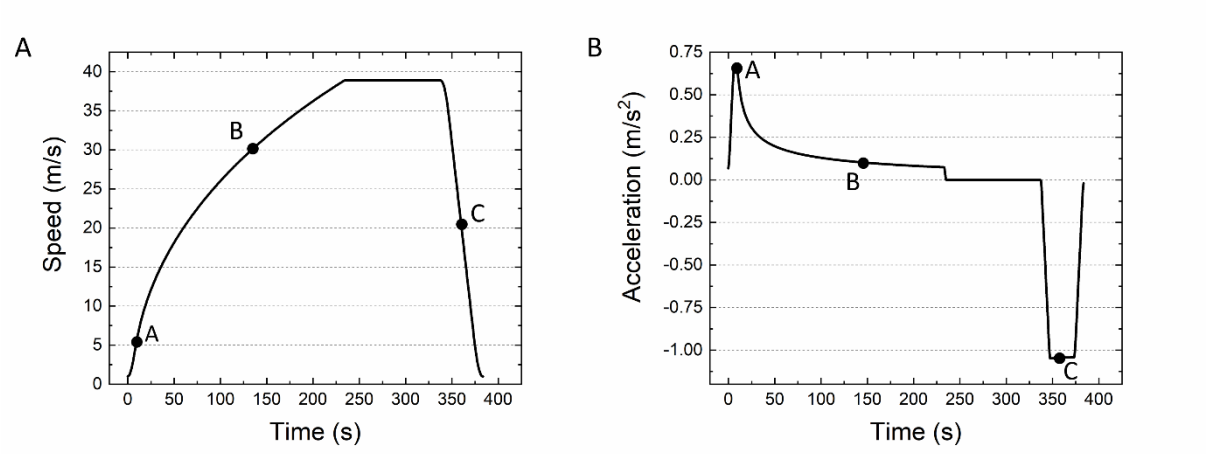


Figure 80: A. Drive cycle from a suburban train route in central Europe, B. Train acceleration during the drive cycle.

Table 23: 1.5 kV DC link railway inverter simulated configurations

Topology	Switch. Frequency (Hz)	Twater (ºC)	Multiplicator
3.3 kV Si/R_G: 1.5 Ω	500	40	1
2 level	500	40	50
	500	70	1
	500	70	50
3.3 kV SiC/R_G: 24 Ω	500	40	1
2 level	500	40	50
3.3 kV SiC/R_G: 2.4 Ω	1500	40	1
2 level	1500	40	50
	1500	70	1
	1500	70	50

Table 24: 3 kV DC link railway inverter simulated configurations

Topology	Switch. Frequency (Hz)	Twater (ºC)	Multiplicator
6.5 kV Si/R_G: 7.5 Ω	500	40	1
2 level	500	40	55
	500	70	1
	500	70	55
3.3 kV SiC/R_G: 24 Ω	500	40	1
3 level ANPC	500	40	55
3.3 kV SiC/R_G: 2.4 Ω	1500	40	1
3 level ANPC	1500	40	55
	1500	70	1
	1500	70	55

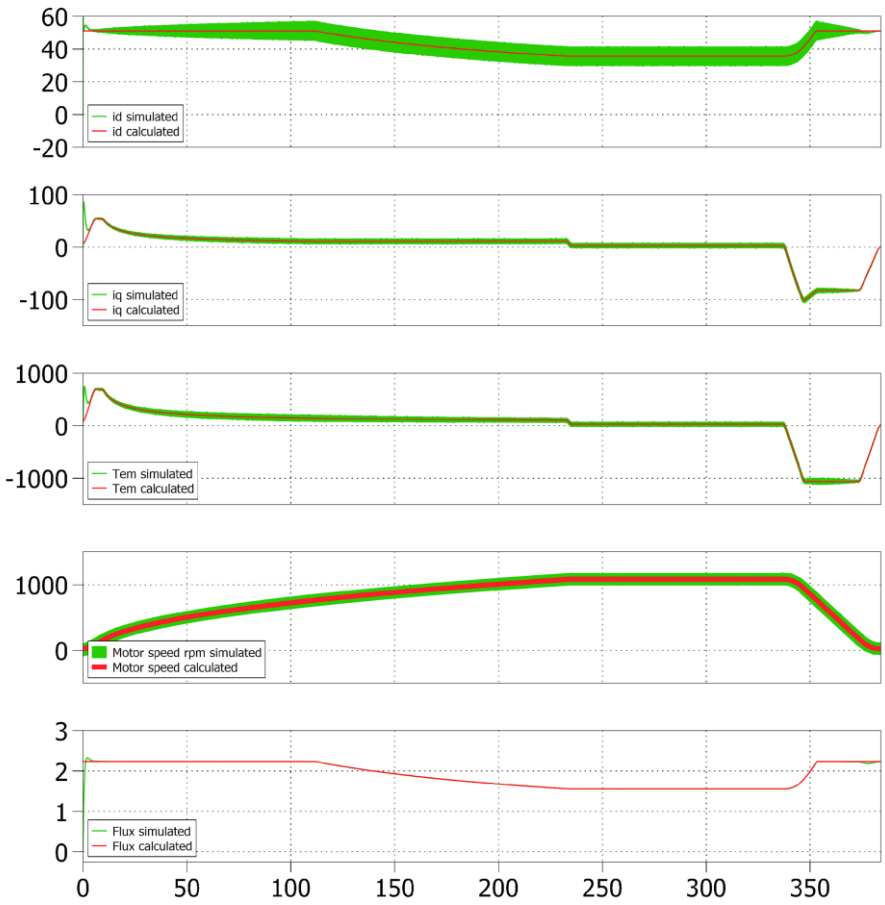


Figure 81: Drive cycle simulation at 5 kHz from a 2-level topology. The graph unities from top to bottom are direct current component - id (A), quadrature current component - iq (A), electromagnetic torque -Tem (N.m), motor speed (rpm), and motor flux (Wb).

The train parameters and modelling are based on [13], considering the most significant force contributions. Equations 6-8 show the parameters for the requested motor force.

$$F = m.a \quad (6)$$

$$Fd = (0.75 + 0.0011664 * v^2) * G \quad (7)$$

$$Ft = F + Fd \quad (8)$$

The requested motor force (Ft [N]) is the sum of the inertial (F [N]) and drag (Fd [N]) forces. The other parameters from Eqs. 6-8 are the train acceleration (a [m/s2]), train weight (G [kN]) and train speed (v [m/s]). The considered coefficients are from modern passenger trains [13]. Some additional suitable parameters are considered, such as the wheel diameter of 0.687 m [14] and a gear ratio of 1 to cover

the vehicle speed range from Figure: 81A, according to the nominal motor parameters. Since we focus on the power module losses, just one power converter must be simulated, reducing computer simulation effort. Several power converters and motors are connected to the train's carriages in a real train, and the traction effort is equally divided under ideal conditions. Thus, the effective train mass (m) of 12 Tons was considered to simplify the simulation and obtain the practical effect on one power converter. This value corresponds to the effective effort distributed to the simulated power converter and not from the whole train. This value was chosen so the maximum power converter current during operation reaches a maximum derated nominal current. Power derating is required to ensure the long-term reliability of power modules and to guarantee a long semiconductor lifetime of 20 – 30 years. The nominal power may be 50 – 80 % of the power converter nominal current, depending on the design considerations (switching frequency, cooling design, expected module lifetime, power module cycling capability). Figure: 83 shows the inverter output current (configuration 2-level) in one output phase for three distinct moments indicated in Figure: 81 (Points A, B, and C). The current waveforms are typical of a sinusoidal pulse width modulation (SPWM) modulation technique with variable modulating frequency in function of the shaft speed. As expected, the switching and output frequency ratio decreases for higher shaft speeds, and the current distortion increases [14]. As one can see, point B presents the highest distortion, followed by C and A. Another characteristic is the high current value during acceleration and brake phases caused by the inertial force component that requires most of the motor traction effort. Point C, with the highest acceleration value of – 1m/s2, presents the highest fundamental rms current of 290 A, followed by points A (~ 205 A) and B (~150 A).

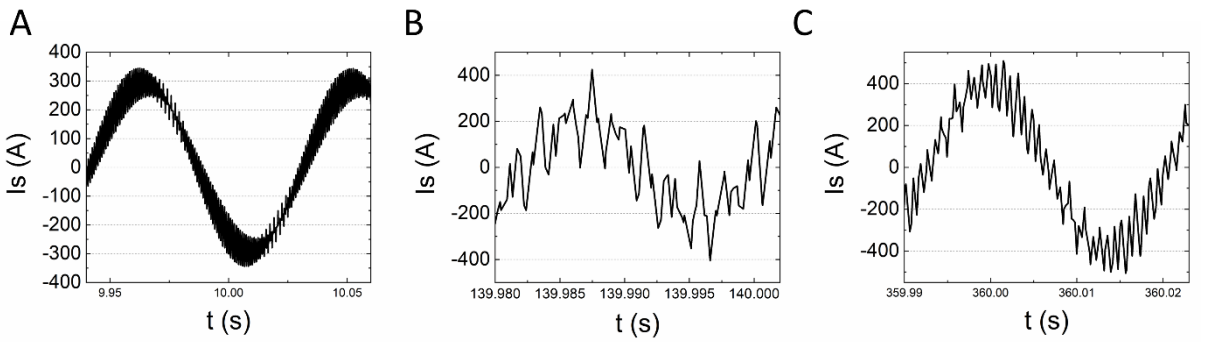


Figure 82: A. One-phase inverter output current at point A from Figure: 81, B. One-phase inverter output current at point B from Figure: 81, C. One-phase inverter output current at point C from Figure: 81.

Another point was to investigate this drive cycle under distinct load conditions to evaluate the SiC at higher junction temperatures and current. Different water temperatures were considered (40 and 70 ºC). Additionally, a multiplication factor in the squared speed term from Equation 7, indicated in Table 23 and Table 24, was artificially set to increase the device currents during cruising. Generally, this region presents the lowest current, with the acceleration and braking presenting the highest currents due to high inertial acceleration. Such a modified case could represent a situation where the train operates at high-speed uphill, requiring more traction power from the inverter.

5.1.2.1.5 kV DC link system

The topology configurations from Table 23 were simulated and the results are indicated in Table 25. Figure: 84 shows the device temperature for three different drive cycle conditions when the water temperature and the multiplicator value are changed. Figure: 84A shows the case when the multiplicator is 1 and water temperature equals 40 ºC. The highest temperature is achieved during the train braking, reaching the highest current. During the cruise phase, the temperature is the lowest since the opposing force is not significant. In Figure: 84B, due to the increase of the multiplicator value to increase the device current during cruising, the device temperature reaches the peak value at this moment. Finally, Figure: 84C shows the case when the water temperature is increased to 70 ºC. Since the multiplicator value is the same as the first case (Figure: 84A), the shape is similar with an offset in the device temperature.

Table 25 shows that the most significant energy loss reduction per phase occur in drive cycles, most often on sub-load conditions and lower temperatures, reaching potential loss reductions of up to 63% from the Si IGBT case for the low gate resistance configuration. Even with the water temperature being increased up to 70 ºC, the loss reduction is still 59%. A more significant reduction occurs when the current increases during the cruising phase (increased multiplication factor). The loss reduction percentage is reduced to around 40% in such a case.

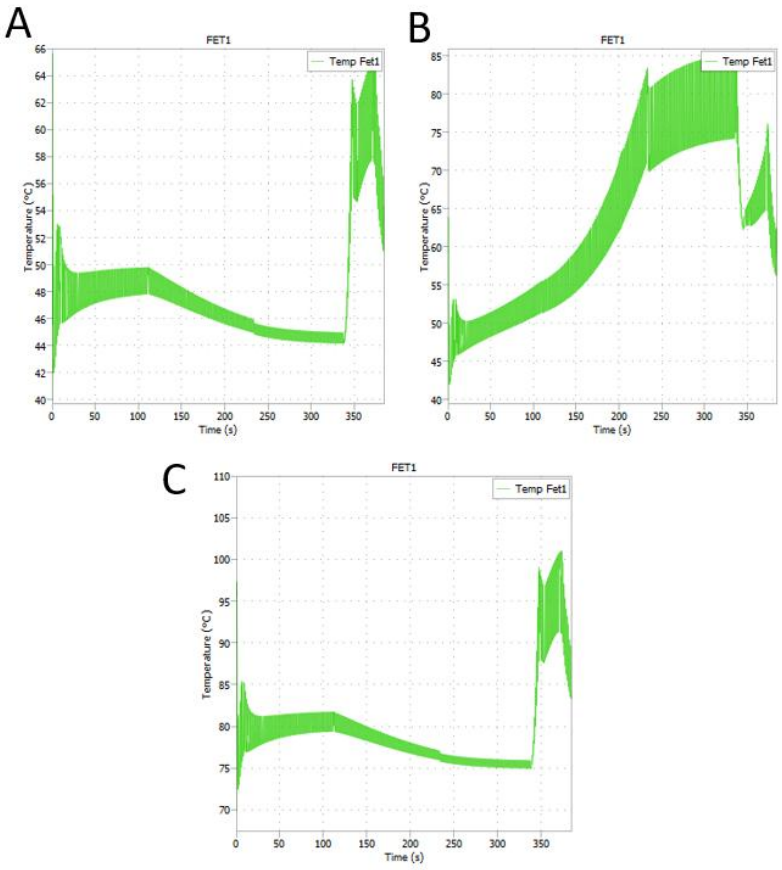


Figure 83: A. MOSFET temperature during drive cycle at T_{water}: 40 ºC, multiplicator: 1, fs: 1500 Hz, RG: 2.4 Ω, B. MOSFET temperature during drive cycle at T_{water}: 40 ºC, multiplicator: 50, fs: 1500 Hz, RG: 2.4 Ω, C. MOSFET temperature during drive cycle at $T_{water:}$ 70 ºC, multiplicator: 1, fs: 1500 Hz, RG: 2.4 Ω.

Table 25: 1.5 kV DC link railway inverters simulated configurations. The drive cycle energy loss per phase is demonstrated for each configuration. Additionally, the saved energy per phase in comparison to the equivalent Si-based topology (same T_{water} and Multiplicator) is shown in absolute values and percentage.

Topology configuration	Switching frequency (Hz)	Twat (ºC)	Multiplicator	E_{loss}/phase (kWh)	Saved energy -compared to Si (kWh)	Saved energy- Si case as reference (%)
3.3 kV SiC R_G: 2.4 Ω	1500	40	1	0.01772	0.03081	63.5
3.3 kV SiC R_G: 2.4 Ω	1500	40	50	0.04827	0.03723	43.5
3.3 kV SiC R_G: 2.4 Ω	1500	70	1	0.02128	0.03069	59
3.3 kV SiC R_G: 2.4 Ω	1500	70	50	0.05856	0.03336	36.3
3.3 kV SiC R_G: 24 Ω	500	40	1	0.02169	0.02684	55.3
3.3 kV SiC R_G: 24 Ω	500	40	50	0.05757	0.02793	32.6
3.3 kV Si R_G: 1.5 Ω	500	40	1	0.04853	-	-
3.3 kV Si R_G: 1.5 Ω	500	40	50	0.08550	-	-
3.3 kV Si R_G: 1.5 Ω	500	70	1	0.05197	-	-
3.3 kV Si R_G: 1.5 Ω	500	70	50	0.09192	-	-

5.1.3. 3 kV DC link system

Table 26 shows the simulation results for the 3 kV DC link-based inverters. The same behavior from the 1.5 kV DC link analysis is observed here, with the most significant variable to reduce the losses being the current increase during the cruising phase (higher multiplicator factor) followed by the temperature increase. The main difference is that the loss reduction can reach about 60 to 74 % for the low gate resistance case. This was expected based on the efficiency curves, which at higher currents is better for the 3-level topologies than the 2-level topologies compared to the 1.5 kV DC link case. Consequently, the energy loss reduction per phase are higher.

Table 26: 3 kV DC link railway inverters simulated configurations. The drive cycle energy loss per phase is demonstrated for each configuration. Additionally, the saved energy per phase in comparison to the equivalent Si-based topology (same T_{water} and Multiplicator) is shown in absolute values and percentage.

Topology configuration	Switching frequency (Hz)	Twat (ºC)	Multiplicator	E_{loss}/phase (kWh)	Saved energy - compared to Si (kWh)	Saved energy- Si case as reference (%)
6.5 kV Si R_G: 7.5 Ω	500	40	1	0.099463	-	-
6.5 kV Si R_G: 7.5 Ω	500	40	55	0.13964	-	-
6.5 kV Si R_G: 7.5 Ω	500	70	1	0.10706	-	-
6.5 kV Si R_G: 7.5 Ω	500	70	55	0.15256	-	-
3.3 kV SiC ANPC/R_G: 2.4 Ω	1500	40	1	0.025394	0.07407	74.5
3.3 kV SiC ANPC/R_G: 2.4 Ω	1500	40	55	0.050183	0.08946	64
3.3 kV SiC ANPC/R_G: 2.4 Ω	1500	70	1	0.03111	0.07595	70.9
3.3 kV SiC ANPC/R_G: 2.4 Ω	1500	70	55	0.06169	0.09087	59.5
3.3 kV SiC ANPC/R_G: 24 Ω	500	40	1	0.03334	0.06606	66.4

3.3 kV SiC ANPC/R_G: 24 Ω	500	40	55	0.059296	0.08034	57.5

5.2 Lifetime loss and CO2 emission reduction

The SiC inverter lifetime loss reduction compared to the respective Si inverter will be detailed for one topology configuration (3.3 kV SiC, RG: 2.4 ohm, 2-level). The same procedure is applied for the other cases, and the results are indicated in Table 27 and Table 28 for the 1.5 kV DC link and the 3 kV DC link railway systems, respectively. Since different drive cycle conditions may happen, it was considered an average of the saved energy for each topology configuration. The average saved energy per phase over one drive cycle for the two level 3.3 kV SiC (RG: 2.4 ohm) configuration compared to the Si IGBT topology is 0.033 kWh. We assume a typical train operation of about 12 hours per day, during which the drive cycle will be repeated around 108 times daily (drive cycle duration approximated to 400 s). Considering a train operation of 300 days per year, the yearly saved energy per phase is 1.069 MWh. In a 25-year lifetime and considering the whole inverter (3 phases), the lifetime loss reduction per inverter is 80.2 MWh by substituting the Si IGBT inverter for the SiC (RG: 2.4 ohm) inverter. From [15], it is well known that the use-phase is the dominant stage in terms of consumed energy, with the semiconductor manufacturing stage presenting a negligible contribution to the entire power converter life cycle (smaller than 0.3 %). In this section, we introduce the analysis of the use-phase energy, while the manufacturing phase will be further investigated in chapter 6. The highest achieved lifetime loss reduction was 200.7 MWh for the 3-level SiC topology at low gate resistance. Such loss reduction contribute to reducing the carbon footprint of the existing railway technology, helping to mitigate the effects of carbon dioxide emissions. Such a fact was estimated based on the loss reduction and the carbon intensity generation from Germany in the year of 2023 (381 gCO2-eq/kWh). Values up to 76 tons of CO2-eq per inverter lifetime could be reduced by implementing SiC-based topologies. These values can be increased even more in countries where the carbon intensity generation is higher or with a more intensive use of the inverter during its lifetime.

Table 27: 1.5 kV DC link 3-phase inverter details and inverter lifetime loss reduction and CO2-eq savings (25 years) in relation to the 3.3 kV Si IGBT-based inverter.

Inverter configuration	Si- 2 level	SiC – 2 level R_G: 2.4 Ω
Converter rating [kW]	714	630
Switching frequency [Hz]	500	1500
Lifetime loss reduction compared to the Si inverter [MWh]	-	80.2

CO_2-eq saved [tons]*	-	30.6

*Carbon intensity generation of 381 gCO2-eq/kWh considered in the calculation

Table 28: 3 kV DC link 3-phase inverter details and inverter lifetime energy and CO2-eq savings (25 years) in relation to the 6.5 kV Si IGBT-based inverter

Inverter configuration	Si- 2 level	SiC – 3 level R_G: 2.4 Ω
Converter rating [kW]	788	833
Switching frequency [Hz]	500	1500
Lifetime loss reduction compared to-the Si inverter [MWh]	-	200.7
CO_2-eq saved [tons]*		76.5

* Carbon intensity generation of 381 gCO2-eq/kWh considered in the calculation

In order to evaluate the performance of the 6.5 kV/150 A module, a 2-level inverter topology with a 3 kV DC link simulation. The primary difference was that no experimental data were available to validate the simulation results for the SiC case. Static, switching losses and thermal impedance parameters were used in the simulation based on experimental static and switching module characterization results. The efficiency simulation results were compared to the 6.5kV Si-based 2-level inverter at 500 Hz switching frequency. In order to obtain a fair comparison, the efficiency curve from the 6.5kV/300 A Si IGBT module (Figure: 78) was linearly scaled down in terms of currents by a factor of 2 to compare with the 150 A rated SiC module. Figure 84 depicts the higher efficiencies achieved by SiC technology, even with a higher switching frequency of 1.5 kHz, compared to 500 Hz for Si technology.

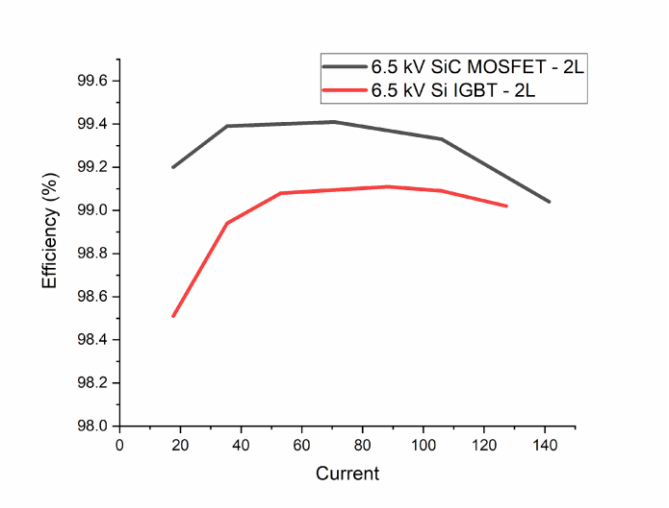


Figure 84: Efficiency comparison between 2 level inverters based on Si IGBTs at 500 Hz switching frequency and SiC MOSFETs at 1500 Hz switching frequency. The current rating of the switches is 150 A.

Finally, a drive cycle simulation (based on profile from Figure: 81) was performed to compare a 2-level inverter topology with a 3 kV DC link simulation based on 6.5 kV Si IGBT and SiC MOSFET technologies. The Si IGBT results were taken from previous section, considering that half of the energy losses occurred due to the downrating of the modules to 150 A for a fair comparison with the 150 A SiC module, with motor load current profile halved by a factor of two. Table 29 shows that SiC technology can reduce energy losses by up to 60% when switching at 500 Hz and 50% when switching at 1500 Hz. These values align with previous results from this report for the other module technologies, demonstrating the high potential of SiC technology at higher voltage classes to save a significant amount of energy.

Table 29: 3 kV DC link railway inverters simulated configurations comparison based on 6.5 kV/150 A Si IGBT and 6.5 kV/150 A SiC MOSFET semiconductor technologies. The drive cycle energy loss per phase is demonstrated for each configuration. Additionally, the saved energy per phase in comparison to the equivalent Si-based topology (same Twater and Multiplicator) is shown in absolute values and percentage.

Topology configuration	Switching frequency (Hz)	Twat (ºC)
6.5 kV Si – 2L R_G: 7.5 Ω	500	40
6.5 kV SiC – 2L	500	40
6.5 kV SiC – 2L	1500	40

5.3 Potential Reduction of Losses in Switzerland

Energy consumption of traction systems is typically challenging to estimate because it is highly dependent on the drive cycling. Further, traction systems have other components that affect energy consumption, e.g., locomotive shape, location wind speed, HVAC power electronics for passage comfort, speed profile/timetable optimization, motor type, etc.

However, since most traction systems operate in a sub-load regime where SiC outperforms Si because of the ~0.7 V threshold voltage of bipolar IGBTs, SiC has a great competitive edge against its Si counterpart as demonstrated in this report. Switzerland presented a total traction energy consumption of 1.66 TWh [16] in the year of 2024.

Approximately 60-80% of the locomotive energy demand is transmitted through the traction inverters [17], corresponding to ~1.3 TWh/yr. Considering this energy value as the input of traction inverters, and based on the fact that Si IGBT inverters may present an average efficiency of around 98%, depending on the manufacturer's design characteristics, an annual energy loss of around 26 GWh is estimated. According to the results presented in this report, SiC-based inverters can offer loss reductions of around 40-75% compared to Si-based inverters, depending on the drive cycle characteristics. Assuming a 50% loss reduction, the estimated yearly reduction of energy losses by introducing SiC inverter technology would be around 13 GWh/yr.

6 Life Cycle Analysis

6.1 Manufacturing energy

Semiconductors devices present a highly complex manufacturing process that can be divided into three main categories: (1) Substrate production, (2) Front-end, and (3) Back-end processing, as indicated in Figure 85. The first step comprises the processes performed from material extraction until wafer fabrication. The front-end stage encompasses the physical and chemical processes performed in a fab environment to transform the wafer into power device chips. Finally, the back-end processing corresponds to wafer die cutting and packaging. All steps are critical from a technical point of view and essential for achieving a reliable functional product. However, regarding cumulative energy demand (CED), the back-end processing has a minor contribution, being not the focus of most investigations so far. In addition, the SiC and Si LinPak packaging fabricated by Hitachi Energy presents the same footprint, design and materials. Thus, the packaging production energy has not been considered since it is roughly the same for both technologies and will not impact the final energy demand comparison. The LinPak packaging comprises a protecting case with external electrical contacts and a base plate for heat transfer (Figure: 86A). Internally, four substrates, as shown in Figure: 86B, are placed with bonded chips on the copper surface. Semiconductor chips are electronic devices that operate as a switch controlled by an external

signal from a controller. These chips can operate in a blocking state (open switch), with no current flowing through them, and in conducting state (closed switch), with the electrical current flowing. Such operation is responsible for the energy conditioning in power converters. The chips are soldered on the substrate top copper layer (see Figure: 86B). These substrates are made of two copper layers electrically isolated by an alumina layer. Alumina is an insulator material responsible for the electrical isolation of the bottom copper layer from the chips. This bottom layer is soldered to the external base plate made of AlSiC. This plate is the thermal connection of the chips to the external cooling system, and it is electrically isolated for safety reasons. The electrical chip connections are distributed on the top copper layer through a wire bonding technique, and then the external electrical connections are made to the users. The LinPak design is part of a class of standard state-of-the-art power modules based on a joint effort of several manufacturers. The objective was to fabricate a more reliable power module generation with improved interconnect technologies, low stray-inductance and compatibility with WBG chips [88]. These devices are aimed to be used in medium voltage applications, with each manufacturer providing a different name for a similar case design, as shown in Figure: 88. Different current ratings of SiC LinPaks are presented at 450 A, 500 A and 900 A.

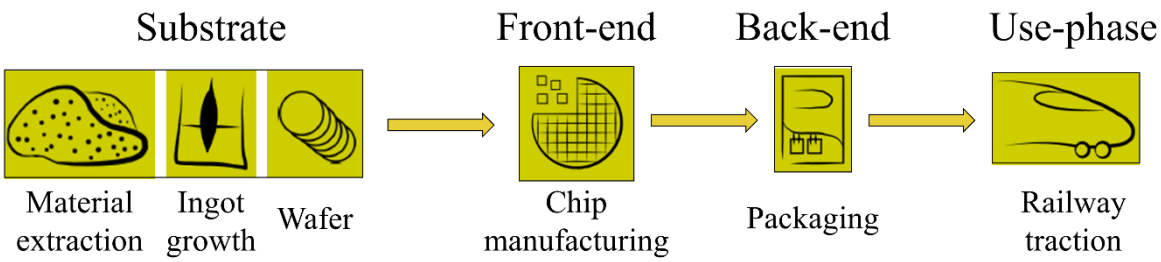


Figure 85: Power module life cycle. Substrate, front-end and back-end are part of the semiconductor manufacturing fab and the use-phase is the final application in a railway power converter.

The front-end processing presents the highest energy consumption from all three stages [18, 19], having the highest impact on the CED analysis of power devices. Due to its high complexity, one possible way of obtaining such data is by industrial reports (when available) from the electricity use and the wafer total consumption in a given period. This work used a direct measure of the fab energy consumption and the number of fabricated chips. Hence, a metric of the energy required per wafer area can be accurately obtained for specific chip technology. Hitachi Energy provided manufacturing energy consumed data for Si and SiC processed wafers. The Si IGBT data has higher accuracy since this technology presents a well-established production line.

The substrate production is the second stage in terms of cumulative energy demanded [18, 19]. The energy assessment in our work was performed for industrial standard monocrystalline 150 mm Si wafers and 150 mm 4H-SiC wafers. Intensive research and development on manufacturing larger wafers to

reduce processing costs and enhance chip production are being performed, with prospects for commercial 300 mm Si wafers and 200 mm SiC wafers. The required data for the substrate CED were obtained from the literature [18, 19]. Regarding the embodied energy of the high-purity chemicals, gases and ultra-pure water used during the processing (substrate, front-end and back-end), this category presents a lower impact on the CED analysis of silicon semiconductor processing. A contribution smaller than 11% of the total CED has been consistently reported [18, 19]. Furthermore, the investigation of the used chemicals presents a high uncertainty caused by the scarcity of semiconductor-grade chemicals' embodied energy data. In order to keep the modelling manageable and due to the relatively smaller contribution to the CED (as demonstrated for Si processing), we have not considered the embodied energy of chemicals in the model.

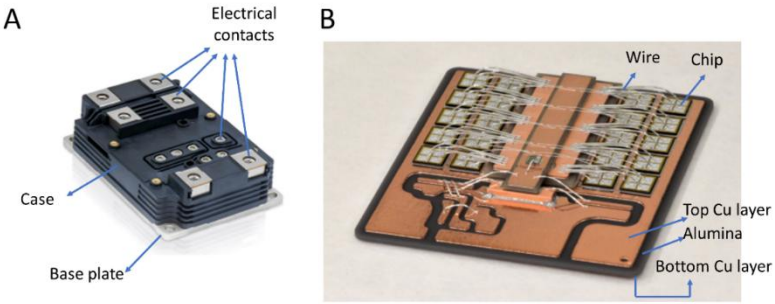


Figure 86: A. LinPak power module, B. Power module substrate with SiC chips bonded on the copper.

Figure 87: New generation of medium voltage power modules from different manufacturers. The modules are compatible with Si and SiC chips.

The analysis provided here mainly focuses on the substrate and front-end electricity requirements due to their higher contribution to the total CED. Both stages also present the most significant differences between different materials in the fabrication process. The technologies were compared during the manufacturing phase in terms of the electrical energy consumed per wafer area (kWh/cm2). Finally, a comparison between Consumed energy/module is provided, representing the module grey energy. We have

considered the same assumptions from [18] and [20] that the end-of-life energy requirement is negligible compared to substrate and front-end processing and that the transport energy has a small contribution, being equivalent among distinct power semiconductors, and not estimated in this work [18].

6.2 Power Module Manufacturing Analysis

This section highlights the process steps for Silicon (Si) and Silicon Carbide (SiC) power modules and their cumulative energy demand.

6.2.1. Silicon IGBT LinPak module

In power electronics applications, high-purity monocrystalline electronic-grade silicon is required. In particular, contamination with elements that are also suitable, as dopants must be brought below critical values by means of the Czochralski process. This process consists in filling a rotating quartz crucible with the polycrystalline silicon obtained in the Siemens process and melting it at a temperature higher than 1400 ºC in an inert gas atmosphere (e.g., argon). Due to its high heat conductivity, the quartz crucible sits inside a graphite crucible, which homogeneously transfers the heat from the surrounding heater to the quartz crucible. A monocrystalline silicon seed crystal with the desired crystal orientation is dipped into the melt. It acts as a starting point for the crystal formation supported by the heat transfer from the melt to the already-grown crystal. A slight temperature drop initiates the crystallization of silicon on the seed crystal. The seed crystal is slowly pulled upward out of the melt, and a cylindrical silicon monocrystal hanging on the seed crystal starts to form. The pulling rate and temperature are regulated such that the silicon monocrystal, whose orientation and structure are identical to the seed crystal, can be pulled with a constant diameter. The diameter is usually around 150 to 300 mm, with a height of around 2 m. High-purity silicon crystallizes in a monocrystalline form on the crystal, leaving almost all impurities in the melt. The monocrystals grown with the Czochralski technique are cut into shorter workable cylinders with a band saw. In order to increase the throughput, wire saws with many parallel wires, which cut many wafers at once, are used. The wafers are then polished, as surface damage can occur on the wafer during sawing.

The analysis from electronic-grade Si substrates adopted in our work has already been estimated by [19] with an adjusted yield of 75 % [18], providing an estimate of 0.45 kWh/cm2. The wafers are further processed at into finished packs. They undergo more than 200 steps during the front-end stage. The main processes are listed below:

Wafer Oxidation: This process is performed for gate oxide growth and to create a protective layer for other steps during the front-end stage (e. g. ion implantation). The wafers are lined up and annealed in a furnace with the addition of oxygen gas to grow an oxide film on the wafer surface.

Photolithography: This process aims to transfer the device patterns onto the wafer that will be further processed in front-end steps. Around 12 different masks are used in an industrial IGBT manufacturing cycle. A photosensitizing agent known as a photoresist is applied to the surface. The silicon wafer is

rotated at high speed during the coating process, so the photoresist is applied thinly and uniformly onto the wafer. A semiconductor lithography system aligns the silicon wafer and the photomask, reduces the electronic device pattern on the photomask and then projects light on the device pattern to the silicon wafer. After the light exposure, the developing process is performed to dissolve the photoresist exposed areas (in the case of positive photoresists), immersing the wafer in a liquid solvent to transfer the pattern onto the wafer's surface.

Etching: The etching removes any unwanted material from the wafer during processing. This process is performed several times and can be executed with liquid chemicals (wet etching) or in a plasma environment (dry etching), depending on the desired etching pattern or target material.

Doping: Transistors and diodes must have different electrical conductivity values in particular device regions to achieve the desired performance and functionality. External elements (dopants) such as boron, phosphorus, arsenic and other elements are inserted in the crystalline structure of the wafer in a controlled way. Possible methods are diffusion at high temperatures or ion implantation (ion bombarding).

Annealing: High-temperature processes in furnaces are required several times for material growth (e. g. wafer oxidation), material deposition (e. g. polysilicon gate deposition), dopant electrical activation (after ion implantation), dopant diffusion, and metal sintering to reduce electrical contact resistance.

Metallization: Metals are deposited onto the surface and in the back of the wafer to perform the electrical connections of the fabricated device to the external circuit. Several metals can be deposited using physical deposition methods (e. g. Sputtering).

The Si front-end stage was divided into two case scenarios, considering high and low utilization of the production facility. Such cases occur because the energy demand from some manufacturing processes have a fixed energy requirement. Consequently, the energy demand per wafer may vary according to the number of fabricated devices. At a high utilization rate of the production plant (Scenario 1), the energy requirement is 183.9 kWh (per 150 mm (6") wafer). At a low utilization rate (Scenario 2), the energy consumed is higher, leading to an electrical energy demand of about 221.8 kWh (per 150 mm (6") wafer). These data have been provided by the power semiconductor fab of Hitachi Energy in Switzerland, for the IGBT module production line, encompassing the global average energy demand of Si IGBTs and anti-parallel diodes. In calculating the energy demanded per area for the front-end process, the total required wafer energy was divided by the number of chips per wafer and then by the chip area. For a 6" wafer, sixty Si (60) chips of 1.3 x 1.3 cm each can be produced (typical IGBT and diode 3.3 kV chips dimension – information from an open module [93]), excluding losses, and fifty-seven (57) chips when production losses are considered (yield of 95 %). The energy required for production per chip varies depending on the capacity utilization of the production facility. Thus, the two scenarios were therefore calculated: For 3.3 kV Si IGBT chips of dimensions 1.3 x 1.3 cm, with a yielding of 57 chips, we have a total front-end energy consumption for the high utilization and low utilization plant use of 1.91

kWh/cm2 and 2.30 kWh/cm2, respectively. A LinPak 3.3 kV/450 A half-bridge comprising two switches (high and low side switches considered) requires a total of 24 Si chips. Considering the substrate and front-end energy demands, the Si LinPak grey energy is 95.72 kWh and 111.54 kWh for the high (Scenario 1) and low (Scenario 2) utilization rate of the production plant, respectively. The demanded energy per chip area and the module grey energy are indicated in Table 30 and Table 31, respectively. This work's calculated front-end energy demand (1.91 up to 2.3 kWh/cm2) is very close to the estimated value from [18, 19] of 2 kWh/cm2. Such a fact indicates that using microelectronic front-end estimates in power electronics Si IGBT devices does not significantly affect final accuracy.

Table 30: Substrate and Front-end energy demand estimate (kWh/cm^2).

Manufacturing stage *	Si devices	SiC devices
Substrate	0.45 kWh/cm^2	4.04 kWh/cm^2
Front-end (Scenario 1) [a]	1.91 kWh/cm^2	2.50 kWh/cm^2
Front-end (Scenario 2) [b]	2.30 kWh/cm^2	3.01 kWh/cm^2
Front-end (Scenario 3) [c]	1.91 kWh/cm^2	4.99 kWh/cm^2
Front-end (Scenario 4) [d]	2.30 kWh/cm^2	6.02 kWh/cm^2

aHigh production Si facility utilization with SiC 1.5 × Si energy demand.

bLow production Si facility utilization with SiC 1.5 × Si energy demand.

cHigh production Si facility utilization with SiC 3 × Si energy demand.

dLow production Si facility utilization with SiC 3 × Si energy demand.

* For Si devices, scenarios 1 and 3 are equal (High facility utilization) and scenarios 2 and 4 are equal (Low facility utilization).

Table 31: Estimate of the LinPak 3.3 kV/450 A module grey energy (kWh/module)

Cases *	Si IGBT module	SiC MOSFET module
Scenario 1 [a]	95.72 kWh	65.40 kWh
Scenario 2 [b]	111.54 kWh	70.50 kWh
Scenario 3 [c]	95.72 kWh	90.30 kWh
Scenario 4 [d]	111.54 kWh	100.60 kWh

[a]High production Si facility utilization with SiC 1.5 × Si energy demand.

[b]Low production Si facility utilization with SiC 1.5 × Si energy demand.

[c]High production Si facility utilization with SiC 3 × Si energy demand.

[d]Low production Si facility utilization with SiC 3 × Si energy demand.

* For Si devices, scenarios 1 and 3 are equal (High facility utilization) and scenarios 2 and 4 are equal (Low facility utilization).

The back-end demanded energy was not evaluated due to its minor contribution to the CED and for not presenting significant energy demand differences between Si and SiC LinPak technologies. However, we will detail the main steps from this stage.

Dicing: The final wafer is further cut into individual chips. Generally, diamond blades are used to cut the chips while spraying ultra-pure water.

Soldering: The individual chips are soldered to the substrates in a high-temperature chamber (~ 150 – 200 ºC). A metallic alloy is melted to join the chip bottom part to the Cu substrate. This step aims to fix the chips to the substrate and to electrically connect the bottom chip contact (MOSFET Drain and IGBT Collector) to the substrate.

Wire bonding: The top chip electrical connections are bonded with wires to the copper substrate with an ultrasonic wire bonder machine. This step electrically connects the top chip contacts (Gate, MOSFET Source and IGBT Emitter) to the substrate.

Packaging: The substrates are soldered to the base plate and fixed inside a closed plastic case. Internal metallic connections are used to connect the substrate to the external connectors. The module is filled with silicone gel for improved electrical isolation, mechanical stability, reliability and dust protection.

Silicon Carbide MOSFET LinPak module

SiC processing presents higher energy demand than silicon in substrate and front-end processing. Such a fact happens mainly due to the higher processing complexity that generally requires higher temperatures. SiC substrate fabrication is mainly performed with the modified Lely method, being the industry standard due to the good wafer quality and high yield (90%). This process is based on a sublimation growth technique, where the source material is held at the bottom of the crucible and the seed plate on the top. The environment temperature is in the range of 1800 – 2600 ºC with argon gas at 10-4 to 760 torr, which the seed is kept at a slightly lower temperature than the source to facilitate the vapor transport. In our work, we have used the estimate from [18] for the modified Lely process given as 4.04 kWh/cm2.

The front-end stage has almost the same steps as the Si processing, with different recipes for each stage. SiC requires a temperature higher than 1600 ºC for dopant activation, whereas Si uses a temperature between 450 – 750 ºC. Furthermore, the gate oxide growth in SiC also requires a slightly higher temperature than Si, with a temperature range between 1100 – 1400 ºC and Si in the range of 900 – 1200 ºC. Such higher temperatures make SiC require a higher energy demand than Si during the front-end. The other processes require lower energy since high temperature is not used, presenting similar magnitudes between both materials, as shown in Figure: 89. For a 6” wafer, excluding production losses,

520 chips with dimensions of 0.5 x 0.5 cm each (typical MOSFET 3.3 kV chips dimension) can be produced. Including process losses, the value reduces to 442 (yield of 85%). The yield value for the SiC technology is very dependent on the wafer quality as well as the power semiconductor manufacturer design and front-end processes, presenting a significant variation between different fabs. Such value also increases with further technology development in substrate fabrication and front-end processing techniques. The value of 69 % was assumed by [18], and further developments have been performed during these years. We estimate an 85 % yield is a realistic value that can be achieved in the future when these modules become a standard commercial product due to intensive improvements in SiC processing.

The SiC front-end energy data from Hitachi Energy have been provided in terms of range values comparative to Si. The front-end production of SiC MOSFETs requires 1.5 to 3 times more energy per 6" wafer than Si IGBTs. The large range is due to the different possibilities of processes involved in the 3.3 kV SiC device production, and accounts further for uncertainties reflected on a SiC production line incorporated within a Si manufacturing facility. It is worth mentioning, that implementing SiC into a high-volume Si facility can strongly reduce manufacturing costs. In addition, these values are also dependent on the automation level of the manufacturing site, but since annealing processes are expected to be the main driven for the SiC higher consumption, the trend is expected to remain similar. The SiC front-end analysis was then split into 4 case scenarios (shown below), considering high and low utilization of the prodoction facility and the range limits (1.5 and 3 X).

Scenario 1: × 1.5 the energy demand of silicon production with high production Si facility utilization.

Scenario 2: × 1.5 the energy demand of silicon production with low production Si facility utilization.

Scenario 3: × 3 the energy demand of silicon production with high production Si facility utilization.

Scenario 4: × 3 the energy demand of silicon production with low production Si facility utilization.

The calculated demanded energy per area (kWh/cm2) for the front-end stage and module grey energy (kWh) for all scenarios are demonstrated in Table 30 and Table 31, respectively. Figure 88 presents a graphical representation of the power modules' grey energy with the substrate and front-end contributions indicated for each scenario. This graphical comparison shows that for SiC technology, the substrate production may present a higher CED than the front-end stage, depending on the plant utilization.

It has been considered that one wafer of 6" can generate 442 chips of 0.5 x 0.5 cm each requiring a total of 40 chips in the 3.3 kV/450 A LinPak power module [60]. The SiC MOSFET module presents a lower CED than the Si IGBT module in all possible scenarios. This fact occurs even considering that the SiC chip yield is lower than the Si IGBT (85 % versus 95 %), caused by the larger number of defects in

the SiC wafer. On top of that, the SiC substrate energy demand per area is also higher than the Si substrate. In fact, the dominant factor is the smaller area per Ampere required per chip in the SiC technology compared to Silicon. Additionally, using the internal body diode as an antiparallel diode, not requiring additional external diode chips as in the case of Si IGBTs, also reduces the required area. As a result, a much smaller area for the same current rating (450 A) is required (10 versus 40.56 cm2). This fact occurs due to the SiC intrinsic characteristics [1], allowing the design of high-power density chips. The SiC LinPak grey energy may be further reduced in the future with the implementation of a High-temperature chemical vapor deposition (CVD) process [18]. Such a method can potentially reduce the wafer defect density [18], attracting semiconductor manufacturers for further research. An estimate of 2.78 kWh/cm2 demanded energy for this process is given in [18], which can reduce the SiC LinPak substrate energy demand to a value of 27.8 kWh compared to the Lely method of 40.4 kWh.

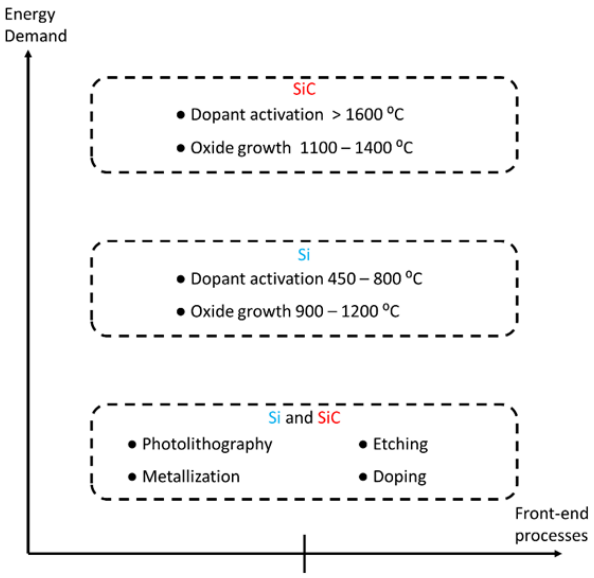


Figure 88: Energy demand representation from different front-end processes for Si and SiC. Dopant activation and oxide growth are the processes with the highest thermal budget required, with SiC exhibiting the highest values.

Regarding the front-end estimates, our values were in the range of 2.50 up to 6.02 kWh/cm2, depending on the chosen scenario. Reference [18] estimated 2.43 kWh/cm2 based on 600 V SiC Schottky diode processing data. Our estimates are about 1.03 – 2.48× higher than the estimate of [35]. Such difference may be related to the fact that 3.3 kV SiC MOSFETs may present a higher energy demand than 600 V SiC Schottky diodes since low voltage diodes present more straightforward manufacturing steps. In a late stage of the project, after the realization of this study, further estimations have been performed by Hitachi Energy of 1.19 kWh/cm2 for SiC wafers and 0.84 kWh/cm2 for Si IGBTs and 0.9 kWh/cm2 for diode wafers, featuring a difference of about ~40% between SiC and Si. This difference is higher than the 30% assumed in this work, thereby representing even a better lifetime energy benefit. At module

level, the 3.3 kV 450A half-bridge modules with 36 25A SiC MOSFETs featured an energy of 9.85 kWh/module, while the same packaging featured 8 IGBTs and 8 diodes with 112.5A rate resulted in 31.2 kWh/module.

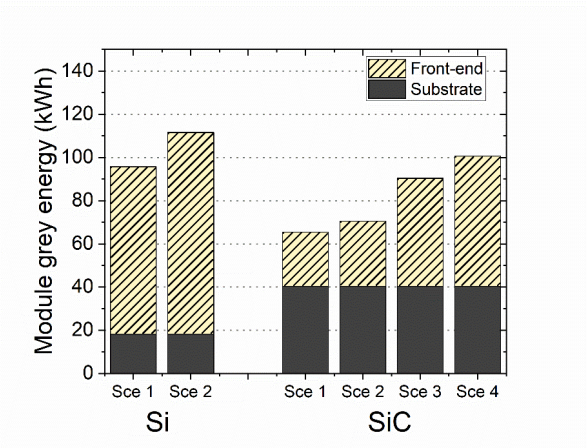


Figure 88: Power modules grey energy for different scenarios with the substrate and front-end energy demand contributions indicated separately. The scenarios shown in the x-coordinate are described as such: Sce 1: × 1.5 the energy demand of silicon production with high production Si facility utilization, Sce 2: × 1.5 the energy demand of silicon production with low production Si facility utilization, Sce 3: × 3 the energy demand of silicon production with high production Si facility utilization, and Sce 4: × 3 the energy demand of silicon production with low production Si facility utilization.

As a summary of this section, the following conclusions are drafted:

- The grey energy per module of substrates of the SiC chips is higher than for Si.
- In all scenarios, the front-end grey energy per module of SiC is lower than Si because of smaller chip size for equivalent current density.
- The overall grey energy of SiC chips per module is equal or lower than Si in all scenarios because both current density, but also because the SiC MOSFET modules do not require a separate antiparallel diode as in the Si case.

7 Conclusions and outlook

The advancement of energy-efficient technologies represents a critical priority for sustainable development and economic stability, particularly in societies confronted with rising electricity costs. A strategic approach to achieving this objective involves focusing on high-power electronic converters, as these systems account for a substantial fraction of global electrical energy consumption and associated losses. Approximately 40–45% of worldwide electricity is consumed by electric motors, with a significant share concentrated in industrial and transportation sectors. Medium-voltage (MV) power converters are integral to these applications, thereby offering considerable potential for global reduction of losses.

At the core of power electronic converters are power semiconductor devices, which play a decisive role in enhancing energy conversion efficiency. Silicon carbide (SiC)-based semiconductors demonstrate markedly lower power losses compared to conventional silicon (Si) technology. The SiC-MILE project was initiated to establish enabling technologies for the future development of MV SiC MOSFETs, power modules, and railway converter systems, with a focus on the 3.3 kV and 6.5 kV voltage classes.

This report details the design and fabrication processes of the 3.3 kV and 6.5 kV SiC chips, including packaging, electrical characterization at both wafer and module levels, and reliability assessments. Additionally, a dedicated converter test bench was constructed to evaluate Si and SiC power module losses under realistic operating conditions, employing highly accurate thermal and electrical measurement techniques. The project achieved several key outcomes aligned with its objectives. Prototypes of 3.3kV and 6.5kV SiC MOSFETs were successfully manufactured in the product line of Hitachi Energy. The electrical parameters were analyzed. TCAD simulations were performed to optimize the cell layout and to find the most suitable parameters. Then the first MOSFET devices were fabricated. For the 3.3kV devices two learning cycles were concluded, where the channel profiles, channel length and JTE dose was optimized. The V_{th} values are slightly dispersed between 2.0V-3.0V. The Rds,on values are between 150mOhm-250mOhm, and the leakage is for all devices between 1-10 uA. For the 6.5kV MOSFET devices the focus of the optimization was mainly on the termination design. Different p+ rings as well as JTE doses were used to find the most optimum device. Modules were fabricated from the most suitable dies and were characterized. It was then successfully demonstrated Si and SiC modules at 3.3 kV and 6.5 kV, with electrical characterization validating their suitability for MV applications. A 3.3 kV MV converter demonstrator was developed, integrating both Si and SiC modules, and supported by test benches that enabled detailed characterization of energy losses across a wide frequency range and varying gate resistances. These results were subsequently applied to calibrate railway SiC converters under diverse topologies, operating frequencies, cooling conditions, and drive cycles. Relative to Si-based railway converters, SiC converters exhibited superior efficiency and load capacity across broad frequency ranges, primarily due to reduced energy losses. This improvement enables the design of more compact systems with lower cooling and magnetic requirements, while also extending the autonomous operating range of battery-powered trains. Hitachi Energy used the knowledge generated in this project to implement SiC LinPak in a leading European Traction OEM. The Battery train enters field of operation in Jan 2025. A 3.3kV SiC LinPak module is used in tandem with the RoadPak™ in BEMU to enable regional none-electrified lines in a range of 80km.

Although fabrication of 6.5 kV SiC modules was successful, failures occurred during converter testing, and further development is ongoing to achieve product qualification. The project also conducted the first comprehensive lifecycle assessment (LCA) of SiC power semiconductors. Results indicate significantly lower equivalent CO_2 emissions compared to mainstream Si technology, with the usage phase contributing most to the reduced environmental footprint. Notably, although the substrate grey energy per module of SiC is higher than Si, the front-end grey energy is significantly lower because the current density

of SiC chips is higher, and SiC modules do not require an extra Si anti parallel diode. Furthermore, SiC traction converters demonstrated reductions in energy losses ranging from 40% to 75%, depending on drive cycle and topology. Assuming a 50% loss reduction scenario, this corresponds to an annual electricity saving of approximately 13 GWh in Switzerland—nearly equivalent to the combined annual output of the Beznau (KKB) and Gösgen (KKB) nuclear power plants.

Building on the promising outcomes of the SiC-MILE project, future research efforts could focus on expanding the application scope of SiC technology within traction systems. There is significant potential to investigate the efficiency gains of SiC-based solutions in HVAC (Heating, Ventilation, and Air Conditioning) converters and DC link converters, both of which play critical roles in the overall energy management of electric rail vehicles. These subsystems often operate under variable load conditions and thermal constraints, making them ideal candidates for SiC integration due to its superior switching performance and thermal conductivity. Detailed studies on power loss reduction, thermal optimization, and lifecycle environmental impact in these converter types could further validate SiC's role in enhancing system-wide efficiency and sustainability. Such investigations would not only deepen our understanding of SiC's capabilities but also accelerate its adoption in broader railway infrastructure, contributing to the next generation of low-emission, high-performance transportation networks.

8 National and international cooperation

This project is a collaboration executed between HITACHI ENERGY and the FHNW in Switzerland.

9 Publications and other communications

L. B. Spejo, I. Akor, M. Rahimo, and R. A. Minamisawa, "Life-cycle energy demand comparison of medium voltage silicon IGBT and silicon carbide MOSFET power semiconductor modules in railway traction applications," Power Electron. Dev. Comp., vol. 6, p. 100050, Oct. 2023.

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