Schweizerische Eidgenossenschaft
Confédération suisse
Confederazione Svizzera
Confederaziun svizra

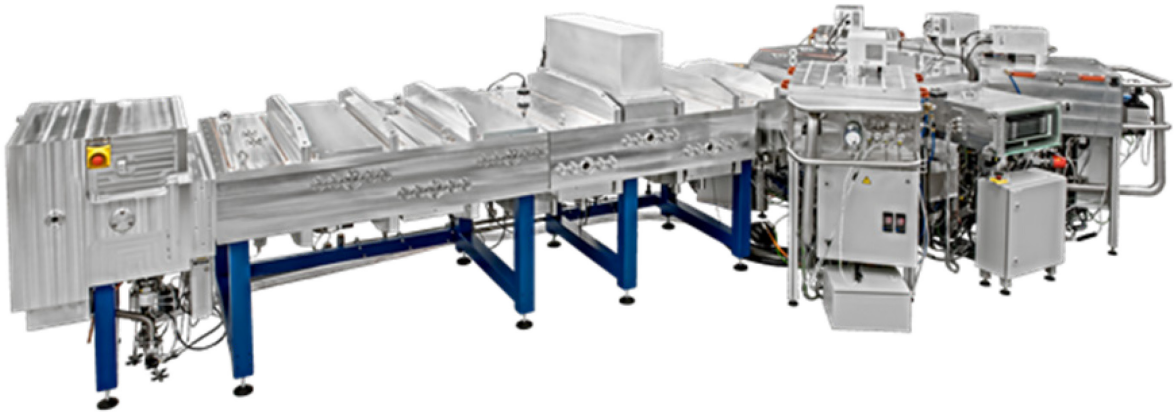
Federal Department of the Environment, Transport, Energy and Communications DETEC

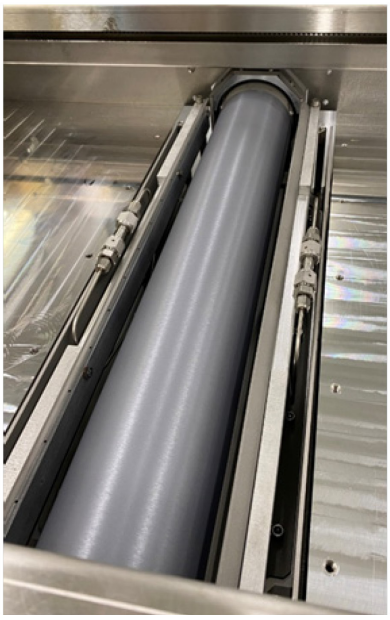
Swiss Federal Office of Energy SFOE
Energy Research and Cleantech

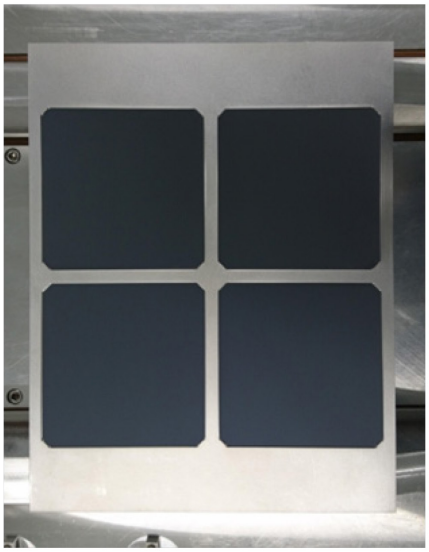
Final report

DELAPS

Demonstration of Large-Area Passivating contact Sputtering for high-efficiency solar cells







Source: ©CSEM 2023

Date: 08.12.2023

Location: Bern

Publisher:
Swiss Federal Office of Energy SFOE
Energy Research and Cleantech
CH-3003 Bern
www.bfe.admin.ch

Subsidy recipients:
CSEM S.A.
Jaquet-Droz 1, CH-2000 Neuchâtel
www.csem.ch

Authors:
Antoine Descoeudres, CSEM, antoine.descoeudres@csem.ch
Bertrand Paviet-Salomon, CSEM, bertrand.paviet-salomon@csem.ch

SFOE project coordinators:
Karin Söderström, karin.soederstroem@bfe.admin.ch
Stefan Oberholzer, stefan.oberholzer@bfe.admin.ch

SFOE contract number: SI/502207-01

Zusammenfassung

Der derzeitige Weltmarkt für Photovoltaik wird weitgehend von kristallinen Siliziumtechnologien beherrscht. Unter ihnen ist die PERC-Technologie zum neuen Standard für Mainstream-Produkte geworden. Die nächste offensichtliche technologische Verbesserung wird in der Einführung so genannter "passivierender Kontakte" bestehen. Für die Herstellung solcher Kontakte aus dünnen Poly-Si-Schichten waren bisher relativ komplexe und langsame Abscheidungsprozesse (LPCVD oder PECVD) erforderlich. In diesem Zusammenhang erscheint das Sputtern als eine sehr interessante Alternative, da es einen hohen Durchsatz und eine einfache Verarbeitung auf Maschinen mit geringen Investitionskosten ermöglicht. Nach der erfolgreichen Demonstration dieses Konzepts an Geräten im Labormaßstab zielte das DELAPS-Projekt auf die Entwicklung von Sputterprozessen auf einer produktionsnahen Pilotanlage für die Herstellung industrieller großflächiger Hocheffizienz-Solarzellen mit einseitig passivierenden Kontakten ab.

Die wichtigste Errungenschaft des Projekts ist die Installation und Inbetriebnahme eines neuen Magnetrons mit einem rotierenden Si-Target, das speziell für Hochtemperatur-Passivierungskontaktanwendungen an der bestehenden Inline-Sputteranlage am CSEM vorgesehen ist. Zusätzlich zu den intrinsischen Si-Schichten können durch die Möglichkeit, Phosphin in das Prozessgas zu geben, auch n-dotierte Schichten in-situ abgeschieden werden, was für die Herstellung von Solarzellen von großem praktischen Interesse ist. Bestehende Sputterprozesse, die auf einer kleinen F&E-Anlage entwickelt wurden, wurden dann auf die industrielle Anlage übertragen und hochskaliert, um *n*-Typ-Poly-Si-Schichten mit vielversprechenden Passivierungs- und Kontakteigenschaften zu erzeugen. Auf der Grundlage der während der Entwicklung dieser Prozesse gesammelten Daten wurde das hohe Durchsatzpotenzial des Sputterns im Zusammenhang mit der Herstellung von Solarzellen mit passivierenden Kontakten bestätigt. Daher könnte der Einsatz des Sputterns anstelle konventioneller Abscheidungsmethoden zu erheblichen Vereinfachungen der bestehenden industriellen Zellprozessabläufe führen.

Résumé

Le marché global actuel du photovoltaïque est largement dominé par les technologies du silicium cristallin. Parmi elles, la technologie PERC est devenue la nouvelle norme pour les produits de masse. La prochaine amélioration technologique consistera sans doute en l'intégration de "contacts passivants". La formation de tels contacts, faits de couches minces de silicium polycristallin, a reposé jusqu'à maintenant sur des méthodes de dépôts relativement complexes et lentes (LPCVD ou PECVD). Dans ce contexte, la pulvérisation cathodique apparaît comme une alternative prometteuse, grâce à un potentiel de production élevé et à un processus simple sur des machines à bas coûts. Après démonstrations réussies de ce concept sur des dispositifs de taille "laboratoire", le projet DELAPS a eu pour but de développer de tels processus de pulvérisation cathodique sur une machine pilote en-ligne proche de la production, pour la fabrication de cellules solaires industrielles de grande surface et à haut rendement avec contacts passivants sur une face.

La principale réalisation du projet est l'installation et la mise en service d'un nouveau magnétron équipé d'une cible de silicium rotative spécifiquement dédié aux applications de contacts passivants à haute température sur la machine de pulvérisation cathodique en-ligne existante au CSEM. Outre les couches de silicium intrinsèques, la possibilité d'ajouter de la phosphine dans le gaz de pulvérisation permet également de déposer des couches dopées in situ de type *n*, ce qui présente un grand intérêt pratique pour la fabrication de cellules solaires. Les procédés de pulvérisation existants développés sur un outil de R&D de petite taille ont ensuite été transférés et mis à l'échelle dans la machine industrielle, avec pour résultat des couches de silicium polycristallin de type *n* aux propriétés de passivation et de contact prometteuses. Sur la base des données réelles recueillies au cours du développement de ces procédés, le potentiel de production élevé de la pulvérisation cathodique dans le contexte de la fabrication de cellules solaires à contacts passivants a été confirmé. Par conséquent, l'implémentation de la pulvérisation cathodique à la place des méthodes de dépôt conventionnelles pourrait conduire à des simplifications significatives des flux de processus industriels existants pour la fabrication de cellules.

Summary

The current global photovoltaics market is largely dominated by crystalline silicon technologies. Among them, the PERC technology has become the new standard for mainstream products. The next obvious technology upgrade will consist in implementing so-called "passivating contacts". The formation of such contacts, made of poly-Si thin layers, has relied so far on relatively complex and slow deposition processes (LPCVD or PECVD). In this context, sputtering appears as a very interesting alternative, thanks to its high throughput potential and simple processing based on machines with low CAPEX. After successful demonstrations of this concept on lab-scale devices, the DELAPS project aimed at the development of sputtering processes on an in-line close-to-production pilot tool, for the fabrication of industrial large-area high-efficiency solar cells featuring passivating contacts on one side.

The main achievement of the project is the installation and commissioning of a new magnetron equipped with a rotary Si target specifically dedicated to high-temperature passivating contact applications on the existing in-line sputtering tool at CSEM. In addition to intrinsic Si layers, the possibility to add phosphine in the processing gas permits to deposit in-situ *n*-type doped layers as well, which is of high practical interest for solar cell fabrication. Existing sputtering processes developed on a small-size R&D tool have then been transferred and upscaled in the industrial tool, yielding *n*-type poly-Si layers with promising passivation and contacting properties. Based on actual data gathered during the development of these processes, the high throughput potential of sputtering in the context of the fabrication of solar cells featuring passivating contacts has been confirmed. Therefore, the implementation of sputtering instead of conventional deposition methods could lead to significant simplifications of the existing industrial cell process flows.

Main findings

- Installation and commissioning of a pilot in-line semi-industrial sputtering tool equipped with a silicon rotary target, allowing for large-area depositions of intrinsic and in-situ doped silicon layers
- Demonstration of sputtering processes for polycrystalline silicon layers used in high-efficiency crystalline silicon solar cells featuring high-temperature passivating contacts
- Proof-of-concept for a simplified high-efficiency cell process flow with high-throughput potential compatible with mass production conditions

Contents

Abbreviations

a-Si	amorphous silicon
AlO_x	aluminum oxide
B_2O_3	boron oxide
c-Si	crystalline silicon
CAPEX	capital expenditure
DC	Direct Current
ECV	Electrochemical Capacitance-Voltage
ETL	Electron Transport Layer
HTL	Hole Transport Layer
HTPC	High Temperature Passivated Contact
IBC	Interdigitated Back Contact
iV_{oc}	implied open-circuit voltage
$J_{0,pass}$	saturation current density in passivated area
$J_{0,met}$	saturation current density in metallized area
LPCVD	Low Pressure Chemical Vapour Deposition
OPEX	operational expenditure
PCD	Photo-Conductance Decay
PECVD	Plasma-Enhanced Chemical Vapour Deposition
PERC	Passivated Emitter Rear Contact
PERT	Passivated Emitter Rear Totally diffused
PH_3	phosphine
PL	Photo-Luminescence
poly-Si	polycrystalline silicon
PV	photovoltaics
PVD	Physical Vapour Deposition
ρ_c (and ρ_c*)	contact resistivity (value measured without isolation of TLM pattern, overestimated)
RF	Radio Frequency
SiN_x	silicon nitride
SiO_x	silicon oxide
Si:P	phosphorus-doped silicon
TCO	Transparent Conductive Oxide
TLM	Transfer Length Method
TOPCon	Tunnel Oxide Passivated Contact
TRL	Technology Readiness Level

1 Introduction

1.1 Background information and current situation

The global PV market is nowadays largely dominated by c-Si technologies, and this situation will most likely continue for the coming decades. Recently, the PERC technology has continuously gained market shares and has now become the standard for mainstream c-Si products. Its industrial success relies on cell efficiency improvement obtained with a relatively minor adaptation of the classical "aluminum back surface field" cell technology, which was the previous standard. Incremental technological upgrades appear thus as the most favoured evolution scheme in the PV industry, compared to the introduction of more disruptive approaches with nonetheless higher efficiency potential (like the heterojunction technology or back-contacted cells). The PERC technology and its derivatives are expected to be still dominating for a few years [1].

The next mainstream technology upgrade is expected to be the implementation of so-called "high-temperature passivated contacts" or HTPC at the back side of PERC-type cells. With such contacts, carrier recombination losses occurring at the direct c-Si/metal interface are strongly reduced thanks to the insertion of a thin dielectric layer in between. One example of HTPC is the use of an ultra-thin tunnel SiO_x layer of a few nanometers on the c-Si substrate surface, followed by a doped poly-Si layer of ~100 nm underneath the metallic contacts. The most known example of this principle is the TOPCon technology initially developed at Fraunhofer ISE in Germany. Figure 1 shows schemes of the most straightforward evolution for industrial solar cells based on the PERC technology, with implementation of HTPC at the back side. At a later stage, HTPC could even be implemented on both sides of the cells, to further reduce recombination losses at the front side. Since typical poly-Si layers in HTPC are rather thick and thus absorbing light parasitically, this more advanced cell architecture will however require a localization method to restrict the front poly-Si layers only under the metallized areas, the rest of the front surface being passivated with transparent dielectric layers (typically SiN_x, AlO_x or SiO_x).

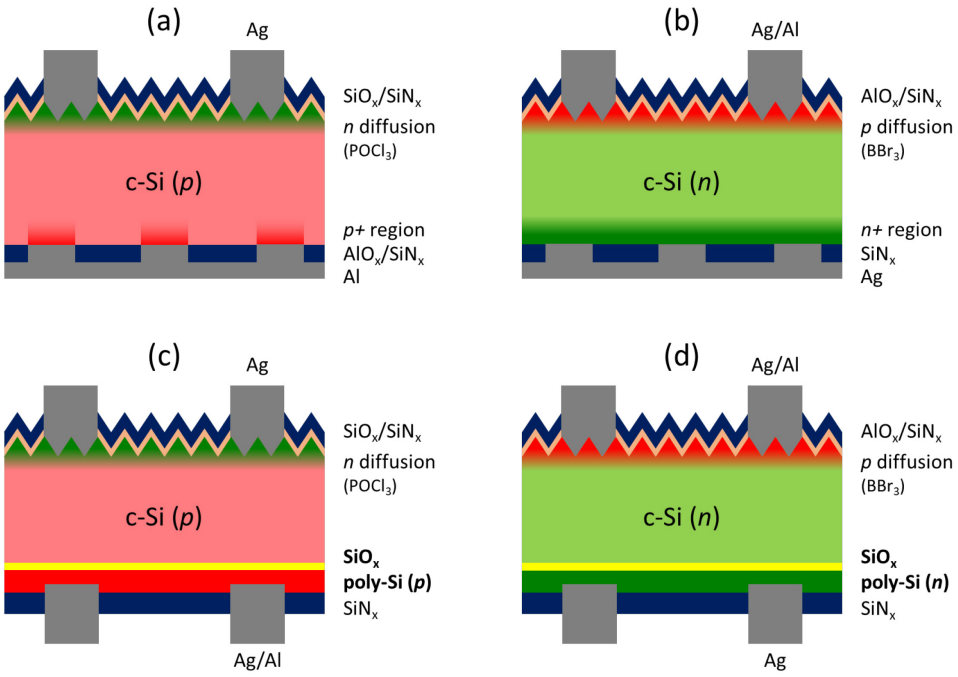


Fig. 1: Expected evolution of existing (a) PERC (using p-type substrates) and (b) PERT (using n-type substrates) industrial cells into (c) PERC+ and (d) PERT+ devices, with implementation of HTPC at the back side.

Very high efficiencies above 26% have been demonstrated on lab-scale devices featuring HTPC (both sides contacted [2] or back-side contacted [3]). However, their fabrication processes remain complex and not yet fully adapted for mass production, even though remarkable progress has been made recently on large-area industrial devices (>25% announced by several Chinese companies [4-7]). The main bottleneck is the deposition of the poly-Si layer, usually done via LPCVD or PECVD. These two methods have limitations, especially regarding their throughputs for mass production and also in terms of wrap-around, as parasitic deposition on substrate edge readily occurs (effectively shunting the *p-n* junction and consequently requiring an additional fabrication step to etch back the poly-Si from the unwanted side of the solar cell). Sputtering – a PVD method – appears in this context as a very promising alternative, thanks to higher throughput potential (>6000 wafers/hour vs. ~4000 wafers/hour for PECVD, for example), very directional deposition and simple processing based on machines with low CAPEX. Figure 2 summarizes the various advantages and disadvantages of each of the three deposition methods for the formation of HTPC.

	LPCVD	PECVD	PVD
Industrial	Yes	Yes	Yes
Asymmetric doping	No	Yes	Yes
Layer tunability	Low	High	High
Single side deposition	No	Yes, edges difficult	Yes
Production throughput	High	Medium	High
Hazardous gases	Yes	Yes	Optional
Vacuum	Low	High	High
Equipment cost	Medium	High	Medium

Fig. 2: Advantages and disadvantages of LPCVD, PECVD and PVD (sputtering) in the context of HTPC layer fabrication.

1.2 Purpose of the project

In this context, sputtered HTPC appear as a very attractive solution for the solar cell industry, which will allow for the first time to combine both potentials of high-efficiency devices with high throughput and simple processing. Indeed, the addition of only one sputtering tool would be required in existing PERC production lines, leading to efficiency increase by replacing the back contact with an HTPC approach. In addition, sputtering could also be used to form the tunnel SiO_x layer usually grown by wet chemistry, in the very same tool as for the poly-Si layer that would be directly deposited on top of it. Eventually, sputtered Si compounds could be implemented in perovskite/silicon tandem structures to form recombination junctions. In such devices, the use of high-temperature compatible bottom cell contacts would be notably beneficial for the subsequent perovskite processing.

Such sputtered poly-Si layers needed for the formation of HTPC have been investigated in the frame of a parallel SFOE R&D project led by EPFL PV-Lab (project "iPrecise", March 2021 – February 2024). This project was focused on the development of advanced high-efficiency lab-scale solar cells featuring HTPC on both sides and eventually in the interdigitated back-contacted configuration. A specific part of this project performed by CSEM was precisely dedicated to the development of sputtered poly-Si layers, deposited exclusively in a R&D single-wafer sputtering equipment (Oerlikon ClusterLine).

The present DELAPS P+D project has therefore been built on the know-how acquired during the "iPrecise" R&D project and on previous in-house initial developments made at CSEM. While these R&D studies have investigated the effect of tuning deposition parameters at lab scale to optimize cell efficiency and to elucidate the fundamental mechanisms governing the properties of PVD-based HTPC

cells, it appeared necessary to start in parallel a P+D project to develop an in-line processing in another industrially-relevant equipment (INDEOtec Octopus II), to demonstrate its industrial feasibility for potential customers. The DELAPS P+D project has thus been constantly fed with results from the different R&D studies, but represents a step further in terms of industrialization of this technological approach.

1.3 Objectives

The main objective of DELAPS was therefore to transfer and optimize the developed processes from the R&D sputtering reactor used so far to an in-line close-to-production pilot sputtering tool installed at CSEM, including the necessary hardware upgrade required for such activities (see section 2 below). The use of industry-compatible equipment permits to upscale the produced PERC+ and PERT+ devices, aiming eventually at the demonstration of high efficiencies on full-area 6" solar cells.

In more detail, the objectives of the project were:

- Upgrade of the Octopus II semi-industrial PVD reactor and infrastructure at CSEM with a new magnetron and a silicon rotary target, allowing for large-area depositions by sputtering of intrinsic and in-situ doped silicon layers;
- Transfer of the best-known sputtering processes for HTPC, previously developed at EPFL/CSEM in a R&D tool, to the Octopus II reactor;
- Thorough optimization of these processes, to fabricate high-quality HTPC layers characterized by implied open-circuit voltages (iV_{oc}) > 730 mV and contact resistivities (ρ_c) < 1 mΩ·cm^2 for *n*-type doping (measured on symmetric test samples);
- Demonstration of the high-throughput potential of the developed sputtering processes, targeting 6000 wafers/hour once implemented in mass production equipment;
- Fabrication of full-area 6" PERT+ solar cells featuring sputtered HTPC at their back sides, with efficiencies > 24%;
- Calculations of Cost of Ownership (CoO) for the developed technology, and definition of a roadmap for its further industrialization based on the small pilot line established at CSEM at the end of the project.

An assessment of the fulfillment of these objectives at the end of the project is given in section 4.4 below.

It has to be noted that the specific objectives of the project have been revised at mid-project and some activities initially planned had to be withdrawn. Indeed, several unforeseen technical issues arose during the project and have strongly slowed down the advancement of the work: significant challenges for the fabrication of a doped-Si rotary target, and global supply chain problems for numerous parts needed for the hardware upgrade, mainly.

Even though the development of *p*-type contacts, some cell efficiency targets, and the fabrication of mini-modules were abandoned compared to the initial plan, the industrial relevance and impact of the project remained. Indeed, the demonstration of *n*-type HTPC formation (of most industrial interest compared to *p*-type nowadays) by in-line sputtering with a large-area rotary target is already a significant achievement for the PV community. Regarding cell efficiency targets, the TRL of sputtered HTPC has probably been overestimated at the time of project submission (unexpected difficulty for rotary Si target production, mainly). Thus, at mid-project the project scope appeared too broad and some goals too ambitious considering the time frame of the project, leading to this revision of project objectives.

2 Description of facility

As previously mentioned, two different PVD equipment are used at CSEM for the development of sputtered poly-Si HTPC layers. First, the Oerlikon ClusterLine is a single-wafer tool with several chambers, each equipped with a magnetron and with one or up to four small size sputtering targets, powered with DC or RF sources. This tool is especially well suited for R&D experiments, since it allows for the investigation of a large variety of target materials and process parameters, including co-sputtering with multiple targets. The main drawbacks are the limited size of the chambers (suited for single 6-inch wafer) and consequently a low process throughput.

On the other hand, the INDEOtec Octopus II is an in-line PVD reactor equipped with up to six large-area planar or rotary targets (Figure 3), able to process four 6-inch wafers per carrier-plate (Figure 4, left). Even if the size of the carrier-plate is still limited, the in-line concept and the use of rotary targets are nevertheless fully compatible with requirements of mass production tools, allowing for high throughput, machine up-time and target material usage, and good deposition uniformity. A successful demonstration of a sputtering process on this Octopus II machine is therefore completely relevant for industrial customers, the remaining upscaling work to a real mass production size being afterwards relatively easy. The main drawback of this machine is a low flexibility of the hardware compared to the ClusterLine, mainly due to the large size of the targets (more costly, more difficult to be fabricated and to be changed routinely). In the context of a process development and its industrialization, these two machines available in CSEM clean room are truly complementary, as the iPrecise and DELAPS projects were.

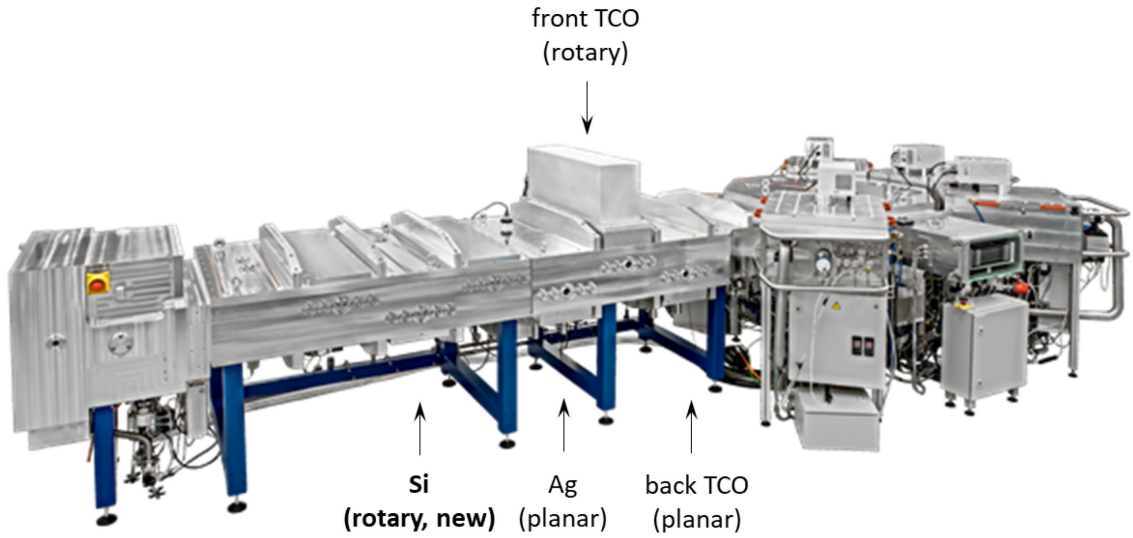


Fig. 3: Octopus II PECVD-PVD cluster tool by INDEOtec installed at CSEM. The sputtering tool used in this project is the long part visible on the left, several PECVD reactors being on the right. The target configuration is indicated on the picture.

At the beginning of the DELAPS project, the Octopus II PVD tool was equipped with three magnetrons / targets, all used for the production of silicon heterojunction solar cells (front and back TCO and back metallization, see Figure 3). A first crucial part of the project was therefore dedicated to the design, construction, and installation of a new DC rotary magnetron, exclusively used for the sputtering of Si layers for HTPC formation.

As it will be shown in section 4 below, one major outcome of the iPrecise project for DELAPS activities was the definition of the ideal specifications for the Si rotary target, giving the best properties for *n*-type HTPC applications. It has been shown that the best choice was a phosphorus-doped Si target (Si:P)

with 3% P-content (or at least 2%), permitting in-situ doping. However, the fabrication of such a target appeared extremely challenging in practice. In addition to global supply chain issues occurring for a vast range of materials and parts during the time of the project, very few suppliers worldwide could fabricate such Si:P targets with the required properties, and only one actually agreed to try to produce it. After several attempts to spray-coat a rotary target, this company finally renounced, facing some safety issues with P incorporation in Si for high P content, this material being easily inflammable. As a fallback option, it was decided to fabricate an intrinsic Si rotary target instead. This target was installed in the Octopus II tool (see Figure 4, right) and was used during the remaining part of the project. Different *n*-type doping methods were investigated, and results are given in section 4 below.

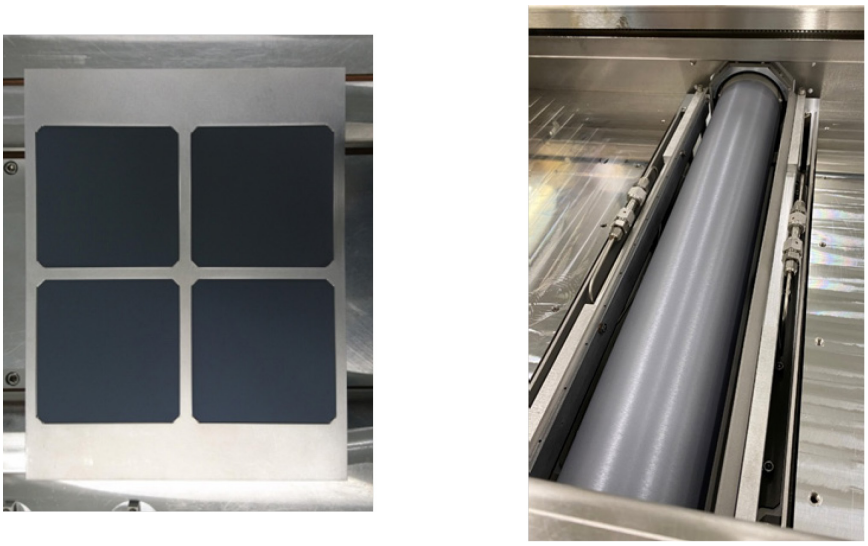


Fig. 4: (Left) Octopus II carrier-plate with four 6-inch wafers; (Right) Si rotary target installed on the new DC magnetron, mounted in the PVD vacuum chamber. Sputtering is done from below the carrier-plate.

In addition to the upgrade of the Octopus II machine itself, an adaptation of the existing CSEM infrastructure was also needed for this project. As it will be described below (section 4), the addition of a new gas line for sputtering with an argon-phosphine ($Ar+PH_3$) mixture was a highly interesting approach for in-situ *n*-type doping. As phosphine is a toxic gas, a complete safety assessment was required. A dedicated gas scrubber to handle exhaust gases at the outlet of the Octopus II PVD pumping system has been installed. Additionally, a thorough upgrade of the Octopus II electrical cabinet, automation system and software were also performed for safety reasons.

Despite the many technical difficulties encountered, the Octopus II PVD machine has been finally successfully upgraded. CSEM possesses now a quite unique pilot tool to perform in-line large-area sputtering of intrinsic and in-situ doped Si layers, of industrial relevance. This represents undoubtedly one of the main achievements of the DELAPS project.

3 Procedures and methodology

Two main tasks were performed during the project:

- Octopus II hardware upgrade (see section 2 above for details): Magnetron design and construction, Si target specification and fabrication, electrical and software upgrade, infrastructure adaptation, safety assessment.
- PVD cell process development: During the first part of the project, preliminary work was done on the ClusterLine tool (exploitation of some iPrecise results and dedicated experiments), to define the most promising cell process approaches and the necessary inputs for the Octopus II hardware upgrade (e.g. Si target specifications, doping method). In a second phase, once the upgrade was completed, process transfer, upscaling and new developments were performed on the Octopus II tool.

Regarding the development of PVD cell process, a specific method has been set up to characterize thoroughly the properties of the poly-Si layers developed for HTPC. Such layers must fulfill two main purposes: passivation of the c-Si wafer surface and efficient carrier extraction. Passivation is classically quantified by the implied open-circuit voltage iV_{oc} and the saturation current densities $J_{0,pass}$ in non-metallized areas of the wafer and $J_{0,met}$ under the metallized contacts, these parameters being measured by PCD and PL methods. The most relevant parameter quantifying the carrier extraction is the contact resistivity ρ_c between the metallization and the poly-Si layer, measured by TLM (transfer length method). Additionally, the active dopant profile in the poly-Si layer and in the wafer is another important property for HTPC contacts, measured by ECV (electrochemical capacitance-voltage profiling). A dedicated screen-printing metallization design has been developed in order to measure all these parameters on a single wafer, symmetrically passivated with the poly-Si layer under test. As shown in Figure 5, the metallization features classical TLM pads for ρ_c (top left corner), non-metallized areas for iV_{oc} and ECV, but also several squares with printed lines of various metallization fraction. The dependance of the passivation level on the different metallization fractions allows to extract $J_{0,pass}$ and $J_{0,met}$ separately. This approach permits to efficiently test different process conditions for sputtered poly-Si layers, without the need to fabricate complete solar cells. Eventually, the most promising layers are obviously also integrated in complete devices, characterized by standard illuminated current-voltage measurements with a sun simulator.

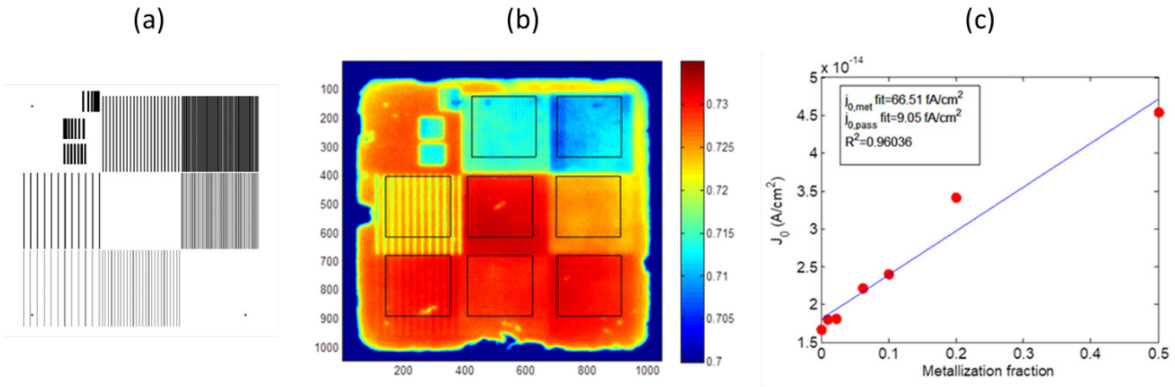


Fig. 5: Methodology for characterization of HTPC properties (iV_{oc}, $J_{0,pass}$, $J_{0,met}$, ρ_c) on symmetrical test samples: (a) design of metallization screen; (b) example of iV_{oc} mapping measured with PL and PCD; (c) dependance of J_0 on metallization fraction.

4 Results and discussion

4.1 Poly-Si layer development on R&D tool

As explained above, several experiments have been performed on the ClusterLine – partly done in the frame of the iPrecise project – to acquire knowledge about the PVD cell process and to define the best specifications for the Octopus II hardware upgrade. For clarity and conciseness, only the most relevant results will be presented here. It can be noted that numerous process parameters have to be optimized, most of them having a strong influence on HTPC performance and being inter-dependent to each other. Following the general process flow of a PVD HTPC solar cell, one has indeed to optimize: wafer surface preparation and cleaning by wet-chemistry, tunnel oxide growth method and properties, sputtering process parameters (target, plasma and deposited poly-Si layer properties), annealing conditions for layer crystallization, dielectric deposition for passivation and poly-Si hydrogenation, metallization by screen-printing (paste properties, screen design, printing parameters), and firing conditions.

Although both types of doping were initially planned to be studied in the project, the focus has mainly been put on the development of *n*-type poly-Si layers. These layers are indeed much more interesting from the industrial point of view currently, since they are readily integrated at the back side of PERT+ or TOPCon solar cells (see Figure 1d), this cell architecture being expected to be the one featuring passivated contacts largely dominating the market in the coming years and with a strong growth potential as well [1]. Figure 6 shows the typical structure of symmetrical test samples used to develop these poly-Si layers.

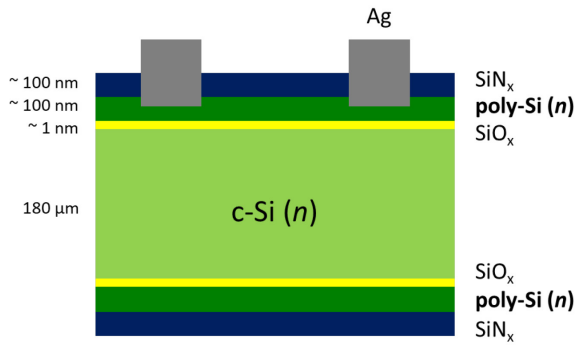


Fig. 6: Schematical structure of a symmetrical test sample used for the development of n-doped poly-Si layers (not to scale).

The doping of poly-Si is a key characteristic to promote excellent surface passivation and carrier extraction. Different approaches were investigated to perform the *n*-doping of sputtered poly-Si layers: in-situ doping using Si:P targets, and ex-situ doping either plasma-assisted or with subsequent $POCl_3$ diffusion. It is observed that enough active phosphorous in the poly-Si is required to achieve good passivation and carrier extraction levels, with very promising values of iV_{oc} above 735 mV and ρ_c ~2 mΩ·cm^2 at best (Figure 7). Regarding in-situ doping, in view of the ECV profiles measured for the studied conditions (Figure 8), shifting from a 2% to a 4% P-content in the Si:P target has a strong impact: the concentration of active P dopants in the sputtered layer increases from $3 \cdot 10^{19}$ to $4 \cdot 10^{20}$ cm^{-3}. This clearly results in improved iV_{oc} and ρ_c values up to 3% P-content, with a decrease in passivation beyond (increased recombination in c-Si with the 4% target). Best results with in-situ doping are on par with ex-situ approaches, pointing towards the requirement for P dopant concentration in the poly-Si layer of at least 10^{20} cm^{-3} and an optimum of 3% for the P-content in the Si:P target for practical solar cell applications. It can be noted that, industrially speaking, in-situ doping is the most convenient approach, as it does not

require any extra equipment or process step. Doping with $POCl_3$ diffusion is however also an interesting alternative, as most of cell manufacturers already possess tube furnace in their production lines.

As a first demonstration, PERT+ solar cells were fabricated with the implementation of a sputtered *n*-type poly-Si layer at the back side, using plasma-assisted ex-situ doping in this case. A certified efficiency of 22.8% was obtained on a full-area 6-inch solar cells, as shown in Figure 9. A detailed loss analysis showed that main limitations come from the non-optimized front side of the device (which is out of control of CSEM, being provided by an external industrial partner), the actual sputtered backside being potentially able to provide efficiencies up to 24.8% [8]. Similar efficiencies are expected with the latest in-situ doped layers according to the results of Figure 7, but their implementation in solar cells still remains to be done.

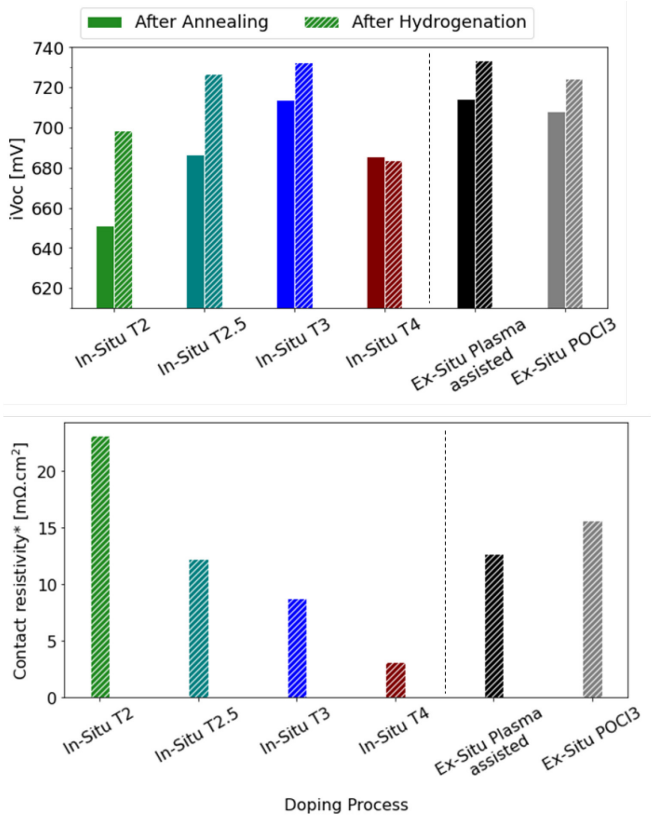


Fig. 7: Dependence of the iV_{oc} (top) and ρ_c (bottom) of wafers symmetrically coated with sputtered n-doped poly-Si, on the doping approach of the poly-Si: in-situ doping with Si:P targets containing various P-content (from 2% to 4%), ex-situ doping plasma-assisted or with $POCl_3$ diffusion. Values are given right after the annealing of the sputtered layers and after hydrogenation. Note that ρ_c* values are over-estimated compared to ρ_c due to absence of poly-Si etch-back between the TLM pads and isolation of the TLM pattern.*

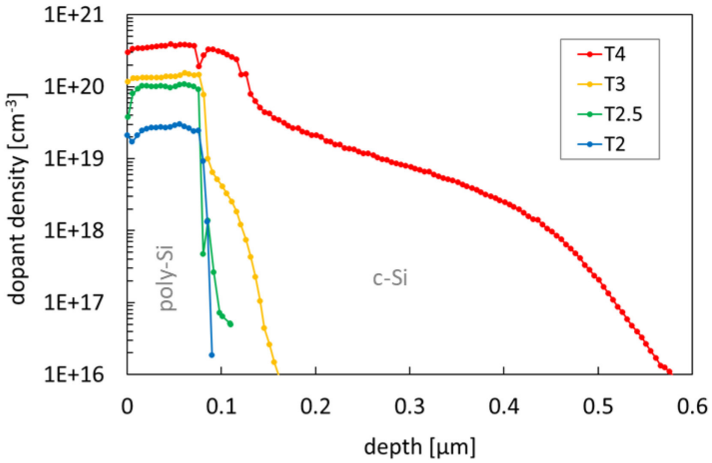


Fig. 8: Dependence of phosphorus profiles of poly-Si layers and surface region of the Si wafer measured by ECV on the P-content of the Si:P target used for the sputtering (from 2% to 4%), after annealing at 900°C and hydrogenation. Measurements start at the surface of the poly-Si layers.

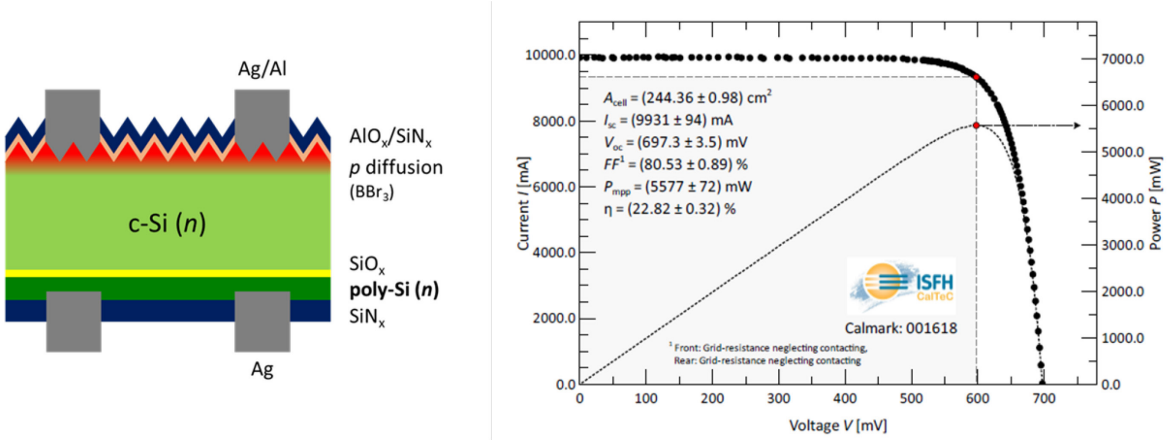


Fig. 9: (Left) Schematic structure and (Right) certified IV curve and main IV parameters of a 6-inch PERT+ solar cell featuring a passivating contact on the rear, formed by sputtered n-doped poly-Si.

In addition to the deposition of poly-Si layers, sputtering could also be used for other HTPC cell process steps. The first example is the formation of the tunnel SiO_x layer. Usually grown by wet chemistry, forming this crucial layer in the same system than the poly-Si could be industrially advantageous, as it simplifies the process flow (see section 6 for details). Note that many TOPCon manufacturers in China are also working toward using the same PECVD or LPCVD tool to deposit the tunnel SiO_x layer. At CSEM, SiO_x has been deposited by reactive sputtering, introducing O_2 in addition to Ar during the sputtering process using an intrinsic Si target. Interestingly, the process time can easily be kept under 10 seconds for such a thin layer, emphasizing the industrial relevance of this method. Passivation and carrier extraction properties of passivating contacts implementing sputtered and chemically formed SiO_x were directly compared. Using same poly-Si layers, similar levels of iV_{oc} and ρ_c have been measured, with values around 715 mV with sputtered SiO_x after hydrogenation (Figure 10), demonstrating the relevance of this approach.

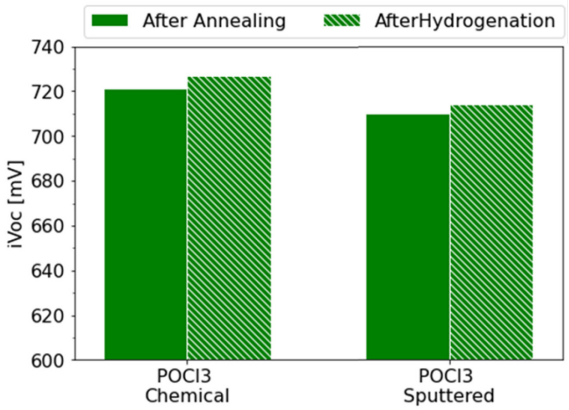


Fig. 10: Dependence of the iV_{oc} of symmetrical test structures on the tunnel oxide formation method, after annealing and after the hydrogenation process.

The second example is the formation of the boron emitter at the PERT+ cell front side, which could also be performed by sputtering and annealing instead of the standard BBr_3 diffusion. Experiments were done using co-sputtering with an intrinsic Si target and a B_2O_3 target simultaneously, for the deposition of a B-rich SiO_x layer. As the sputtering power can be set independently on the two targets, the B-content in the deposited layer can be controlled precisely and B profiling across the layer thickness can also be done if required. After deposition, the layer was annealed at > 900°C to diffuse B atoms in the c-Si bulk and to form the emitter region. In order to passivate the emitter surface with dielectric layers (AlO_x and SiN_x usually), a complete etch-back of the B-doped SiO_x layer is needed beforehand. This was done in an HF solution. Figure 11 shows resulting profiles of active B dopants in the wafer. The properties of the emitter (doping level, depth) can easily be tuned with the sputtering deposition parameters and annealing conditions. Sheet resistances measured on these emitters are found to be well suited for actual solar cell applications. In terms of process integration, this method can potentially lead to a very interesting industrial process flow for PERT+ solar cells, as sputtered Si layers of both doping types could be deposited in the same tool for the emitter (front side) and the back HTPC layer formation, with a single annealing step afterwards.

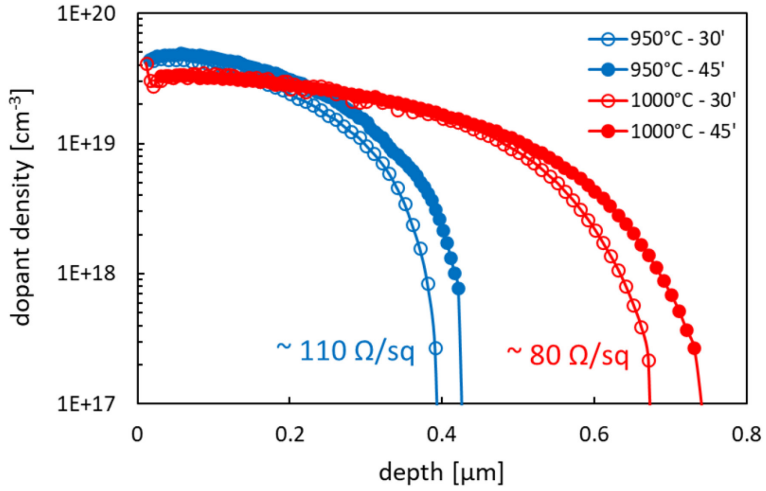


Fig. 11: ECV profiles of boron emitters formed by annealing of a p-type Si layer co-sputtered from an intrinsic Si target and a B_2O_3 target, for various annealing conditions. Corresponding emitter sheet resistance values are given in the graph.

Following the results obtained on the ClusterLine presented above, the following specifications and priorities were defined for the upgrade of the Octopus II machine:

- Addition of a DC rotary magnetron (most relevant for mass production compared to planar);
- Main focus on *n*-type poly-Si layers (most industrial interest compared to *p*-type ones);
- In-situ doping preferred (most convenient doping method);
- Ideal choice for target: Si:P rotary target, with sufficient doping level (3% P-content);
- Fallback option for target (Si:P too difficult to manufacture in practice): intrinsic Si rotary target, with a solution for *n*-type in-situ doping;
- *N*-type in-situ doping: installation of an additional PH_3 gas line, allowing for doping profiling as well;
- *N*-type ex-situ doping options: plasma-assisted or with $POCl_3$ diffusion, post-deposition.

4.2 Process transfer and upscaling on industrial tool

One major requirement for any industrial thin film deposition equipment is a good uniformity of the deposited layer thickness over the substrate surfaces. In this context, in-line sputtering systems with rotary targets have an advantage compared to closed-reactor batch systems, since the movement of the substrates under the target during sputtering allows for a very good uniformity along the displacement axis. Sputtering processes were transferred from the ClusterLine to the Octopus II reactor, and the first step was therefore to qualify the deposition uniformity. Figure 12 shows a thickness mapping measured by spectroscopic ellipsometry on four co-processed wafers, after the deposition of an intrinsic a-Si layer of roughly 100 nm. Excellent layer thickness uniformity is demonstrated (>98%).

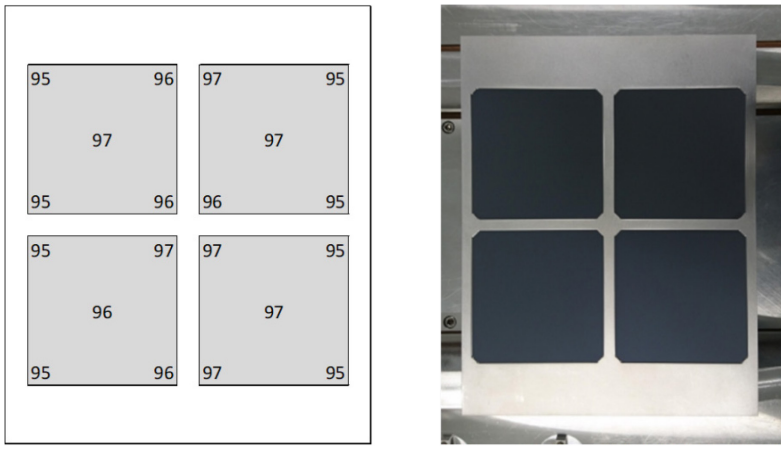


Fig. 12: (Left) Thickness uniformity mapping in nanometers of a ~100 nm sputtered poly-Si layer, measured on five locations across the surfaces of the four 6-inch wafers placed in the carier-plate; (Right) corresponding picture of the wafers in the carrier-plate.

In addition to thickness, the uniformity of HTPC properties (passivation, contact resistivity) is obviously also important for practical solar cell applications. Validation of the poly-Si process transfer and upscaling was done on four co-processed symmetrical test samples, passivated with poly-Si layers deposited in the Octopus II (*n*-type plasma-assisted ex-situ doping in this case). A good passivation uniformity was verified (Figure 13), with average iV_{oc} and ρ_c* values of 720 mV and 8 mΩ·cm^2, respectively. These

results are at a similar level than those obtained with the R&D sputtering tool, demonstrating a successful process transfer. It shows also that the Si material quality of the rotary target is well suited for HTPC applications (sufficiently low density of metallic impurities), and that possible cross-contamination issues coming from the other targets installed on the machine (TCO and metals) are well controlled.

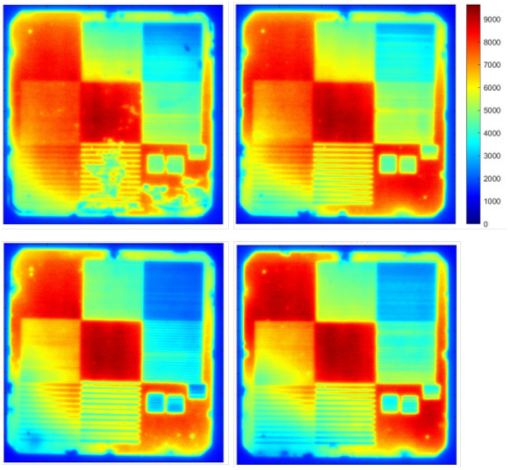


Fig. 13: PL imaging of four co-processed symmetrical test samples. The PL non-uniformity in each wafer bottom left corners is not related to sputtering but due to other high-temperature process steps.

Even if the Octopus II is not a real mass production tool, the data gathered from the developed processes on this machine are nevertheless useful to estimate a potential throughput in a real industrial environment. Based on the actual deposition rate measured on the Octopus II with a typical Si sputtering process and using simple upscaling assumptions (deposition rate linear with sputtering power, maximal power density of 6 W/cm^2 for a Si target, typical dimensions of a mass production rotary target of 2 m in length and 16 cm in diameter), it can be estimated that a throughput of about 12'000 wafers per hour could be feasible (M10 size wafers, 100 nm thick poly-Si layer). Even if some machine down-time must be added for maintenance and target replacement (not considered in this simple estimation), sputtering appears thus to be competitive compared to standard deposition methods for poly-Si layers (LPCVD or PECVD). Since it is extremely difficult to obtain precise cost data from actual companies developing HTPC cell processes and equipment manufacturers, a precise cost comparison for CAPEX and OPEX between these different deposition methods could unfortunately not be made.

4.3 New developments on industrial tool

The addition of PH_3 to the Ar sputtering gas is a unique feature of the Octopus II tool, permitting new developments compared to the R&D tool for *n*-type in-situ doping. As the PH_3 flow can be controlled independently, this doping method is highly relevant as it allows for dopant gradient and precise profiling across the layer thickness, if needed. As shown in Figure 14, the PH_3 flow has a clear and direct impact on the doping level of the poly-Si layer, as expected. The experimental range of PH_3 flow available on the machine is well adapted, as it permits to obtain active dopant densities from 10^{18} to 10^{21} cm^{-3} in the layer (targeted values for HTPC are typically in the 10^{20} – 10^{21} cm^{-3} range). Whereas the poly-Si layer doping – and hence the contact resistivity – is directly correlated to the PH_3 flow, the dopant in-diffusion in the c-Si bulk – and hence the surface passivation – appears to be strongly dependent on the annealing conditions. For example, it is observed that changing the annealing temperature from 850 to 900°C for a given PH_3 flow strongly affects the diffusion depth (open and closed yellow symbols in Figure 14). Therefore, the contact and passivation properties of the contact formed with this method can be independently and finely optimized by adjusting the PH_3 flow and the annealing conditions, which is of high practical interest.

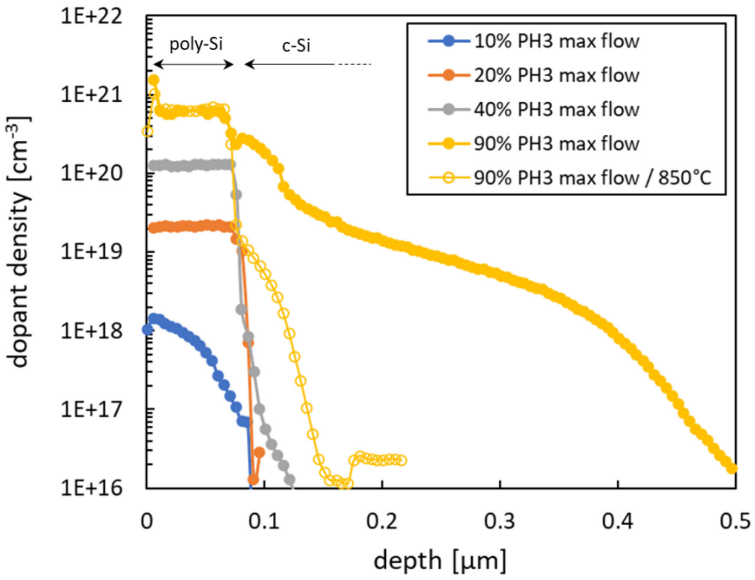


Fig. 14: Active phosphorus profiles of poly-Si layers and surface region of the Si wafer for various PH_3 gas flows used during sputtering, measured by ECV after annealing. Unless stated otherwise, annealing temperature is 900°C.

Promising results were obtained with PH_3 in-situ doping, with iV_{oc} values above 710 mV and ρ_c* values below 5 mΩ·cm^2 (Figure 15). As explained above, these data clearly shows that both PH_3 flow and annealing conditions drive passivation and contact properties: losses in iV_{oc} occur with too high PH_3 flows and/or annealing temperature (too deep in-diffusion leading to increased recombination in c-Si), whereas ρ_c decreases with increasing PH_3 flow and/or annealing temperature (better contact with high surface doping). Further optimization of process parameters is still on-going, with significant room for improvement. These poly-Si layers in-situ doped with PH_3 are the best candidates for implementation at the rear side of PERT+ solar cells, and will be tested soon in complete devices.

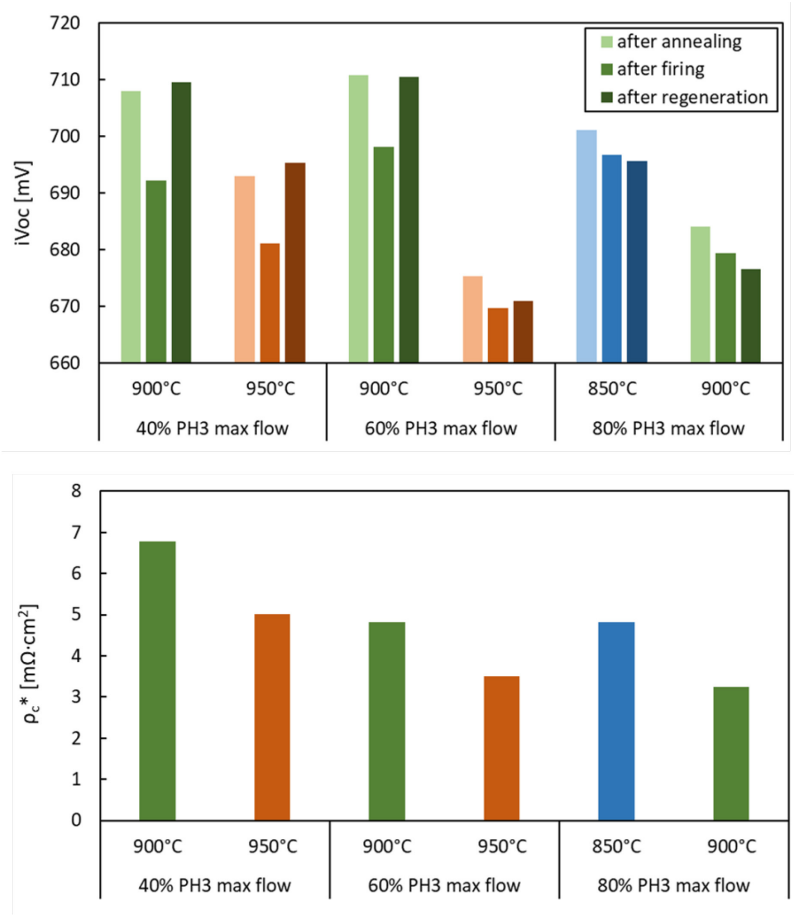


Fig. 15: iV_{oc} (top) and ρ_c (bottom) of symmetrical test wafers coated with n-doped poly-Si layers sputtered with various PH_3 gas flows, and annealed at 850, 900 or 950°C.*

In addition to the development of *n*-type poly-Si layers, a few experiments were dedicated to investigate the feasibility of *p*-type layers in the Octopus II tool as well. As no *p*-type dopant is available in-situ, plasma-assisted ex-situ doping was used for these tests on intrinsic sputtered poly-Si layers. Whereas contacting properties still need to be evaluated, good passivation was already obtained with iV_{oc} values up to 720 mV, demonstrating a proof-of-concept for *p*-type HTPC with sputtering.

4.4 Project objectives assessment

In this section, the fulfillments of the various project objectives are briefly assessed and commented.

- *Upgrade of the Octopus II semi-industrial PVD reactor and infrastructure at CSEM with a new magnetron and a silicon rotary target, allowing for large-area depositions by sputtering of intrinsic and in-situ doped silicon layers;*

→ Fully achieved. Despite technical problems and delays, the upgrade was finally fully completed during the project. CSEM possess now a unique pilot tool for sputtered HTPC layers, with the option of *n*-type in-situ doping with PH_3 gas.

- *Transfer of the best-known sputtering processes for HTPC, previously developed at EPFL/CSEM in a R&D tool, to the Octopus II reactor;*

→ Fully achieved. Sputtering processes with excellent layer uniformity were demonstrated, and passivation and contact properties of *n*-type ex-situ doped HTPC are at a similar level than in the R&D sputtering tool (iV_{oc} ~720 mV, ρ_c* ~8 mΩ·cm^2).

- *Thorough optimization of these processes, to fabricate high-quality HTPC layers characterized by implied open-circuit voltages (iV_{oc}) > 730 mV and contact resistivities (ρ_c) < 1 mΩ·cm^2 for n-type doping (measured on symmetric test samples);*

→ Partly achieved. New developments were made in the last part of the project to optimize poly-Si layers in-situ doped with PH_3. Despite promising results already suitable for implementation in actual solar cells and with still a large room for improvement, best measured properties are nevertheless slightly below these targets (iV_{oc} ~710 mV, ρ_c* ~5 mΩ·cm^2).

- *Demonstration of the high-throughput potential of the developed sputtering processes, targeting 6000 wafers/hour once implemented in mass production equipment;*

→ Fully achieved. Based on measured deposition rates in Octopus II tool and with simple upscaling assumptions, one can estimate a potential throughput up to 12'000 wafers/hour in a mass production environment, demonstrating that sputtered HTPC may be competitive with existing deposition techniques.

- *Fabrication of full-area 6" PERT+ solar cells featuring sputtered HTPC at their back sides, with efficiencies > 24%;*

→ Not achieved. Due to delays related to the hardware upgrade in the first part of the project, the latest developed poly-Si layers could not be implemented in solar cells during the project itself. CSEM will nevertheless exploit the results of the project and fabricate in the coming months PERT+ cells featuring poly-Si layers sputtered in the Octopus II tool. In view of the achieved layer properties and based on results obtained with the R&D sputtering tool (22.8% efficiency with potential up to 24.8%, with a similar *n*-type poly-Si layer), cell efficiencies above 22% at least could be expected soon.

- *Calculations of Cost of Ownership (CoO) for the developed technology, and definition of a roadmap for its further industrialization based on the small pilot line established at CSEM at the end of the project.*

→ Partly achieved. As it will be described in section 6 below, possible advanced cell structures and cell fabrication process flows using sputtering for the formation of HTPC can be envisaged, giving a general roadmap for sputtered HTPC. Concerning CoO calculations, quantitative estimations could unfortunately not be done due to the lack of available data from companies regarding cost of the various equipment and processes involved. Simplification of existing process flows are however realistically possible with sputtering, as commented in section 6.

5 Conclusions

The results of the DELAPS project have demonstrated that sputtering is a versatile and competitive deposition method in the frame of the fabrication of crystalline silicon solar cells featuring HTPC. High-quality poly-Si layers of both doping types can be formed by sputtering with several possible approaches for their doping, be it in-situ (using a doped-Si target, or with dopant precursors in the sputtering gas) or ex-situ (i.e. post-deposition, plasma-assisted or with dopant diffusion). The control of the sputtering process parameters allows for a high tunability of the HTPC layer properties, which is of great importance for the optimization of both passivation and carrier extraction at the same time. In addition to the poly-Si layers themselves, sputtering can also be efficiently used for other cell process steps, such as the formation of the tunnel oxide or the front-side diffused emitter.

This project has also shown that sputtering is highly relevant in a mass production environment, as R&D processes can be successfully upscaled and transferred to in-line sputtering tools, with a high throughput potential. In this context, the demonstration of processes in the pilot semi-industrial Octopus II reactor equipped with a rotary Si target and with in-situ doping is the major achievement of the project. Even if full cell processes could not be developed in the timeframe of the project as initially planned, the promising technological bricks obtained show nevertheless that the HTPC cell fabrication process could be greatly simplified at the industrial scale with the introduction of sputtering. With this unique pilot tool developed in the frame of the DELAPS project, CSEM will exploit further these results and will continue to develop HTPC cell sputtering processes to advertise and show the industrial potential of this technological approach.

6 Outlook and next steps

Considering the very fast pace of industrial progress on the HTPC solar cell technology seen in recent years, especially in China, the implementation of sputtering in current production lines for relatively simple cell architectures like PERC+ or PERT+ seems nowadays unlikely. Indeed, companies are currently establishing lines of several tens of gigawatt capacity with more conservative approaches for the deposition of poly-Si layers, mainly tube PECVD and LPCVD to a lesser extent. However, sputtering could still be relevant in the medium term, particularly for more advanced cell structures yielding higher efficiencies as those described in Figure 16, giving a general roadmap for the sputtered HTPC technology.

The first example is solar cells featuring HTPC on both sides (Figure 16a). For such devices, sputtering could significantly simplify the global cell process flow in comparison with LPCVD or PECVD, as shown in detail in Figure 17. As already mentioned, the main asset of sputtering in this context is its high directionality, resulting in the absence of wrap-around parasitic a-Si deposition on the wafer edges that need otherwise to be etched away by a wet chemistry step. Additionally, the possibility to deposit the tunnel oxide also by sputtering in the same tool represents another interesting feature. This way, the two crucial steps for the formation of HTPC on both sides (SiO_x and a-Si deposition) could be elegantly done in one single tool with targets installed for top and bottom depositions, saving significant processing time and costs compared to the conventional approach.

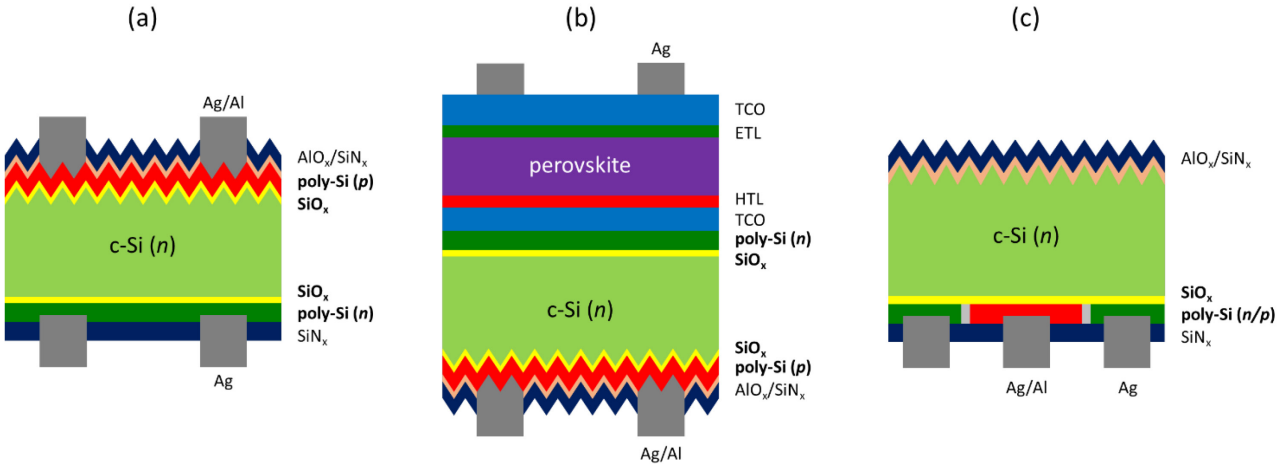


Fig. 16: Advanced solar cell structures featuring HTPC: (a) cell with both-sides HTPC, (b) perovskite/silicon tandem, with bottom cell featuring both-sides HTPC, (c) IBC cell with HTPC.

It has to be noted that, to be competitive in efficiency, the cell structure depicted in Figure 16a would require a localization of the front poly-Si layer to be present only under the metallized fingers, in order to reduce light parasitic absorption in the front side. This would slightly complexify both process flows of Figure 17, but probably once more in favour of the flow using sputtering. Again, thanks to the directional nature of this deposition method, one could imagine to simply use mechanical shadow masks to efficiently localize the front a-Si deposition. However, recent progress made on B emitter and fine line screen-printing have considerably improved the performance of simpler cell structure like PERT+ and would represent a challenge for cells with both-sides HTPC and localized front poly-Si to be economically competitive with them.

The second advanced cell structure under development nowadays is the perovskite/silicon tandem architecture, as shown in Figure 16b. Even if large-area perovskite deposition and layer stability still represent a challenge, promising efficiencies over 30% are theoretically possible on industrial devices.

Since the c-Si bottom cell structure is very similar to the one of the cell with both-sides HTPC, all the advantages previously described brought by sputtering in the cell process flow remain valid.

Finally, the third possible evolution of cell structure is the IBC architecture, with both HTPC localized at the cell back side (Figure 16c). Conventionally made by complex and costly processes like photolithography, the patterning of the back poly-Si layers could advantageously be done during the deposition itself by shadow masks if sputtering is used, as mentioned above. Another process simplification could eventually be made with the tunnel recombination junction concept requiring only one masking step, as it was demonstrated in the case of IBC silicon heterojunction solar cells [9], but this approach remains nevertheless to be investigated with poly-Si layers. For the HTPC IBC application also, it appears therefore that sputtering could be industrially relevant as well in the future.

As a final and general comment, it turned out in recent years that competing with industrial Chinese companies in the “cell efficiency race” actually became extremely difficult for research institutes like CSEM or EPFL, as the huge cell production capacity of these companies gives them a massive advantage. The role of research institutes appears nowadays probably slightly different than a few years ago, shifting from being leaders in manufacturing record efficiency devices to being developers of innovative technological bricks that are later implemented by industrial solar cell companies. In this context, even though the cell efficiency objectives were not achieved, the outcome of the DELAPS project can however be considered as successful, as it triggered interest from some industrial potential customers of CSEM.

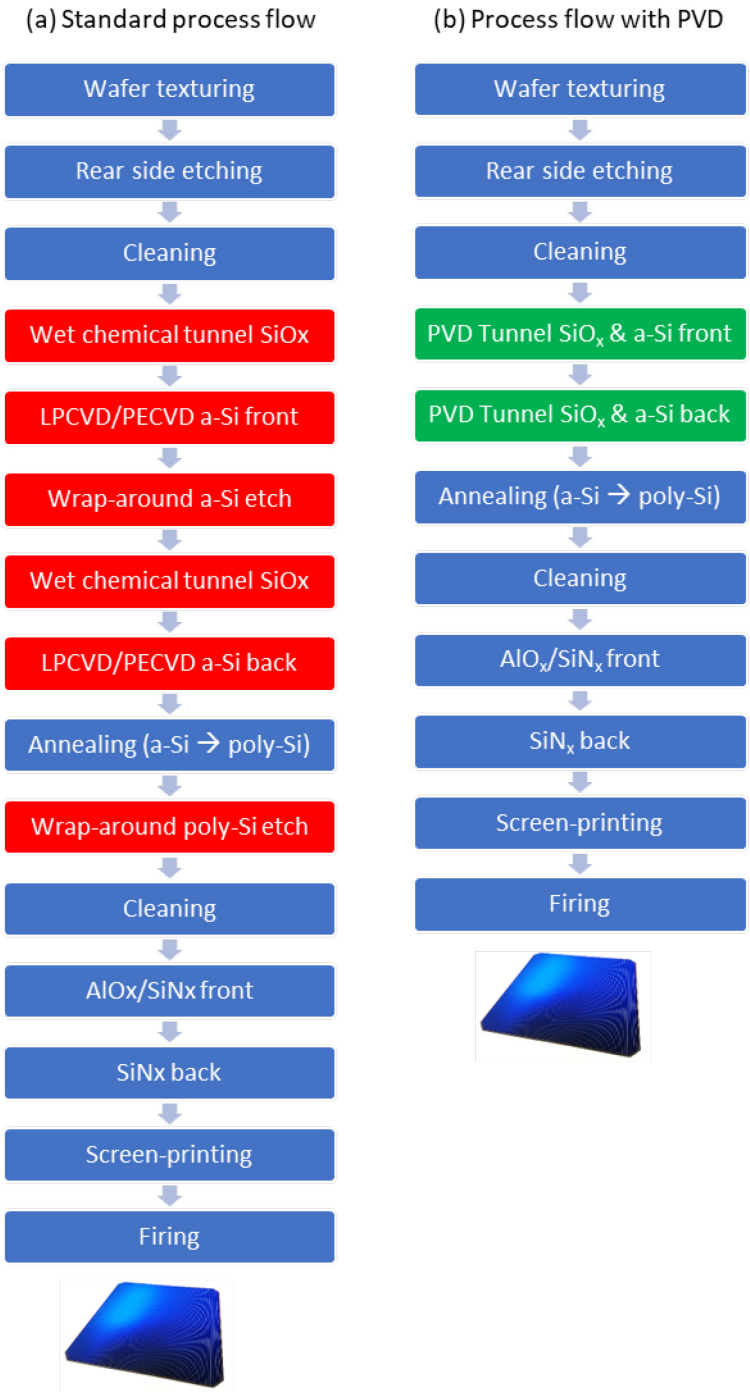


Fig. 17: Possible cell fabrication process flows for devices with both-sides HTPC, (a) with poly-Si deposition by LPCVD or PECVD, (b) with tunnel oxide formation and poly-Si deposition by sputtering (PVD).

7 National and international cooperation

Whereas CSEM was the only partner directly funded by SFOE for this project, several companies in Switzerland and in Europe were indirectly involved as well in the technical developments made, particularly for the hardware upgrade. As the manufacturer of the Octopus II machine, INDEOtec in Neuchâtel was obviously strongly involved in this project for the integration of the new magnetron, the required automation and software modifications and carrier plate fabrication. The construction of the magnetron itself was subcontracted. Concerning the target manufacturing, some specific small size targets for the ClusterLine (Si:P with various doping levels, B and B_2O_3) as well as the development of the large-area Si rotary target were done in collaboration with European companies. As these targets are made of highly non-standard materials and are technically very challenging to fabricate, a good cooperation has been established between CSEM and these companies in order to progress as much as possible on this critical topic.

8 Communication

The main achievements of the project have been publicly disseminated in national and international scientific conferences and meetings, as listed in section 9 below.

9 Publications

A. Descoeudres, C. Allebé, P. Wyss, C. Ballif, B. Paviet-Salomon, “Sputtered poly-Si layers for the formation of *n*- and *p*-type passivating contacts” (oral presentation), *40th European Photovoltaic Solar Energy Conference and Exhibition (EU PVSEC 2023)*, September 2023, Lisbon, Portugal.

A. Descoeudres, C. Allebé, P. Wyss, C. Ballif, B. Paviet-Salomon, “Sputtered poly-Si layers for the formation of front and rear passivating contacts of perovskite/silicon tandem’s bottom cells” (poster), *13th International Conference on Crystalline Silicon Photovoltaics (SiliconPV) and 12th nPV workshop*, April 2023, Delft, The Netherlands.

A. Morisset, C. Allebé, A. Descoeudres, J. Hurni, S. Libraro, E. Genc, F.-J. Haug, B. Paviet-Salomon, C. Ballif, “Development of passivating contacts using cost-competitive deposition method for high-efficiency silicon solar cells” (poster), *21. Schweizer Photovoltaik-Tagung (PV Tagung)*, March 2023, Bern, Switzerland.

C. Allebé, A. Descoeudres, P. Wyss, P. Boillat, N. Pernès, B. Paviet-Salomon, C. Ballif, "Sputtering for the formation of Si-based passivating contacts", *IEEE J. Photovoltaics*, to be published.

10 References

[1] *International Technology Roadmap for Photovoltaic (ITRPV)*, www.vdma.org/international-technology-roadmap-photovoltaic (2023).

[2] A. Richter et al., *Nat. Energy* **6**, 429-438 (2021).

[3] F. Haase et al., *Solar Energy Materials & Solar Cells* **186**, 184-193 (2018).

[4] Y. Chen et al., *Prog. Photovolt. Res. Appl.* **31**, 1194-1204 (2023).

[5] Jinko Solar, www.pv-tech.org/jinkosolar-lays-claim-to-n-type-topcon-cell-efficiency-record-of-26-1/

[6] Jollywood Solar, www.jolywood.cn/en/NewsDetails-368-1104.html

[7] LONGi, www.pv-magazine.com/2021/06/02/longi-achieves-25-21-efficiency-for-topcon-solar-cell-announces-two-more-records/

[8] A. Ingenito et al., *Sol. Energy Mater. Sol. Cells* **249**, 112043 (2023).

[9] A. Tomasi et al., *Nature Energy* **2**, 17062 (2017).