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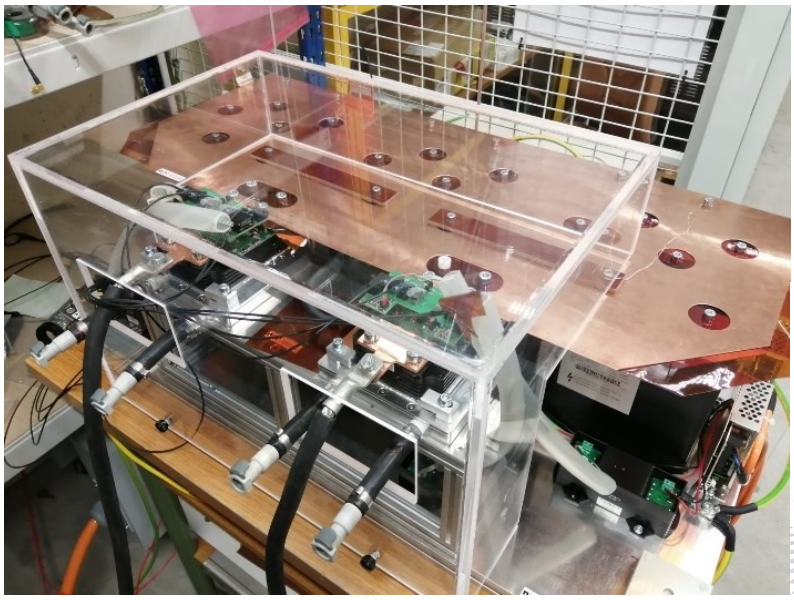
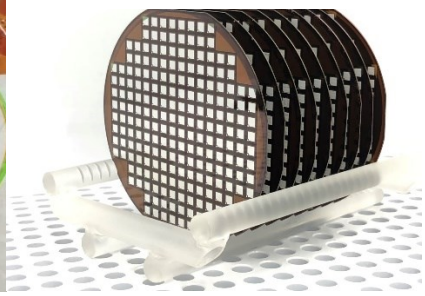
**Swiss Federal Office of Energy SFOE**
Energy Research and Cleantech Division

**Interim report dated** 13.10.2022

# SiC-MILE

## SiC Medium Voltage Devices





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# Zusammenfassung

Die Entwicklung neuer Technologien zur Reduzierung weltweiter Energieverluste ist heute eines der Hauptziele. Eine ausgezeichnete Strategie, um ein solches Ziel zu erreichen, besteht darin, auf Technologien zu zielen, die in elektronischen Hochleistungswandlern verwendet werden, da ein erheblicher Teil des globalen Energieverbrauchs mit diesen Systemen zusammenhängt. Mittelspannungs-Stromrichter weisen solche Eigenschaften auf, die zur Steuerung von Motoren verwendete Mittelspannungsantriebe haben einen enormen weltweiten Einfluss, da etwa 60 % des weltweiten Energieverbrauchs von Motoren stammen. Siliziumkarbid (SiC) ist ein Schlüsselmaterial, das im Kern von Energiesystemen (z. B. MV-Antrieben) verwendet wird und das Potenzial hat, die globalen Energieverluste stark zu reduzieren. Der SiC-Markt erreichte 2019 etwa 500 Millionen US-Dollar, wobei bis 2025 ein Umsatz von 2,5 Milliarden US-Dollar prognostiziert wird. Obwohl EV-Technologien einen erheblichen Teil des Wachstums im LV-Bereich ausmachen, wird sich die MV-SiC-Technologie in einer Reihe von Anwendungen erheblich weiterentwickeln.

Diese Technologie hat das Potenzial, den Energieverbrauch in der Schweiz und weltweit stark zu senken, indem Energieverluste für industrielle Antriebsanwendungen um bis zu 540 TWh reduziert werden. In der Schweiz werden Energieeinsparungen für industrielle Antriebsanwendungen erwartet, die 2,6 % des jährlichen Landesverbrauchs entsprechen. Zudem sollen bei einer Prognose von 25 Jahren Produktlebensdauer rund 6,8 Milliarden Franken eingespart werden.

Das SiC-MILE-Projekt zielt darauf ab, eine Technologie zu etablieren, die die zukünftige Entwicklung von SiC-MOSFET-Produkten für Mittelspannung (MV) ermöglicht, wobei der Schwerpunkt auf den Spannungsklassen 3,3 und 6,5 kV liegt. Es werden Leistungsmodule entwickelt, die auf MS-Hochleistungsanwendungen wie Bahnstromrichter und Industrieantriebe abzielen. Es wird erwartet, dass eine solche Technologie die Konstruktion von Leistungswandlern mit bemerkenswerten Energieeinsparungen und erheblichen Gewinnen hinsichtlich Kompaktheit und Gewicht ermöglichen wird.

Das Design der 3,3-kV-SiC-Chips sowie das Packaging wurden in diesem Bericht detailliert beschrieben. Darüber hinaus wurde der Bau eines dedizierten Konverterprüfstands entwickelt, um die Verluste der Si-Leistungsmodule im realen Konverterbetrieb mit hochgenauen thermischen und elektrischen Methoden zu charakterisieren.

1) Simulationen, Prozess und Integration für die Entwicklung von 3,3kV-SiC-Chips, mit einer erfolgreichen Demonstration.

2) EM-Design und Bonding-Prozesse für SiC-basierte LinPak-Gehäuse mit reduzierten Streuinduktivitäten.

3) Demonstration eines Si-Linpak-Konverters einschließlich thermischer und elektrischer Prüfstände zur Charakterisierung.

Das Projekt liegt im Zeitplan und es sind keine Verzögerungen zu erwarten. Im nächsten Schritt werden LinPak-Module aus SiC mit 3,3 und 6,5 kV zusammengebaut und in den jeweiligen Umrichterdemonstratoren getestet. In der Zwischenzeit werden Testtechniken für die Charakterisierung des Systems entwickelt und getestet, einschließlich Methoden, die durch FEM-Simulationen unterstützt werden.

# Summary

Developing new technologies to reduce worldwide energy losses is one of the main objectives nowadays. An excellent strategy to achieve such a goal is to target technologies used in high-power electronic converters since a significant part of global energy consumption is related to these systems. Medium voltage power converters present such characteristics, which medium voltage drives used to control motors present a tremendous worldwide impact, with around 60% of global energy consumption coming from motors. Silicon carbide (SiC) is a key material used in the core of power systems (such as MV drives) with the potential to reduce global energy losses strongly. The SiC market reached about 500M US$ in 2019, with the forecast to reach 2.5B US$ by 2025. Although EV technologies push a significant part of the growth at the LV range, MV SiC technology will significantly develop in a series of applications.

This technology has the potential to strongly reduce energy consumption in Switzerland and world-wide by reducing energy losses by up to 540 TWh for industrial drive applications. In Switzerland, it is expected energy savings for industrial drive applications that correspond to 2.6% of the annual country consumption. Additionally, considering a 25 years product lifespan prediction, around 6.8 billion Swiss francs are expected to be saved.

The SiC-MILE project aims to establish a technology to enable the future development of medium voltage (MV) SiC MOSFET products, focusing on the 3.3 and the 6.5 kV voltage classes. Power modules will be developed targeting MV high-power applications, such as railway traction converters and industrial drives. It is expected that such technology will enable the design of power converters with remarkable energy savings and significant gains regarding compactness and weight.

The design of the 3.3 kV SiC chips, as well as the packaging, have been detailed in this report. Furthermore, the construction of a dedicated converter test bench to characterize the Si power modules losses under real converter operations with highly accurate thermal and electrical methods has been developed.

In the first year of the project, SiC-MILE was able to achieve the following results, which are in accordance to the proposed deliverables:

1) Simulations, process and integration for the development of 3.3kV SiC chips, with a successful demonstration.
2) EM design and bonding processes for SiC based LinPak packages, featuring reduced stray inductances.
3) Demonstrator of Si Linpak converter including thermal and electrical based test benches for characterization.

The project is on time and delays are not expected. On the next step, LinPak modules featuring SiC with 3.3 and 6.5 kV will be assembled and tested in its respective converter demonstrators. Meanwhile, testing techniques for the characterization of the system are being developed and tested, including methods supported by FEM simulations.

# Contents

# 1 Introduction

## 1.1 Background information and current situation

The vision of the SiC-MILE project is to establish a technology to enable the future development of medium voltage SiC MOSFET products, targeting the 3.3 and the 6.5kV voltage classes. The material properties of SiC enable the fabrication of power semiconductors with superior on resistance for equivalent blocking voltage, which, in turn, goes well beyond fundamental limit of Si technology, and very high frequency operation. Recently, the SFOE funded project AMPERE demonstrated the first prototypes of SiC MOSFET rated at 6.5 and 10kV at the Hitachi ABB Power Grids (HAPG) Corporate Research Center and the FHNW in Switzerland, reaching a major step towards the implementation of these devices (Fig. 1). The devices rated for Medium Voltage (MV) applications will have a major impact on future electrical energy management by means of medium voltage power electronics, where massive investments will be implemented over the coming decades. This will result in benefits not only for the infrastructure across Switzerland, but also provide a low-cost, low-carbon, and high-robust energy to society.

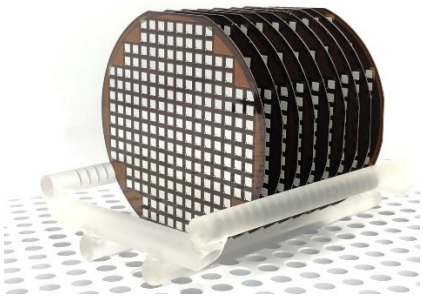


Fig. 1 – SiC MOSFET wafers fabricated from SFOE funded AMPERE project.

Driven by the need of energy efficient technologies for sustainable growth, the market of SiC reached about 500M US$ in 2019 with the forecast to reach 2.5B US$ by 2025, featuring a CAGR of more than 30% in the period (Fig. 2 left). Although a significant part of the growth is pushed by the EV technologies at the LV range, MV SiC technology will significantly develop in a series of applications. From the exemplary market study, MV SiC will correspond to at least 10% of the market. However, those figures are highly underestimated because it assumes low availability of MV SiC products in the market. This technology hindering issue will be tackled in this project, which will speed the time to market of the MV SiC modules up and thus to further increase market share. Figure 2(right) shows the application of SiC technologies and its GaN and Si counterparts for a wide range of conversion power and operating frequencies. MV SiC devices targeted in this project will be implemented in traction, FACTs, HVDC light, wind and MV industrial drives, which is a multi-billionaire market worldwide and heavily present in Switzerland. The availability of SiC MV modules for example will certainly speed up the implementation of new converter technologies into those applications.

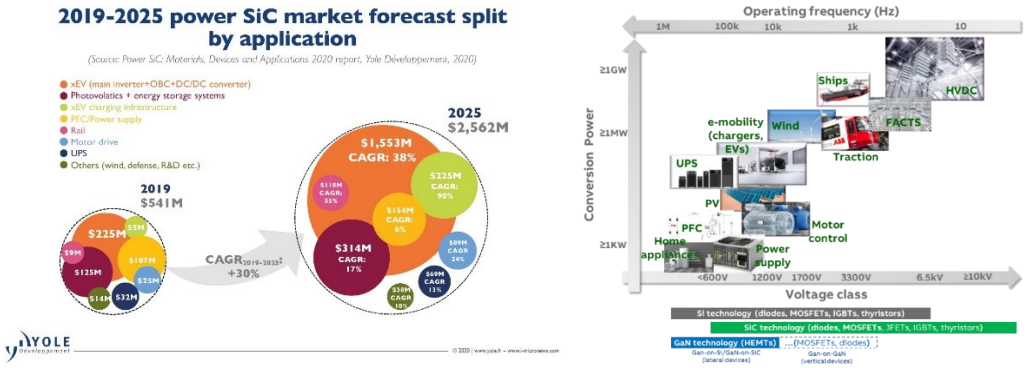



Fig. 2 SiC market forecast (Yole SiC report, 2019 http://www.yole.fr/iso_album/illus_power_sic_marketforecast_yole_nov2020.jpg) (left) Distribution of applications vs. voltage class (lower axis) and operating frequency (upper axis). The applications-related range of Si, SiC and GaN technologies is also shown for comparison (right).

Together with advances in power modules design, the use of SiC technology in rail traction converters leads to remarkable energy savings (up to 30%) as well as significant gains regarding compactness and weight (up to 60%). In wind turbine converters, the use of MV SiC can lead to lower total losses as well as benefits in terms of lower turbine nacelle size and tower heights. For Mega-Watt range applications such as HVDC, the deployment of SiC technology can also deliver substantial benefits in terms of energy efficiency coupled with reductions in size, weight and cost of the power system.
Figure 3 shows the major players in MV SiC technology, indicating that in Europe, Hitachi Energy is the only technology developer. Notice that very large European power semiconductor corporations such as Infineon, STMicroelectronics and ON-semi are not in the market. This is explained by the fact that Hitachi Energy is the technology leader in MV and HV power semiconductors, whose strong position is underpinned by its pioneering on Si thyristor and IGBT technologies. So far, the most explored technology in HAPG is the 3.3 kV class.

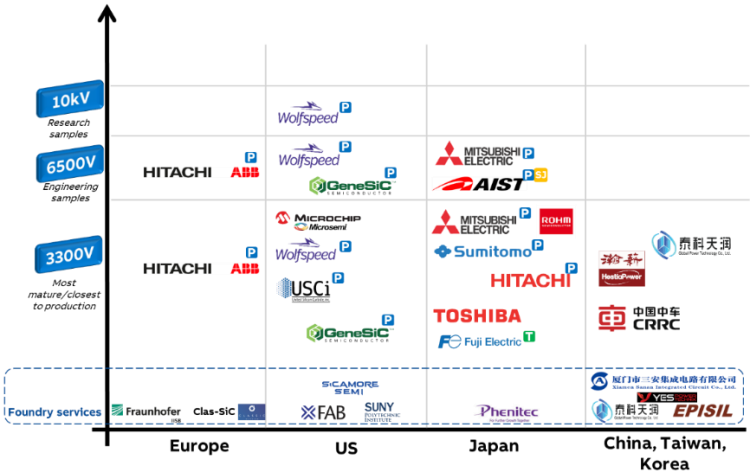



Fig. 3 Map of SiC semiconductor player for voltage ranges of 3.3kV an higher.

Figure 4 depicts a table with all available 3.3 kV technologies in the market and its descriptions from the main competitors of Hitachi Energy. It is important to notice that all those are not commercially available and are on the stage of technology development. Also, most of them reassemble LinPak modules as the new industrial standard.

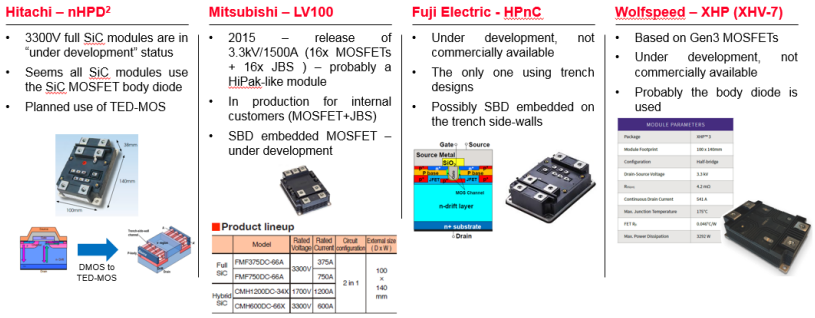



Fig. 4 Summary of 3.3kV full SiC power modules of competitors.

Recently, Hitachi Energy have developed an innovative MOS gate stack technology based on high-k dielectrics for power electronic devices. For the first time, we have successfully demonstrated fully functional vertical power SiC MOSFETs using high-k-based MOS interfaces. The recent results on 1.2kV-rated SiC MOSFETs, showed unrivalled levels of threshold voltage stability during static and dynamic stress operation using Si-like gate voltage swings of +/- 15V.

Through a partnership between the FHNW and Hitachi Energy Semiconductors, SiC-MILE seeks to establish the MV technology platform before moving to a potential product, and thus to enable development of national energy related WBG-based HV power electronics applications. This partnership initially started in the SFOE project - number SI/501529 – Fortgeschrittenes SiC-Material fuer Leistungs-Elektronikgeraete – link: https://www.aramis.admin.ch/Texte/?ProjectID=40193. In this previous project, primary technology platforms for state-of-the-art MV discrete SiC devices have been developed, encompassing simulations, microtechnology processes, integration schemes and characterization systems. In order to achieve the SiC Mile ambitious goals, the FHNW partner with long experience in applied semiconductor devices and power electronics will be technologically backed by Hitachi Energy`s leadership position in high power devices developed in Lenzburg, as well as the unique know-how in power electronics applications from several Swiss-based business units. HAPG, in fact, is a leader in manufacturing of high power IGBTs featuring high performance and reliability, with decades of R&D experience, and thus the right European company to tackle this challenge. The FHNW, in turn, sets high support to energy efficient applied research through its "Energy Chance" strategy, including the hosting of a SCCER-FURIES program, NRP70 research project ("Swiss transformer") and some other SFOE SiC-based research projects.

## 1.2 Purpose of the project

Switzerland is one of the main poles of power electronics technology development in Europe and in the world, which is, in turn, the basis for the vast majority of energy related systems, including rail, renewables, electric vehicles, industrial drives, grid technology and so forth. SiC is the next technology

step in power electronics, which is expected to take over significant market share of its Si counterpart because of its undisputable advantage in energy efficiency. One remarkable example is the use of LV SiC MOSFETs in the new Tesla electric cars, substituting the Si IGBT technology to provide longer all electric range. Whereas the LV SiC market (up to 1.7 kV class) is in full commercialization in renewables and EVs, the MV SiC technology (3.3 to 6.5 kV) is only offered as *development samples*.

The purpose of SiC-MILE is to demonstrate a new generation of 3.3 and 6.5 kV SiC MV chips and packages with required performance, reliability and costs, and to validate them in a converter demonstrator to assess their potential in MV drive applications. The results will be further evaluated for estimating the energy saving potential in Switzerland in traction applications. Such products are not yet available in today's market and its industrialization will further enable the development of new MV applications featuring SiC devices (e.g. MV drives and distributor transformers), which, in turn, will allow significant energy savings.
A significant research and development effort on material processing, microfabrication and process integration must be made to achieve reliable and robust chip designs with optimal performance and yield. Optimized gate oxide stacks to reduce leakage current, optimal epi-layer design to minimize on-resistance, and robust termination designs are some of the state-of-the-art innovations required in this project. Additionally, these chips must be electrically interconnected in a highly optimized power module packaging to achieve ultra-low stray inductances, compactness, equal current ratio sharing between the chips and high robustness and reliability. Implementing new materials for chip-substrate connection (e.g. silver sintering) is one additional innovation to the SiC technology module presented in this project. The SiC Mile project also innovates in designing a customized testbench converter to characterize the power modules under converter operation similar to a real application. Such a test allows the comparison of SiC and Si technologies under identical conditions to accurately depict the WBG technology's potential.

Hitachi Energy Semiconductors is an important supplier of components to other ABB units based in Switzerland, such as Medium Voltage Drives, FACTS and High power rectifiers. Directly after successfully passing technology development phase, first demonstrators will be presented for these end customers. The project will therefore generate nationally further revenues at the application side and help maintain high technology manufacturing in Switzerland. This will speed the development of applications that significantly influence energy efficiency and CO2 emission reduction in Switzerland. As such, the project poses the following relevance:

<u>Technology/scientific relevance:</u>

1. Generation of innovative platforms in SiC based chip/module/converter technology.
2. Impact the development of SiC converter technology in application universities/companies in Switzerland and abroad.
3. Support significant increase of energy efficiency and reduction of CO2 emission in Switzerland as a basis technology for efficient energy systems, for example in traction converters of trains or industrial drives.

<u>Strategic/economic relevance:</u>

1. Supports the technology development at Hitachi Energy semiconductor business unit in Switzerland, which provides more than 350 jobs, and figures as a large exportation company for energy efficient power semiconductors.
2. Enable the development of new SiC products based in Switzerland.
3. Enable the nucleation of a unique supply chain in Switzerland for the development of MV drive products based on SiC, both at Hitachi Energy or ABB Drives.

4. Enable of new system products such as trains or MV industrial drives that will profit end customers.
5. Reduced long-term in-service degradation, lowering maintenance needs and costs of power electronics systems.
6. Smaller power semiconductor players in Switzerland such as SwissSem AG and MQsemi will further profit from the technology output and the SiC market boost in the country, which will further push product demands.

## 1.3 Objectives

The objectives of this project is to demonstrate a new technology of railway power system based on advanced SiC power semiconductors. This technology has the potential to strongly reduce energy consumption in Switzerland and world-wide by reducing energy losses by up 540 TWh for industrial drive applications. In Switzerland, it is expected energy savings for industrial drive applications that correspond to 2.6% of the annual country consumption. Additionally, considering a 25 years product lifespan prediction, around 6.8 billion Swiss francs are expected to be saved.

Specifically, the goal is to demonstrate 3.3 and 6.5 kV SiC MOSFETs chips and packaging modules fabricated in an industrial environment, and to validate the technology in a MV power electronics converter demonstrator with energy conversion efficiency higher than 99%.

Design, processing technology, and development of dedicated measurement systems are within the scope of the project. HAPG will build on these platforms to rapidly accelerate the technology readiness. The specific targets required in order to achieve these ambitious objectives are twofold:

1. To fabricate 3.3 and 6.5 kV SiC MOSFET MV module demonstrators in a Si fab, moving the technology from laboratory to fab (TRL 5 to TRL 7-8). This target requires extremely advanced technology of semiconductor manufacturing that involves interdisciplinary sciences such as Chemistry, Physics, Maths and overall engineering. The targets for the chips and power modules are currents rating of around 300 – 400 A, chip switching losses at nominal conditions smaller than 8 mJ and module stray inductance smaller than 30 nH.

2. The research questions for this target address:

    a) What chip/modules designs can fulfil performance, robustness and reliability required for real industrial applications? Intensive simulation and integration development will be performed to deliver the required specifications.
    b) How processes of a Si fab can be adapted to SiC materials? Incorporation of SiC into high volume Si fabs is paramount to achieve cost viability. Owning the fact that processes are different in several cases over more than 200 steps, there will be significant scientific/engineering work to achieve this target.
    c) How to make SiC cost effective? As aforementioned processes and integrations must be cost optimized in order to compensate for the high costs of SiC substrates.
    d) What are the challenges and advantages of manufacturing SiC from the technology and financial perspectives? The individualities of the technology will be thoroughly assessed.
    e) What are the technology advantages of SiC MOSFET modules compared to those based on Si IGBTs? This research question will provide the basis for the applications of the technology.

3. To build a half-bridge converter demonstrator featuring the 3.3 kV and 6.5 kV SiC module technology. This topology is the building block for power electronics, and provides most of information needed for the assessment of systems. We target a converter demonstrator efficiency of between 96 – 98 % for the Si IGBT converter and > 99% for the SiC MOSFET converter at similar operating conditions. We will then compare their performance under different operations and as such to access their potential performance in railway applications in Switzerland.

4. The research questions for this target are:

    a) What is the SiC module performance in a converter application? $R_{ds}$, Switching losses, rise and fall time module as well as converter metrics such as stability under constant switching, energy losses and efficiency over switching frequency and power range will be assessed as systematically.
    b) What are the performance of the SiC technology under high frequency switching?

Which applications will mostly profit from the MV SiC technology? This research question must be addressed from the technology and financial perspectives using system simulations. Main applications will be assessed in MV VFD and traction converters. 3.3 kV SiC-based railway traction converters applications are expected to present up to 59 % improvement of the electric-energy loss when compared to Si IGBT-based converters, depending on the drive cycle [1].

# 2 Procedures and methodology

The SiC Mile project aims to perform a complete product analysis. The project starts with the SiC chip design and power module assembly. Afterwards, the power converter design and experimental testing of the fabricated modules, followed by energy savings investigation in drive-based applications, is performed. Finally, the life cycle analysis is executed (Fig. 5).

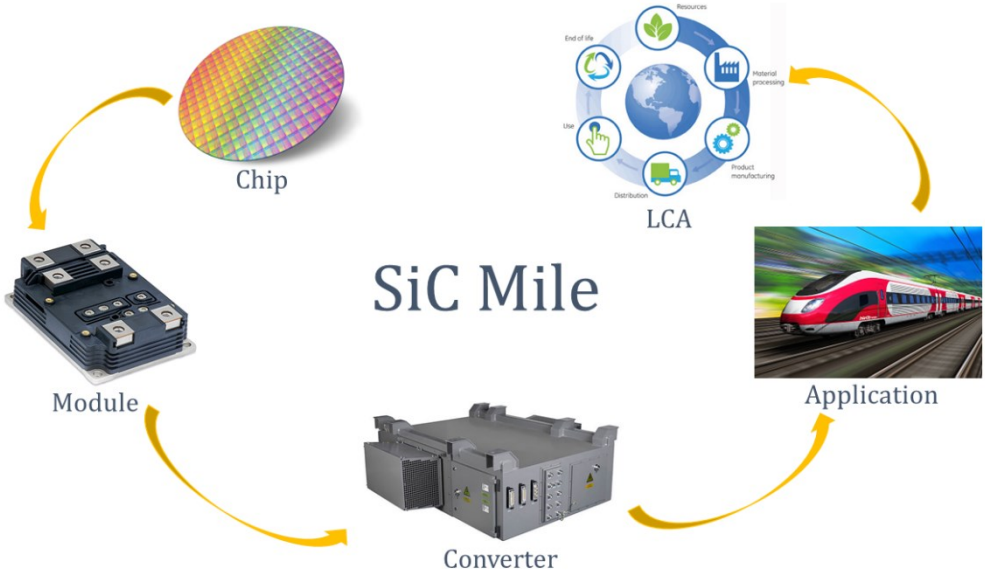



Fig. 5 SiC Mile project methodology overview.

This project flow initially starts with the 3.3 and 6.5 kV SiC chip design and packaging. The focus is initially given to fabrication and integration schemes. Then, the chip design steps are elucidated, focusing on epi-layer design, doping profiles and gate oxide optimization. The packaging design is mainly focused on the module stray inductance optimization.

The second part focuses on designing and constructing of the converter test bench to characterize 3.3 and 6.5 kV Si IGBTs modules. The design considerations and two distinct measurement protocols to characterize the converter power losses (thermal and electrical methods) are presented.
The two testbench converters present the following technical parameters:

1) 3.3 kV Si testbench converter: 1.8 kV operating voltage, a maximum current of 300 Arms, maximum switching frequency of around 2 kHz, driving gate voltage of +15V/-10V and inductor load of 2.5 mH.
2) 6.5 kV Si testbench converter: 3.6 kV operating voltage, a maximum current of 300 Arms, maximum switching frequency of around 2 kHz, driving gate voltage of +15V/-10V and inductor load of 2.5 mH.

The first characterization method is based on the thermal exchange method, in which the inlet and outlet cooling fluid temperature and fluid flow are monitored to provide the module power losses. Such a method can provide high accuracy when accurate temperature sensors are used with state-of-the art flowmeters. In addition, the power loss characterization with power analyzer equipment is also performed. Both methods together provide improved accuracy and reliable results.

# 3 Activities and Results

## 3.1 SiC chip and module development

**Development of integration schemes**

The SiC MOSFET integration process comprises consecutive fabrication modules which must be properly developed and assembled to achieve the desired chip performance and yield. Indeed, each module is formed by subsequent processing steps that are tested and optimized according to well defined learning cycles. The design of the respective learning platform includes the splitting of processing conditions, where the combination of critical variables and development steps is tested in a different way. The assessment of the resulting matrix allows to select optimal conditions according to defined design rules and the targeted specifications for the device. In few cases the learning cycles can still be performed using Si wafers. However, most of them require testing on 150mm SiC wafers, not only substrates, but specifically epi-wafers.

Below is an overview of the main fabrication modules and the foremost learning cycles we have implemented during the SiC MOSFET integration:

| Processing Module | Learning cycle | Goal |
|---|---|---|
| Implantation Hard-Mask | Hard-mask layer stack selection/deposition | Proper screening of implantation species |
| | Hard-mask etch | 90deg etch profile for accurate implantation regions |
| Implantations | Implantation profile | Selection of implantation energies and doses for Channel, Source, P-well, Termination, JFET, Pplus, regions |
| Targets | Targets shape and polarity | Proper alignment of different layers across the process. Critical for right overlapping and desired critical dimensions. Targets must overcome different processing conditions |
| | Targets etch | Targets depth and sidewalls are very important for signal detection and mask alignment in the Lithography tools |
| Lithography | Photoresist coating and develop | Combined with exposure energy it allows to reach the critical dimensions in small size features |
| | Exposure energy | Exposure energy and alignment conditions are key part of accurate overlapping and feature size of different processing steps |
| Self-alignment | Layer deposition and dry-etch | Proper self-alignment for screening channel region during source implantation. Critical for channel length definition |
| Gate Platforms | Gate Oxide surface pre-conditioning | For reducing density of electrically active defects, primary at the interface |
| | Dielectric material and thickness | Integration of dielectric materials with a large permittivity and large band gap |
| | Gate metal contact selection | Low Gate resistivity |
| | Post-depo annealing steps | Improving interplay between Gate metal and Gate dielectric |
| Insulation | Insulation layer stack selection | To ensure proper source-gate insulation |
| | Post deposition treatment | Densification of insulation materials |
| | Layer stack etching | Proper contact opening |
| Ohmic Contact Formation | Metal layer selection and etch | Appropriate source contact region covering while preventing damage of the gate during post deposition anneal |
| | Rapid thermal processing | Formation of ohmic contacts with low resistivity according to proposed specifications |
| Metallization | Metal contact filling | Complete filling of voids at the source contact regions |
| | Wafer Backside metallization | Good adhesion between the SiC ohmic layer and the metallization layer stack |

| | | |
|---|---|---|
| Passivation | Layer selection and deposition | Suitable protection of the transition and termination area mainly from humidity and particles |

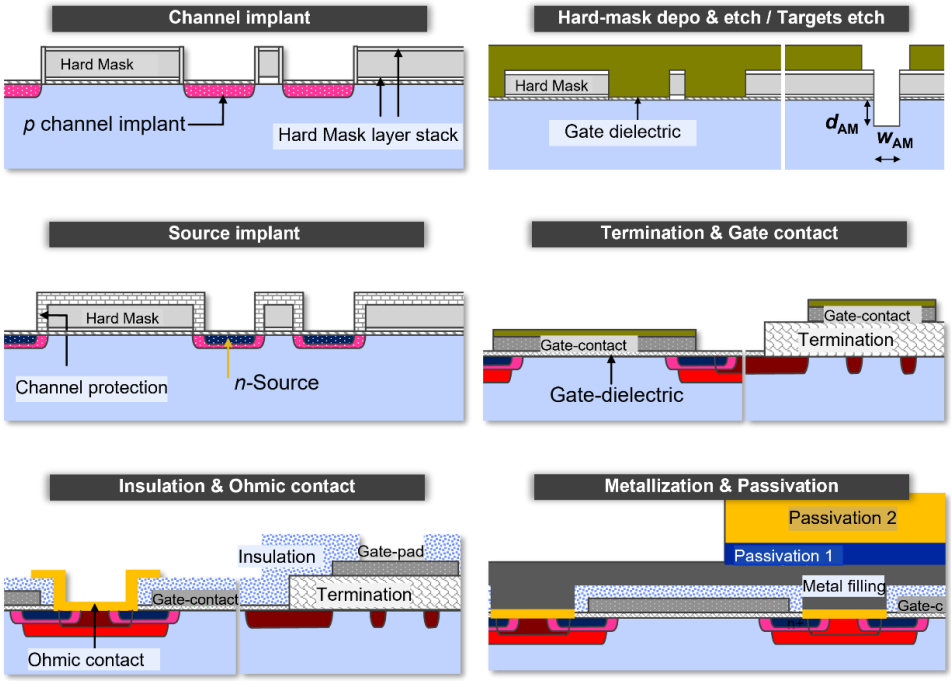



Fig. 6: General overview of most relevant integration steps in the development and manufacturing of SiC MOSFET devices. The different integration steps require several cycles of testing processing conditions and development platforms. The final fabrication router for prototype manufacturing contains about 284 steps.

### Development of fab processes

As mentioned in the proposal, the MOSFET fabrication processes developed in Hitachi Energy PEARL laboratory have been transferred to the CH-SEM Si production line. The active MOSFET cell design is typically defined by implantation and self-aligned processes, which ultimately control the minimum feature size that could be achieved in a controllable and repeatable fashion. Here, we have run many short loops experiments where we mostly verified the following critical steps (as schematically described in fig. 7): ion implantation, self-aligned processing methods, termination are mask etching, gate oxide processing and silicidation of ohmic contacts (both front- and back-side).

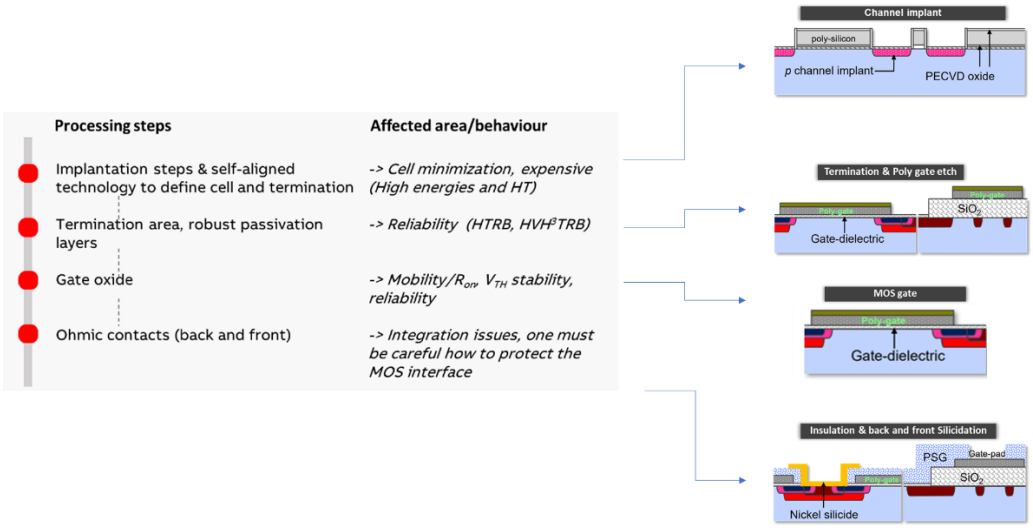



Fig. 7 Schematic chart showing some of the crucial processed needed for the fabrication of a high power SiC MOSFET; schematic cross-sections of a MOSFET during various stages of fabrication are also shown.

To illustrate the gate oxide fabrication and integration aspects, fig.8 shows the evolution of the gate dielectric from the first demonstrators to the ones we currently have. As can be noted, the first samples were showing increased gate leakage current values and were failing before reaching the nominal gate voltage of VGS=15V. Through improved processing, the last gate dielectric demonstrators show very low leakage current levels and are able to support VGS=15V. This is an important steppingstone towards the fabrication of reliable high power SiC MOSFETs.

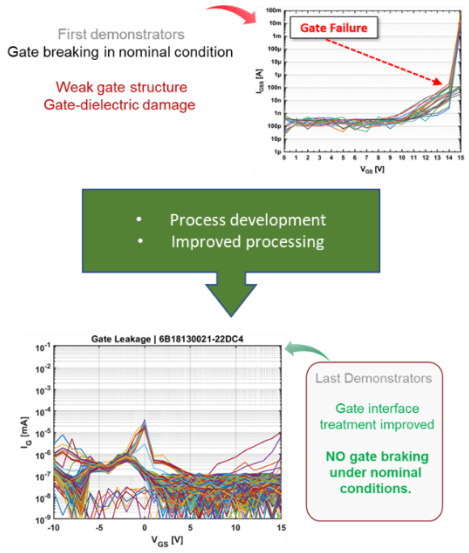
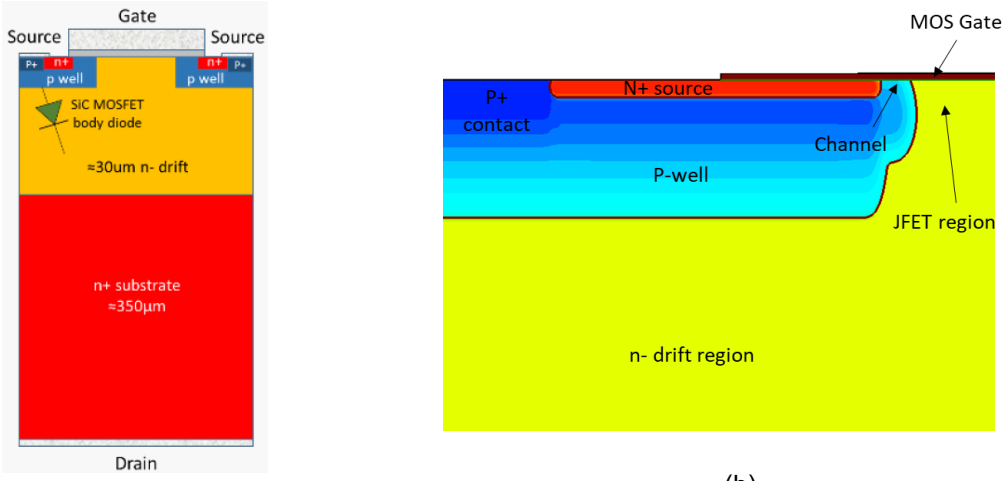



Fig. 8 Evolution of the gate dielectric performance - from the first to the current demonstrators.

### Design of the 3.3kV MOSFET

The schematic cross-section of 3.3kV MOSFET active cell is shown in fig. 9 (a). The 350um of substrate have been modelled by using a resistance (lumped and function of the temperature), which has been added at the drain contact.




(a) (b)

Fig. 9 Schematic cross-section of a 3.3kV MOSFET (a) and TCAD cross-section of the simulated 3.3kV MOSFET active cell (b).

To confirm the choice of the epitaxial layer specifications, Ron vs VBR simulations have been run (fig. 10). This is an important step towards the final MOSFET design as it dictates the performance vs. cost trade-off. Based on these results, the epitaxial layer thickness has been confirmed at 30um.

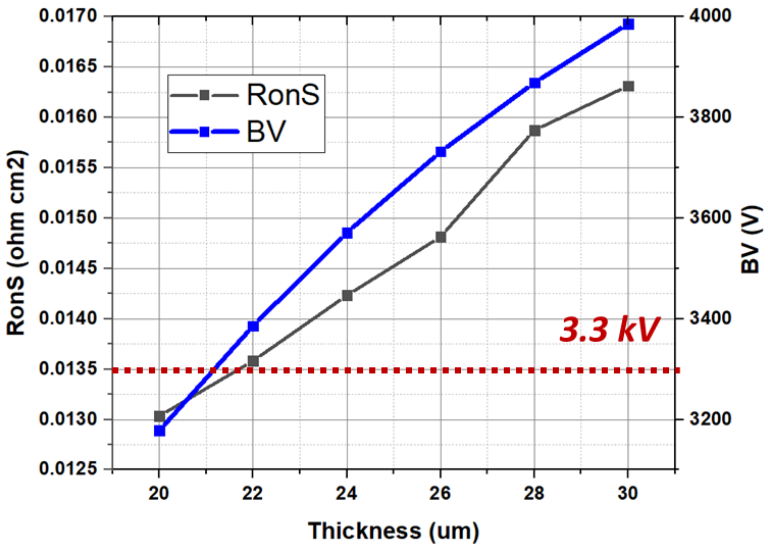
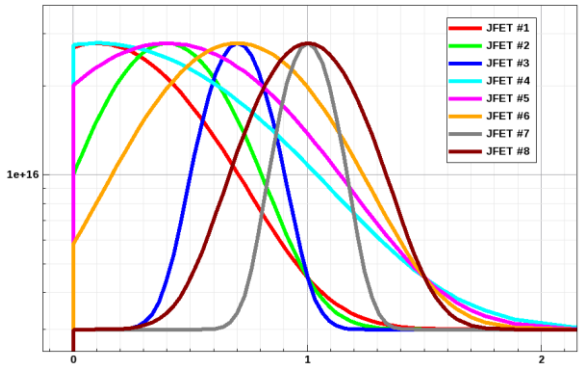


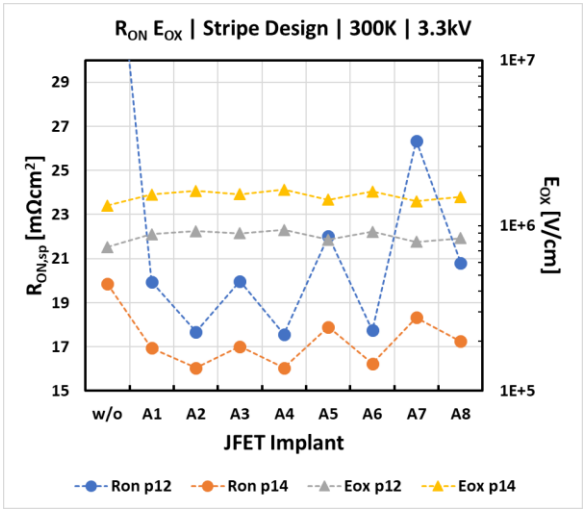

Fig. 10 Ron and VBR dependence on epitaxial layer thickness for a 3.3kV-rated MOSFET.

To analyze the influence of the JFET region on the MOSFET performance (Ron vs long term reliability), several JFET profiles have been investigated through extensive TCAD simulations. For the JFET profile,

a Gaussian doping distribution has been used (as shown in fig. 11). For this investigation, a stripe cell design has been considered. The variation of Ron and field oxide (Eox) for cell pitches of 12 and 14um, respectively, is shown in fig. 11b. As can be seen, there is clear trade-off between Ron and Eox. This means that the cell pitch dimensions have to be carefully chosen towards an optimum on-state/reliability trade-off.




(a)

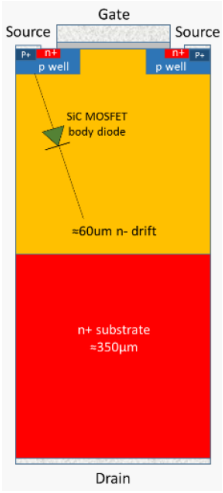



(b)

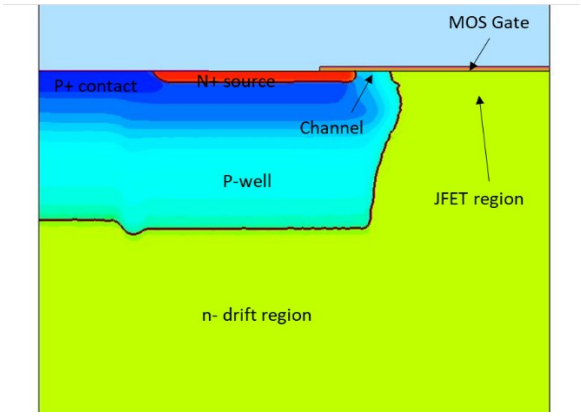
Fig. 11 JFET region profiles investigated (a) and variation if Ron and Eox with JFET region profile, for 12and 14um cell pitches (b).

**Design of the 6.5kV MOSFET**

The schematic cross-section of 6.5kV MOSFET active cell is shown in fig. 12 (a). Similar to the 3.3kV MOSFET case, the SiC substrate has been modelled using a lumped resistance added at the drain contact.



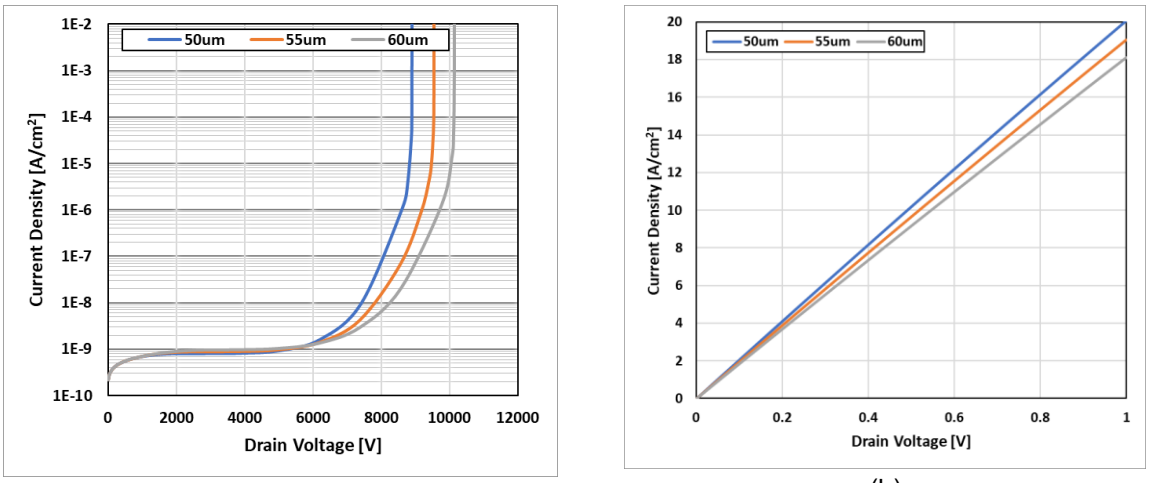

(a)




(b)

Fig, 12 Schematic cross-section of a 6.5kV MOSFET (a) and TCAD cross-section of the simulated 3.3kV MOSFET active cell (b).

The variation of VBR and Ron values with the thickness of the epitaxial layer is shown in fig. 13. Based on the simulations results, an epitaxial layer thickness of 55um has been selected.




(a) (b)

Fig. 13 VBR and Ron dependence on the thickness of the epitaxial layer for a 6.5kV-rated MOSFET.

Starting from the work done and results obtained in the framework of the AMPERE project, we have simulated a JTE-based edge termination for 6.5kV SiC MOSFET. The voltage blocking curves for three different JTE charge doses are plotted in fig. 14. All three JTE doses give blocking voltages in excess of 8kV, which demonstrates more than 90% edge termination efficiency.

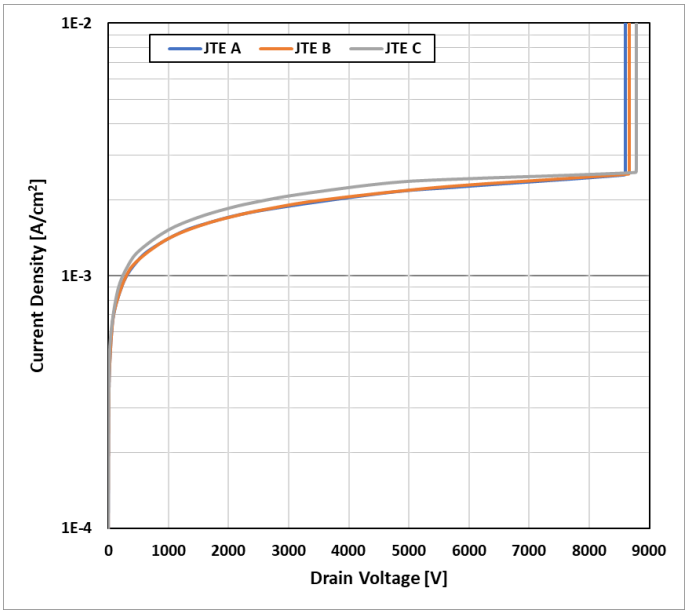



Fig. 14 Blocking curves for a 6.5kV-rated JTE-based edge termination; three different doses have been simulated.

**Electro-magnetic design of the SiC LinPak**

In the scope of this project, a High Voltage (HV) Silicon Carbide (SiC) LinPak module was developed. Due to strategic reasons, the housing block for this new module is chosen to be the same as the HV Si LinPak module under development. This fact is defining critical things such as terminal position and size for main and auxiliary potentials. As a result, the design optimization phase was limited to substrate design, including chip and wire bond layout optimization.

One of the critical aspects of a power semiconductor module is the electromagnetic (EM) behavior. A good EM behavior will help towards current balance, resulting in lower thermal losses and improved reliability. Along the design optimization phase, each proposed iteration was verified electromagnetically by the means of EM simulations using ANSYS Q3D package. Figure 15 shows the coupling inductance ranges for both High Side (HS), in blue and Low Side (LS), in green, switches. The red rhomb represents the average value. The optimization goal is to obtain a design which provides a small range, similar average values for HS and LS, and slightly negative (between -0.2 and -1 nH).

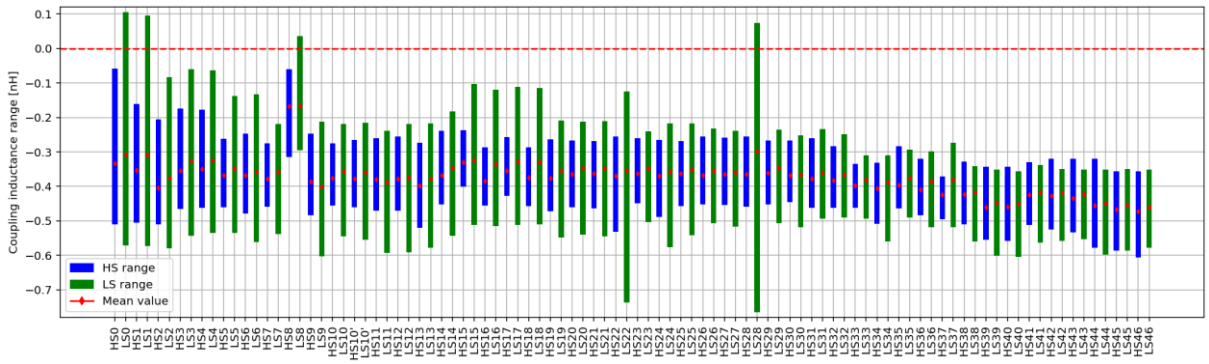



Fig. 15: Coupling inductance ranges of different design iterations for HV SiC LinPak module.

All design iterations were built on *fully populated substrates*, i.e. 20 SiC devices per substrate. It was observed that *half populated substrates*, i.e. 10 SiC devices per substrate, presented similar EM behavior.

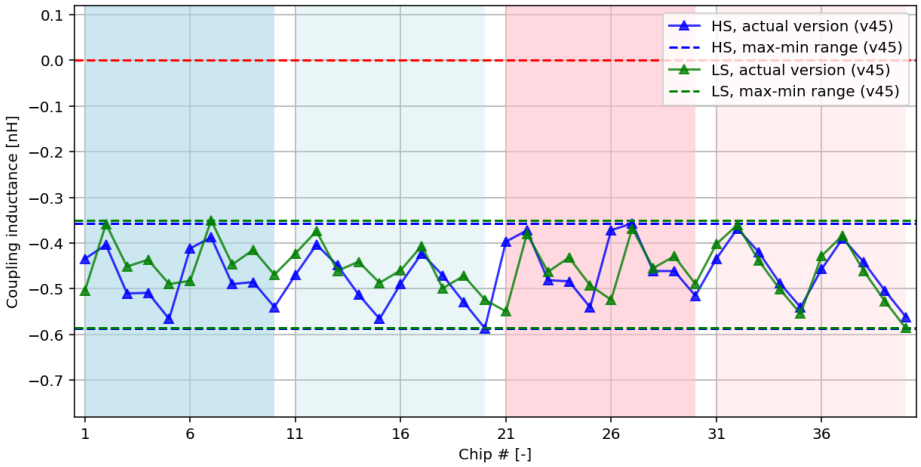



Fig. 16: Coupling inductance values of v45, for HS (blue) and LS (green) switches, per chip.

The best compromise between thermal and EM results was achieved in v45. The resulting EM behavior can be observed in fig 16. Note that the x axis represents the chip number, per switch (i.e. two fully

populated substrates correspond to a total of 40 chips per switch) Additionally, the simulated stray inductance was 29.7 nH, meeting the target specification of <30 nH.

These EM results compare well from coupling inductance range to other LinPak modules in the product portfolio, as shown in the figures below.

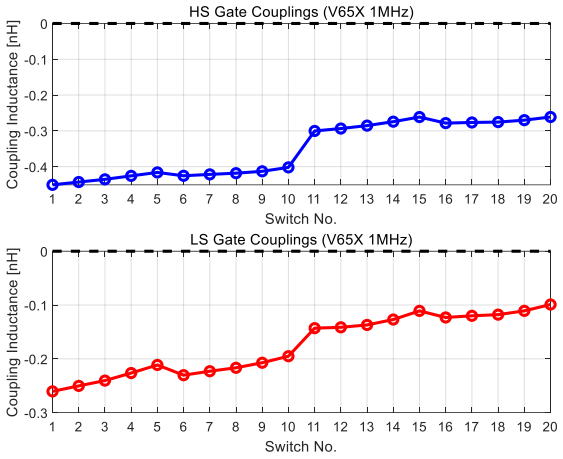



Fig. 17 Coupling inductance values for LV SiC LinPak for 20 chips per side configuration.

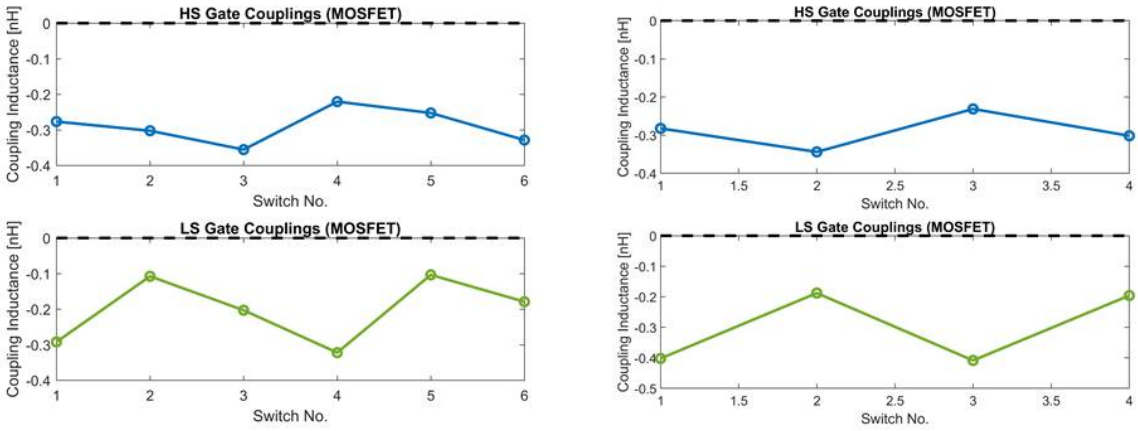



Fig 18 Coupling inductance values for HV Si LinPak, for 3 IGBT+ 2 diode configuration (left) and 2 IGBT + 2 diode configuration (right).

## 3.2 Half-Bridge converter, 3.3 and 6.5kV

Due to the increasing efficiency of power electronic systems, the exact determination of power losses becomes more and more important. Whereas the characterization of the SiC modules provides the basic information necessary for the design of power converters such as static and switching losses as well as SOA, reliability and ruggedness, it does not assess its behavior in real applications. In order to address those features, we will test the technology demonstrators into 3.3 and 6.5 kV half-bridge single-phase converters, which is the basic building block for most of converter topologies (DC-to-AC converters, most AC/AC converters, the DC-to-DC push–pull converter, isolated DC-to-DC converter), and thus a very flexible and robust platform to evaluate power semiconductor modules in applications. Further, we will build similar Si IGBT H-bridge converters in order to assess performance improvement of the SiC counterpart. The SiC and Si LinPak modules will be provided by Hitachi Energy in order to achieve a fair comparison. Based on the literature in SiC converters, we target the converter demonstrator efficiency between 96-98% for the Si IGBT converter and >99% for the SiC MOSFET converter.

The final power specification of the 3.3 and 6.5 kV H-bridge converters is dependent on the SiC module current rate, but we estimate it to be about 225 kW and 275 kW average single-phase AC power, respectively.

The converter mechanical arrangement and topology of the Si IGBT will be the same as that of the SiC MOSFETs, but in the late case, it will be optimized for low stray inductance. The main difference will be related to the gate drives. Because of the challenge to supply very high current, we will use a power electronics topology that recycle the half-bridge converter current, thereby overcoming power limitations. One traditional technique to characterize high-power inverters losses is based on the opposition method. This technique consists of connecting two identical systems in a back-to-back connection, allowing to circulate high power between the systems with a low-power electrical source and without the use of dissipative loads. The physical principle is demonstrated in Figure 19, where the power source provides only the power losses ($P_{losses1}$ + $P_{losses2}$). At the same time, a high-power (P1) circulates between the systems. This is possible because there is no dissipative load consuming active power. Consequently, the power supplied by the source is low when the system operates at nominal conditions, presenting a significant reduction of the facility requirements.

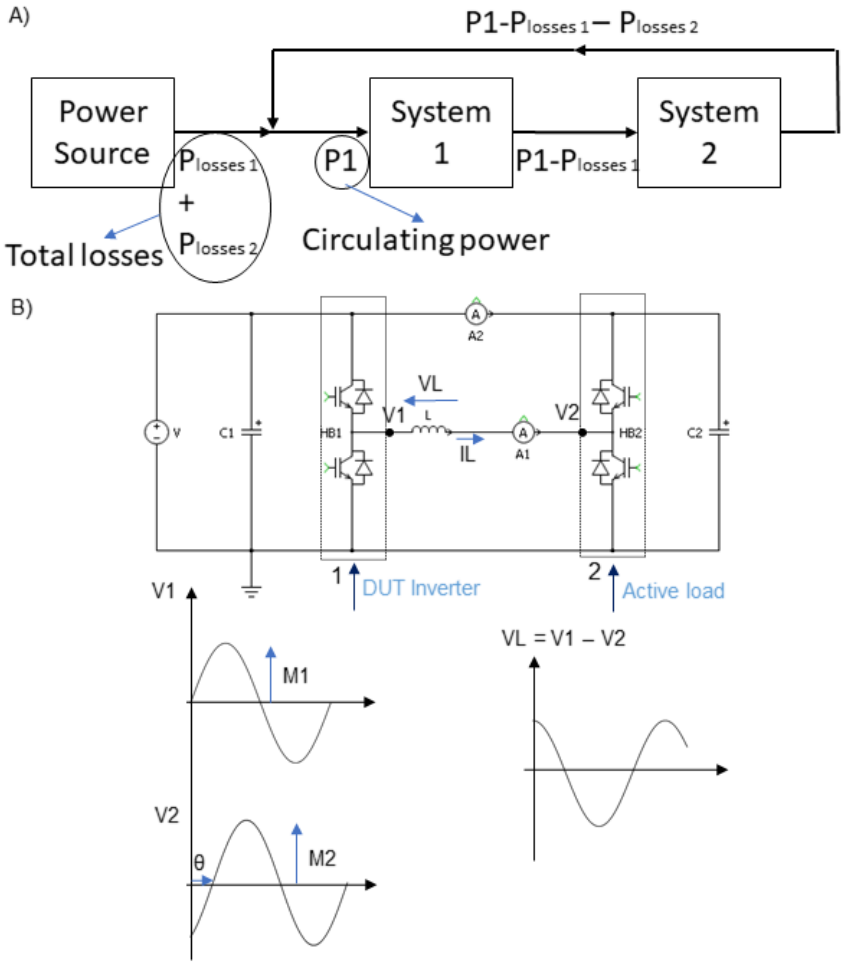



Fig. 19 Single line diagram of Half-bridge converter characterization tester.

Here, the system is composed of two half-bridge legs, identical to a traditional H-bridge inverter. The first leg is the device under test (DUT), and the second one acts as an active load, modulating the AC voltage at 50Hz. An inductor is connected to limit the current due to the differential voltage between the h-bridge legs. By using a sinusoidal pulse-width-modulation (SPWM) control is possible to adjust the fundamental voltage vectors (V1, V2) of the two legs in order to control the magnitude and phase angle of the voltage across the inductor L (VL = V1-V2). Such control is performed by changing the modulation factors (M1, M2) that are responsible for the amplitude voltage control from each leg and the phase shift (θ) between V1 and V2 (Figure 19B). In order to characterize the inverter losses under a specified operating condition, the inductor voltage (VL) is selected to achieve the desired inductor current (IL = VL/XL). For an inverter designed with the 3.3 kV/450A or 6.5 kV/300A Linpak module from Hitachi Energy, the nominal power of about 200-250 kVA can be easily achieved with the opposition method. Furthermore, the switching frequency can be changed to investigate the losses under a range of operational frequencies. Since the MV Si IGBT modules typically do not operate at frequencies higher than 2kHz because of excessive power losses, and thus heating, we will compare the different semiconductor technologies at frequencies starting at 450 Hz till 2000 Hz. At higher frequencies, the module requires down rating the current in order to compensate the switching losses for the conduction losses. Further, at higher frequencies reliability of the motor and bear rings becomes a major issue.

The converter is targeted to operate at 1.8kV for the 3.3kV rated modules, and at 3.6kV for the 6.5kV. In order to allow fair comparison between the Si IGBT and SiC MOSFET modules in the converter application, we will build similar heatsinks and electromagnetic components for both semiconductors.

## 3.3 3.3 kV Converter design

The topology presented in Figure 19 is implemented for the 3.3 kV Si IGBTs Linpack modules from Hitachi Energy. Each part of the system design is detailed in the following topics.

**Capacitor selection**

The capacitors provide high current to the power modules during converter operation and keep a stable DC voltage, limiting the voltage ripple. Figure 20 shows system simulations and analytical modelling results of the voltage ripple for different capacitance values.

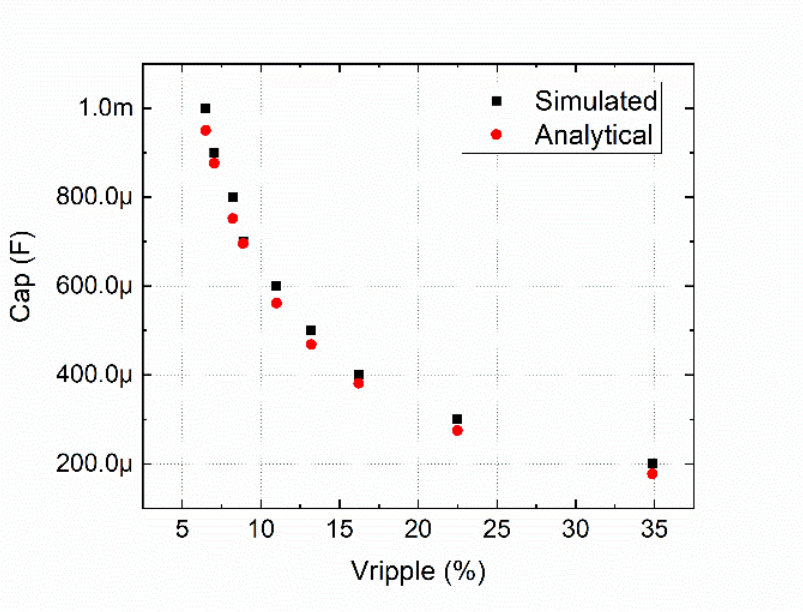



Fig. 20 Capacitance value versus voltage ripple at full load conditions (IL: 300 A, V: 1.8 kV).

The selected capacitor model is the B25645A2677K003 from EPCOS-TDK Electronics, which presents a capacitance of 670 µF, Vmax of 2.3 kV and stray inductance of 14 nH. Performing a series-parallel association of 6 capacitors, we could achieve an equivalent capacitance of 1 mF that corresponds to a ripple of ~ 7% at full load and an equivalent stray inductance of ~ 10 nH. Such low stray inductance is essential to avoid overvoltage during the semiconductor switching.

**Busbar design**

A two-layer laminated copper busbar has been designed to optimize the system's stray inductance. Again, thin Kapton layer has been used for electrical isolation (> 30 kV) between the copper layers and to achieve a low stray inductance busbar (estimated ~ 10 nH).

**Cooling design**

For an efficient heat transfer between the power modules and the active cooling, a cold plate from ATS (model ATS-CP-1000-DIY) has been selected. This cold plate can provide a low thermal resistance of 6 mK/W and is mechanically compatible with the Linpack module dimensions. A Dow Corning 340 thermal paste is used as an interface material between the module case and cold plate to improve heat transfer by reducing the thermal contact resistance.

## 3.4 3.3 kV Si IGBT Gate driver design

The gate driver is a power amplifier circuit responsible for switching on and off the semiconductor. Such circuit receives the low power signals from the controller and produces a high current drive input to the semiconductor gate terminal. Furthermore, the gate driver also provides system protection under short-circuit events and must be well-designed to provide clean switching waveforms and low switching losses. Linpak modules do not present compatible gate drivers available in the market. A homemade gate driver has been designed with desaturation short circuit protection, optical fiber signal connections to improve noisy immunity, voltage isolation and creepage distance respecting medium voltage standards for a safe operation. The gate driver specifications, and the final assembled gate driver photo are shown in Figure 21.

| | **3.3kV/450A Si** |
|---|---|
| **Gate Voltage**[1] | -10 / +15 V |
| **Immunity** | ~25 V/ns |
| **Gate resistor**[2] | 1.5 Ω(on and off) |
| **Max Gate current**[3] | 35 A |
| **Max frequency**[4] | 10 kHz |
| **Operating voltage** | 1.8 kV |
| **Power gate**[5] | 3 W |

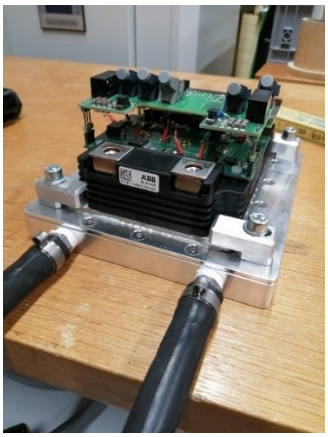


Fig. 21 (Left) Gate driver specifications. (Right) Gatedriver on top of a 3.3 kV Si IGBT Linpack power module with optical connections. The power module is fixed on a cold plate.

### Load Inductor

The inductance value has been selected through extensive system simulations to allow a characterization range from sub-load (~30 A) up to full load conditions (~300 A) with a current THD smaller than 12%. The chosen inductance value is 2.5 mH. A customized inductor has been ordered with the specifications shown in Table 1 and the inductor photo is shown in Figure 22.

Table 1: Inductor parameters

| Parameters | Comments |
|---|---|
| Maximum operating current (continuous)<br>I rms = 300 A | Sinusoidal current at 50 Hz with maximum THD of 12%. |
| L = 2.5 mH | Very stable inductance value in the whole range of current operation (0 up to 300 Arms) |
| Saturation current = 500 A | Large saturation current to guarantee safe operation with transient currents and a stable inductance value in the operating range (0 up to 300 A rms) |
| Operating voltage: Max 4 kV | PWM chopped voltage from inverter output |
| Insulation voltage: 10 kV | |

Fig. 22 Monophase load inductor. The inductor weighs 260 kg with dimensions of 485 x 385 x 730 mm.

### Controller design

A TMS320F28379D microcontroller from Texas Instruments performs the angle control and PWM generation. A dedicated PCB, shown in Figure 23, has been designed to integrate the microcontroller board, optical fiber connections and current sensor. Two different control strategies have been performed: one operating at open feedback loop and a second one at a closed feedback loop. In the closed feedback loop option, the load current is measured by a current sensor, and the controller automatically sets the phase shift. For the open loop control method, the user sets the phase shift according to a look-up table, and no current sensor is required.

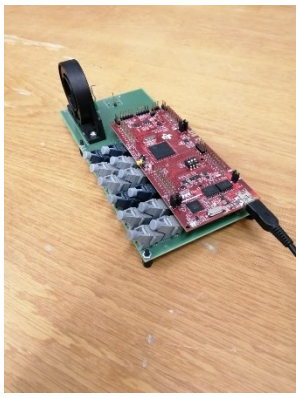


Fig. 23 Microcontroller board with integrated optical connectors and current sensor.

System assembly

The final assembled of the 3.3 kV Si IGBT converter is shown in Figure 24. The system is built on a grounded aluminium plate, and acrylic protection is added for additional safety.

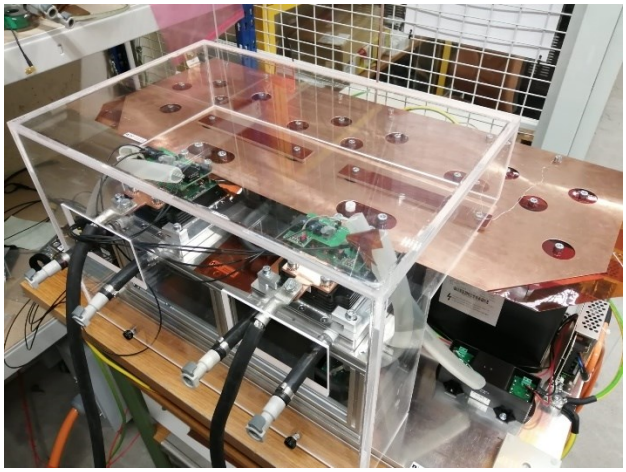


Fig. 24 3.3kV Si IGBT back-to-back monophase converter.

## 3.5 6.5 kV Si IGBT Converter design

The topology presented at Figure 19 is implemented for the 6.5 kV Si IGBTs Linpack modules from Hitachi Energy. Each part of the system design is detailed in the following topics.

**Capacitor selection**

The same capacitor model from the 3.3 kV converter has been selected. A series-parallel association of 4 capacitors was used to achieve an equivalent capacitance of 670 µF and equivalent stray inductance of ~ 10 nH. Such capacitance value guarantees a voltage ripple smaller than 10% at full load conditions.

### Busbar design

For the 6.5kV Si IGBT Linpaks, a new two-layer laminated copper busbar has been designed to optimize the system's stray inductance. Again, a thin Kapton layer has been used for electrical isolation ( > 30 kV) between the copper layers and to achieve a low stray inductance busbar (estimated ~ 10 nH).

### Cooling design

The same cold plate used for the 3.3 kV Linpak modules was used for the 6.5 kV Linpak modules.

## 3.6 6.5kV Si IGBT Gate driver design

A different design from the 3.3 kV Linpak modules has been used since the 6.5kV Si IGBT Linpak power module presents a distinct footprint and requires higher creepage distances. A homemade gate driver has been designed with desaturation short circuit protection, optical fiber signal connections to improve noisy immunity, and Creepage distance respecting medium voltage standards for a safe operation. The gate driver photo and parameters are shown in Figure 25.

| | 6.5kV/300A Si |
|---|---|
| Gate Voltage[1] | -10 / +15 V |
| Immunity | ~25 V/ns |
| Gate resistor[2] | Variable |
| Max Gate current[3] | 35 A |
| Max frequency[4] | 10 kHz |
| Operating voltage | 3.6 kV |
| Power gate[5] | 3 W |

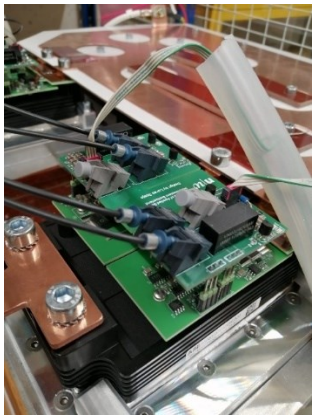


Fig. 25 (Left) Gate driver specifications. Right) Gatedriver on top of a 6.5 kV Si IGBT Linpack power module with optical connections. The power module is fixed on a cold plate.

### Load Inductor

The same inductor load from section 2.1.5 was used for this converter. The inductor has been designed to be used as a load for both converters.

### Controller design

The same control strategy presented in section 2.1.6 has been used for the 6.5 kV converter. Some changes were performed in the controller tuning parameters and look-up tables.

### System assembly

The final assembled system is shown in Figure 26.

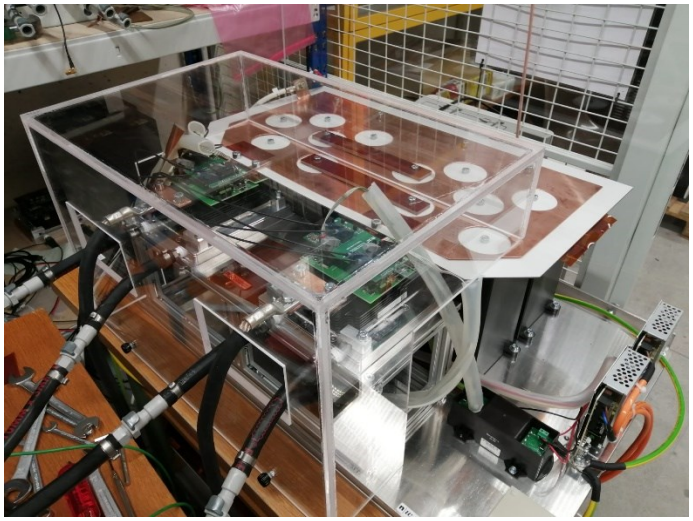


Fig. 26 6.5kV Si IGBT back-to-back monophase converter.

### 3.5. Thermal system and characterization protocol

In this section, we initially describe the power converter cooling system and sensors used in the temperature and flow measurements to characterize the converter losses during steady-state operation. We later discuss the power loss characterization protocol based on this initial description.

The cooling system comprises one cold plate for each Linpak module (2 modules in total) responsible for the convection heat transfer between the power module and the water flow. Rubber pipes connect the cold plates to an air-colled 6.5kW chiller unit responsible for removing the heat to the environment. A Coriolis flow meter is then used to accurately measure the water flow with an accuracy of 0.1%. Four thermocouples (K type – 1 mm thick) were placed in the inlet and outlet of each cold plate to measure the fluid temperatures. The thermocouples have been calibrated in oil bath to achieve an accuracy of ± 0.1 $^{o}$K. Figure 27 shows the chiller unit, the thermocouples placed in the pipes to measure the inlet and outlet temperatures and the power converter integrated with the cooling system.

Fig. 27 (Top-left) Chiller unit. (Top-right) Thermocouples placed in the inlet and outlet of each coldplate. (Bottom) Power converter with cooling system.

Our main goal is to determine the power module's individual losses and converter efficiency. Two methods will be used to characterize the H-bridge converter losses. All measurements will be performed once the converters are ready for safe operation and after 30 min of continuous operation to avoid any transient behavior. Systematic uncertainties will be determined for each measurement technique individually.

1) The first characterization is based on the water flow exchanger method [2]. Here, the semiconductor power losses can be directly obtained using a water-cooled system for the power modules. The principle is based on the heat exchange between the coolant and the semiconductors. Therefore, the coolant flow rate and the inlet and outlet differential temperature must be properly measured (see Figure 28). Equation (1) shows the relation between semiconductor power losses, the input and output differential temperature and the coolant flow rate.

$$P_{loss} = \Delta T * c * \rho * Q \qquad (1)$$

where $P_{loss}$ is the semiconductor losses (W), ΔT is the inlet and outlet water differential temperature (K), c is the water-specific heat capacity (J/kg.K), ρ is the water mass density (kg/m$^3$), and Q is the water volume flow rate (m$^3$/s).
An estimative of the expected measurement error is shown below, considering typical parameter values.

$$Flow = 8.33 * 10^{-5} \pm 0.09 * 10^{-5}\ m^3/s$$
$$density = 1028 \pm 2\frac{kg}{m^3}$$
$$Spec.heat = 3800\ J/kgK$$
$$\Delta T = Tin - Tout$$
$$\delta Ploss \sim Ploss * \frac{\delta \Delta T}{\Delta T}$$

0.2K → ~3.3%

6K @Full load

This method consists of a simplified version of the calorimetric method. It presents relative errors of around 3 % at full load with a decrease in accuracy for low power losses due to the smaller differential temperature (reaching up to around 10% at sub load conditions). A possible solution for this problem is reducing the coolant flow rate to increase the differential temperature [2].

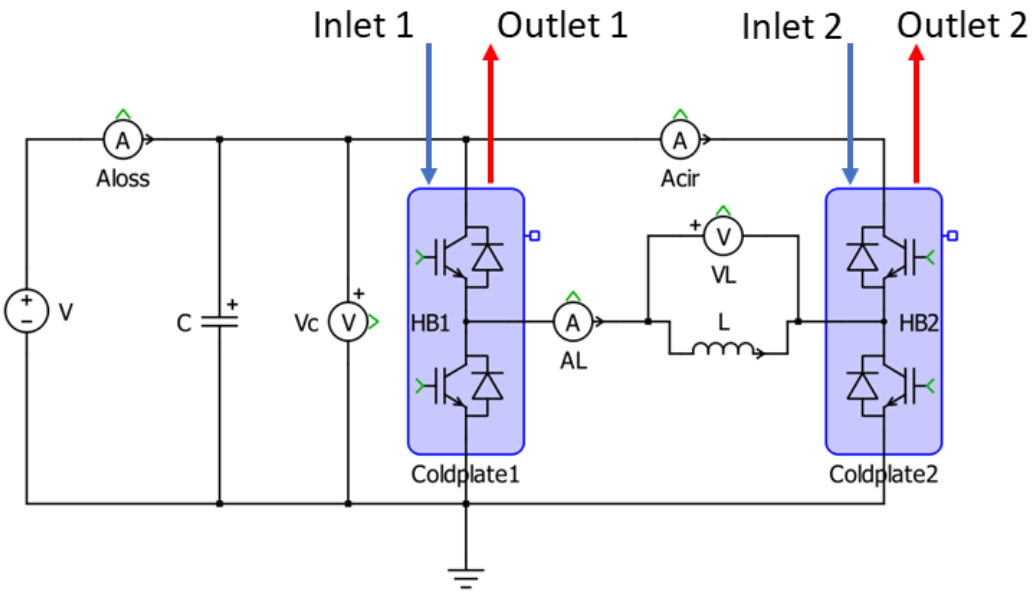



Fig. 28 Back-to-back monophase converter with thermal system inlet-outlet indications for each coldplate and electrical measurement points.

2) The second characterization is based on the opposition method [2]. Here, we electrically measure the voltage and currents using a power analyzer (Model: Hioki PW8001). The overall losses are measured directly from the power supply. In order to obtain the semiconductor power losses, the inductor losses must be estimated. Therefore, we aim to measure the inductor losses (PL = VL * AL), total power losses (Ploss = Vc * Aloss) and circulated power (Pcir = Vc * Acir). The measuring points are indicated in Figure 28.
The converter efficiency can be obtained from Eq. (2) for the back-to-back converter [3]:

$$\eta = 1 - \frac{Ploss}{Pcir+Ploss} \quad (2)$$

An error propagation method will be applied to each voltage and current harmonics to estimate the measurement accuracy.
Both methods constitute state-of-the-art power losses and efficiency measurements in medium voltage power converters. Their results will be compared to provide a consistent and reliable analysis.

For further investigation of the thermal characteristics of the modules, one essential parameter is the semiconductor junction temperature ($T_j$). Such parameter is directly related to the thermal stress the semiconductor is subjected to under an operation point and to the semiconductor/packaging operating limits. Here, we propose using micro thermocouples placed directly underneath the power semiconductor substrates, also known as the power module case, and the average temperature measured ($T_{case}$). By knowing the junction-to-case thermal resistance of the module ($R_{thjc}$) and the characterized power loss ($P_{loss}$), we can estimate the temperature of the chip (Tj) [3], as shown in Eq. (3).

$$Tj = T_{case} + R_{thjc} * P_{loss} \quad (3)$$

Where Tj is the junction temperature (K), $T_{case}$ is the case temperature (K), $R_{thjc}$ is the junction to case thermal resistance (K/W) and $P_{loss}$ is the semiconductor loss (W).
By measuring the junction temperature, we can investigate the operational limits of the power modules for each switching frequency and load current.

### 3.6. Chip and packaging characterization

The on-state performance from the first 3.3kV SiC MOSFETs lots are shown in fig. 29, for VGS=15V and T=25C. For comparison reasons, the IV curves for similarly-rated SiC MOSFETs using SiO2 as gate dielectric are also shown. As can be seen, the use SiO2/SiN stack leads to an improvement of ~14% in Ron values, for same pitch size and active area.

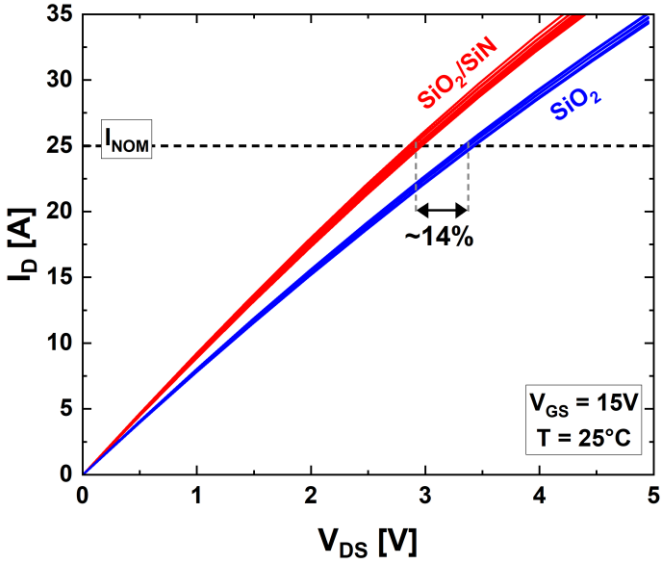



Figure 29: Forward IV of 3.3kV SiC MOSFET using a SiO2/SiN as gate dielectric; for reference, IV curves for similarly-rated SiC MOSFETs with SiO2 gate are also shown.

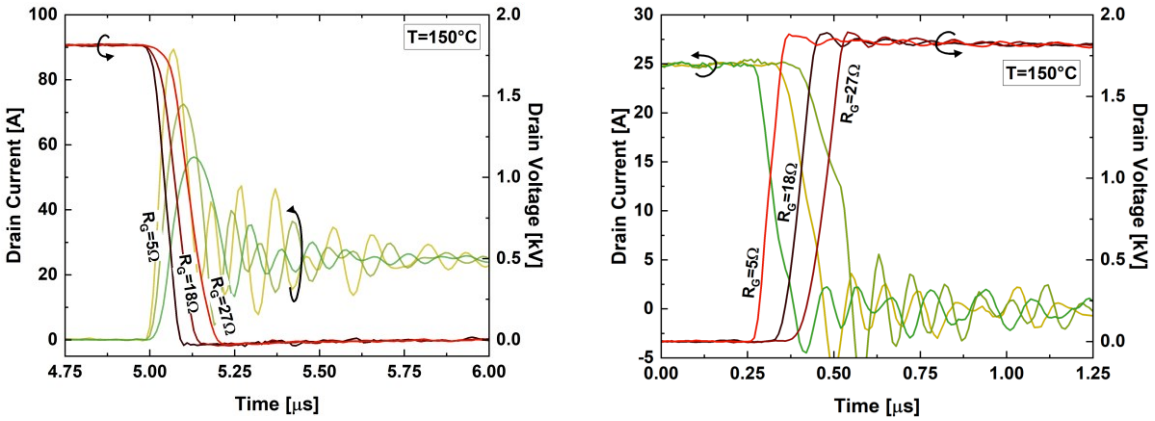
Once the wafer level static measurements mapping was finished, wafers have been diced, good chips have been picked-up and send for LinPak substrates assembly. Pictures of 1x MOSFET and 4x SiC MOSFETs bonded onto LinPak substrates are shown in fig. 30.

(a) (b)

Figure 30: (a) 1x MOSFET and (b) 4x SiC 3.3kV MOSFETs bonded onto LinPak substrates.

The substrates have been tested under nominal conditions, meaning $V_{Nominal}$=1.8kV and $I_{Nominal}$=25A/device. For all the tests the temperature has been set to T=150°C. The double–pulse tester had a fixed stray inductance of Lσ~90–100nH. For all the results reported here, a Si–like driving gate voltage of VGS=±15V was used.

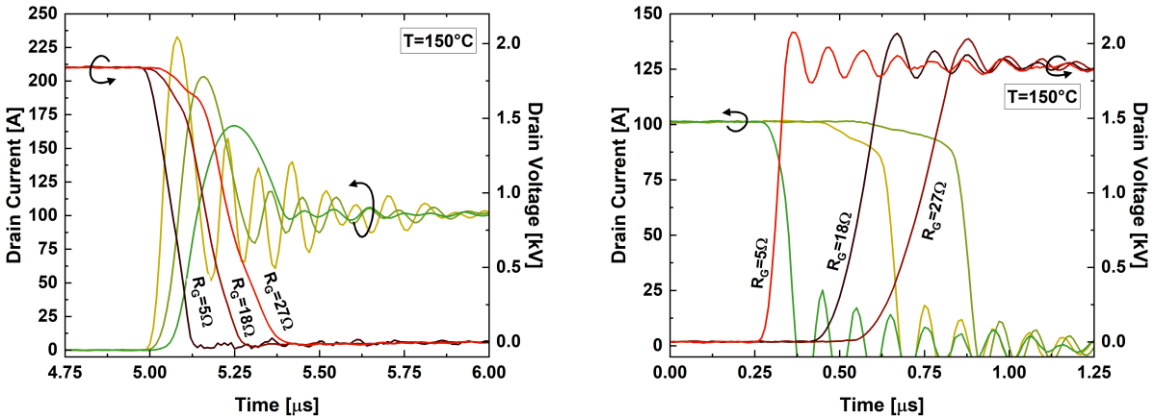
The turn-on and turn-off waveforms for 1x MOSFET substrate are shown in fig. 31. Three different external RG values have been used. The expected influence of the gate resistor on the switching speed dV⁄dt can be clearly observed, demonstrating good control of the dV/dt values. The more pronounced oscillations observed on the current waveforms are not chip–related, they are a result of the experimental setup itself.




(a) (b)

Fig. 31 Turn-on (a) and turn–off (b) waveforms for substrates with 1× devices, at different RG values ($V_{Nominal}$=1.8kV, $I_{Nominal}$=25A/die, $V_{GS}$=±15V, T=150°C)

The turn-on and turn-off waveforms for 4x MOSFETs substrate are shown in fig. 32, for 3 different external RG values. Here, the gate resistor and the stray inductance were not scaled for parallel devices, implying that the RG/chip and Lσ/chip are higher for the substrates with four MOSFETs. This is reflected in the larger overshoot for the drain voltage in Fig. 32(b) due to the higher parasitic inductance. Nevertheless, the substrates successfully passed the switching tests under nominal conditions.




(a) (b)

Fig. 32 Turn-on (a) and turn–off (b) waveforms for substrates with 4× devices, at different RG values ($V_{Nominal}$=1.8kV, $I_{Nominal}$=25A/die, $V_{GS}$=±15V, T=150°C)

The RBSOA capability of a 4x MOSFETs substrate is depicted in fig. 33. Here, the turn-off waveforms are shown for DC link voltage of 2.6kV. The load current has gradually increased from 100A (Inominal=25A/chip) to 200A, which corresponds to 2xInominal. It is worth mentioning that, despite the fact that both voltage and current are beyond nominal values, the substrates with 4x parallel chips still show rather clean waveforms and acceptable voltage oscillations. This proves a reasonably well-balanced current sharing between devices, thanks to a substrate design engineered towards the minimization of parasitic components.

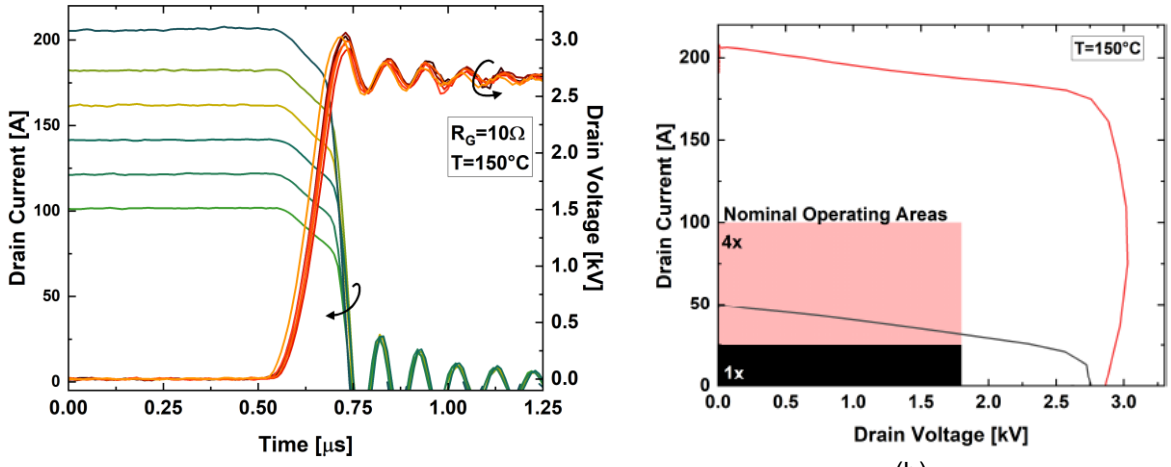



Fig. 33 Turn–off waveforms for substrates 4× devices (a), at different current values; RBSOA extracted from the switching I–V (b) ($V_{SOA}$=2.6kV, $I_{SOA}$=50A/die, $V_{GS}$=±15V, T=150°C)

For a more comprehensive investigation, the switching behaviour of MOSFETs with the proposed SiO2/SiN structure has been compared to devices with same design but fabricated with our standard SiO2 gate dielectric. In Fig. 34, the total switching energy $E_{ON}$ + E*OFF* per chip, calculated under nominal conditions ($V_{Nominal}$ = 1.8kV, $I_{Nominal}$ = 25A), is reported for different values of $R_G$. As could be expected, the SiO2/SiN–based devices exhibit marginally higher energy losses (this is due to the somewhat increased values of the input capacitance). Nevertheless, the increase in energy for the considered case is still moderately small (~12% max). If needed, as already demonstrated above, the energy losses could be adjusted using lower gate resistor values.

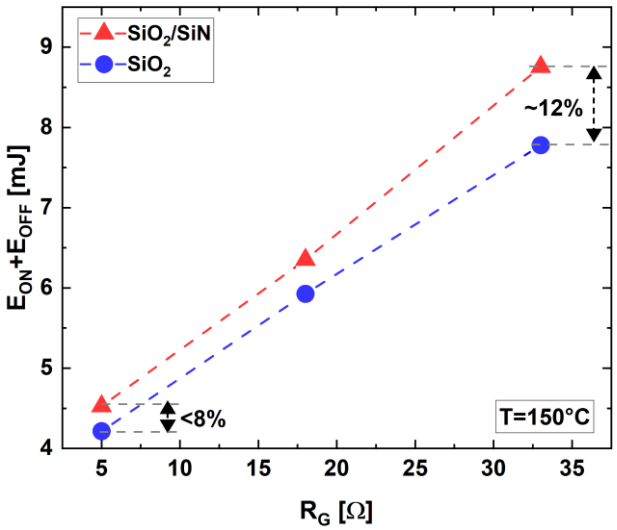



Fig. 34 Comparison of switching energy values for $SiO_2$ and $SiO_2$/SiN stack as gate dielectrics ($V_N$=1.8kV, $I_N$=25A, $V_{GS}$=±15V, T=150°C)

Working towards a fully operational SiC LinPak module (see fig. 35), 10x SiC MOSFETs substrates have been assembled and dynamically tested.

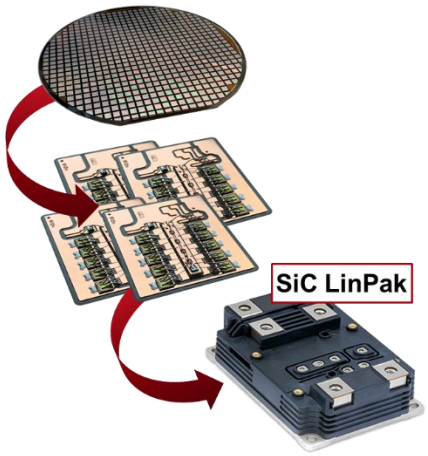
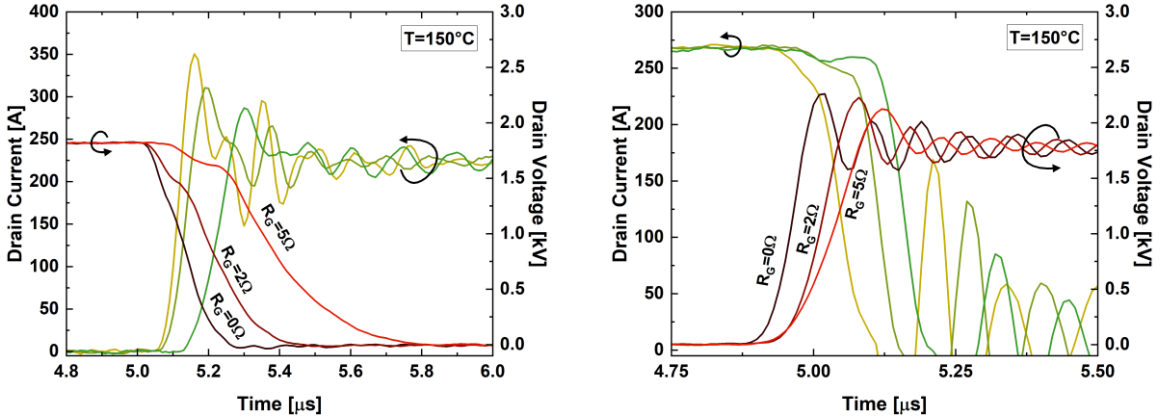



Fig. 35 SiC MOSFETs wafers towards LinPak substrates towards LinPak module chart.

Preliminary turn-on and turn-off waveforms, under nominal conditions, are shown in fig. 36. While some current (turn-on) and voltage (turn-off) overshoots and oscillations are observed, it is important to mention that all substrates under test passed nominal conditions testing without failure.




(a) (b)

Fig. 36 Turn-on (a) and turn–off (b) waveforms for substrates with 10× devices, for different RG values ($V_{Nominal}$=1.8kV, $I_{Nominal}$=250A, $V_{GS}$=±15V, T=150°C).

As mentioned in section 2.1, the module demonstrator is developed in the LinPak platform. The packaging technologies in the current project is shown in below (fig. 37). The chip top-side connection is established by heavy Aluminum wire-bonding. Silver sintering is selected for chip-substrate connection. The selected substrates are with high-performance aluminum nitride and with thick copper on both sides ensure electrical conduction and thermal radiation. For connection between substrate and baseplate, soldering is used. Ultrasonic welding is used for the terminal connection to the substrate. Gel is used as encapsulation.

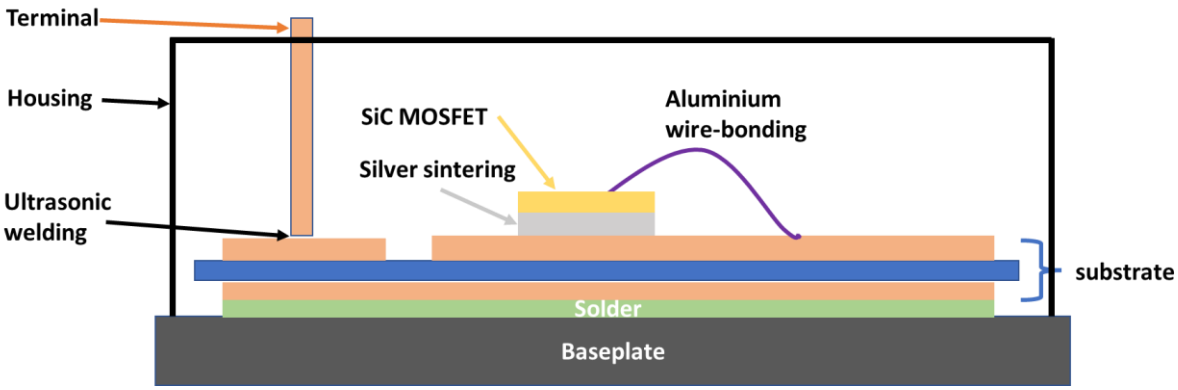


Figure 37: Schematic cross-section of the LinPak demonstrator. The dimensions are not to scale.

Most technologies take the synergy with on-development high-voltage Si-based LinPak product platform. Silver sintering as chip-substrate connection is newly introduced into the project considering the usage of SiC devices. Compared to Si devices, SiC-based devices have much smaller size while having the same power ratings, thus having much higher power density. Their intrinsic material advantages also bring the junction temperature much higher than that of Si devices.
Solders are not suitable for such high-temperature and high-power operations due to their relatively low melting points and low thermal conductivity. High-temperature solder material has melting points around 300 °C (573.15 K). The rating temperatures of many SiC MOSFETs have reached 175 °C (448.15 K), so solder's homologous temperature easily goes beyond 0.75. Such high homologous temperature brings material into exponentially higher creep deformation and therefore limited lifetime.
Silver sintering which produces porous silver joints, serves as one of most promising candidates for SiC-based chip attachment. Its melting point similar as pure silver (969 °C /1242.15 K) means 0.36 as homologous temperature at 175 °C operation, in such region the temperature-related creep is far less critical. Moreover, thanks to the silver material, the thermal conductivity of silver sintering is much better, ranging from 120 W/mK to 330W/mK, depending on the porosity and filler. Die-attach solder materials used in standard LinPak have thermal conductivity in the range of 60 W/mK. Here shows silver sintering joint established in Hitachi Energy Semiconductors (fig. 38).

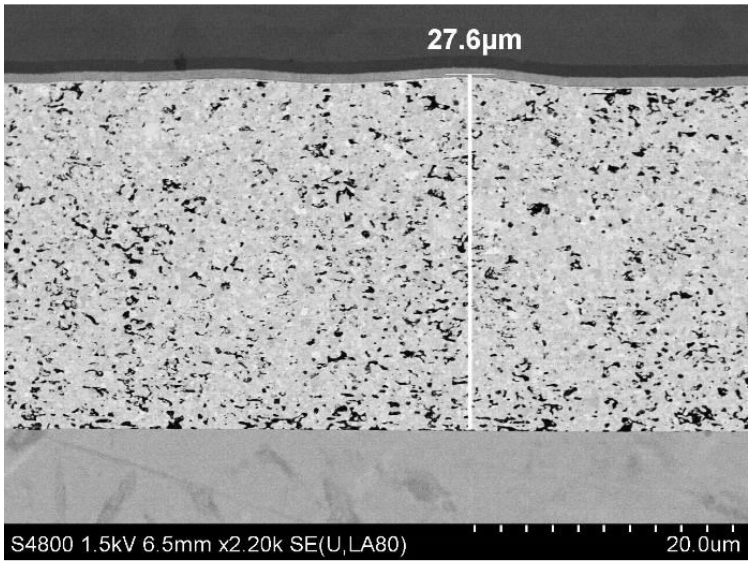
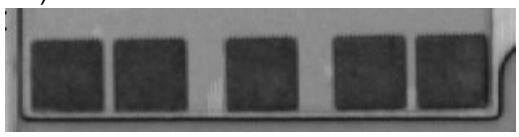
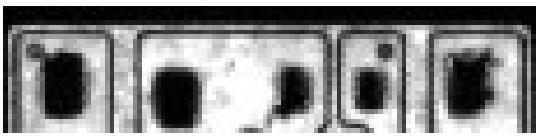


Figure 38. Silver sintering joint. From top to bottom: chip, silver sintering (27.6 µm), substrate.

Therefore, the silver sintering is selected for chip attachment technology for this project.
During the development, scanning acoustic microscope is used as the main method to characterize the interconnections. With the reflection mode, black contrast indicates good interconnections where the sound signal transmits fully without reflection. Light contrast means reflection of the sound signals, indicating voids or delamination. Here shows SAM images of the interconnection of the different layers (fig. 39):

(a)  (b) 

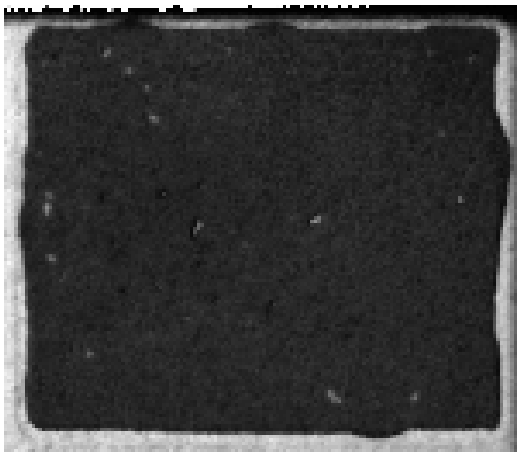
(c) 

Figure 39. SAM image of (a) sintered chip-substrate attachment, interconnections of 5 chips are shown; (b) ultrasonic welded terminal connection, interconnections of 5 terminal feet are shown; (c) soldered substrate-baseplate connection, 1 substrate is shown.

As shown in the SAM images, the established connections are with good quality which have good contact area and contrast. In the later stage of the development, the processes will be further investigated via fine characterization and possibly reliability tests. Based on the characterization results and reliability failure modes, process optimization and improvement can be done.
For Wire-bonding connections, the criteria are high mechanical strength however no damages especially on chips. Current prototype wire-bonding focuses on achieving low gate-source rate, therefore a relatively soft wire-bonding process is used. Future development on improving the mechanical strength can be done.
The other assembly technologies and processes used in this project are inherited from established LinPak with proven process stability. Therefore, no process optimization is planned unless needed.

### 3.7. Converter characterization

In order to validate the busbar and gate driver design, switching measurements have been performed. Any potential overvoltage caused by system stray inductance or switching noise caused by non-optimized gate driver designs could be accessed. The power modules have been switched at nominal voltages of 1.8 kV & 3.6 kV and currents of 400 A & 260 A for the 3.3 kV and 6.5 kV Si IGBT LinPak modules, respectively. The results are shown in Figures 40 and 41. The switching curves presented consistent gate stability and no overvoltage, both because to the optimized busbar design.

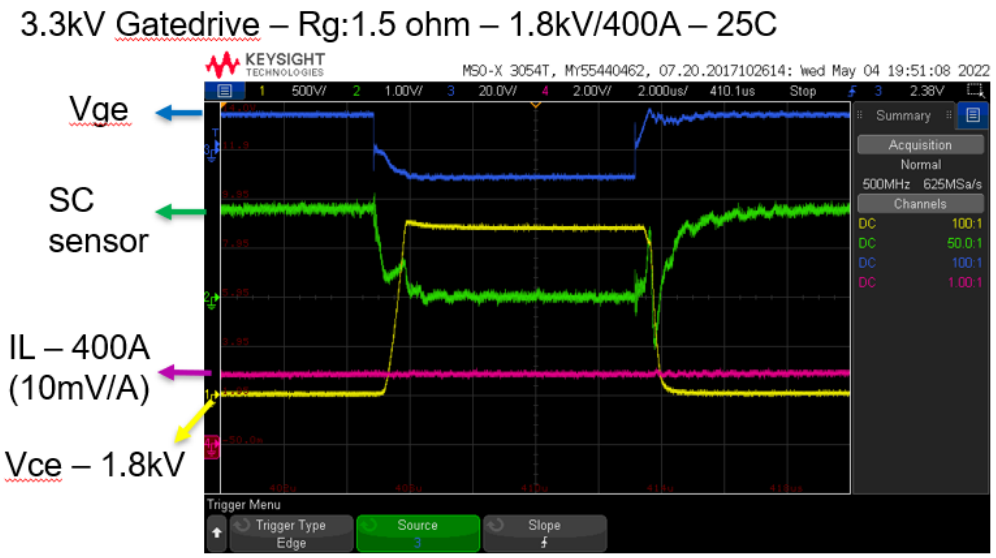



Fig. 40 3.3 kV Si IGBT LinPak switching curves at 1.8 kV/400 A – 25 °C. The gate curve is Vge, the switched current is represented by the inductor current IL, the collector-emitter voltage is represented by Vce. The SC sensor signal is the device current measured by a non-optimized home-made sensor with high-noise.

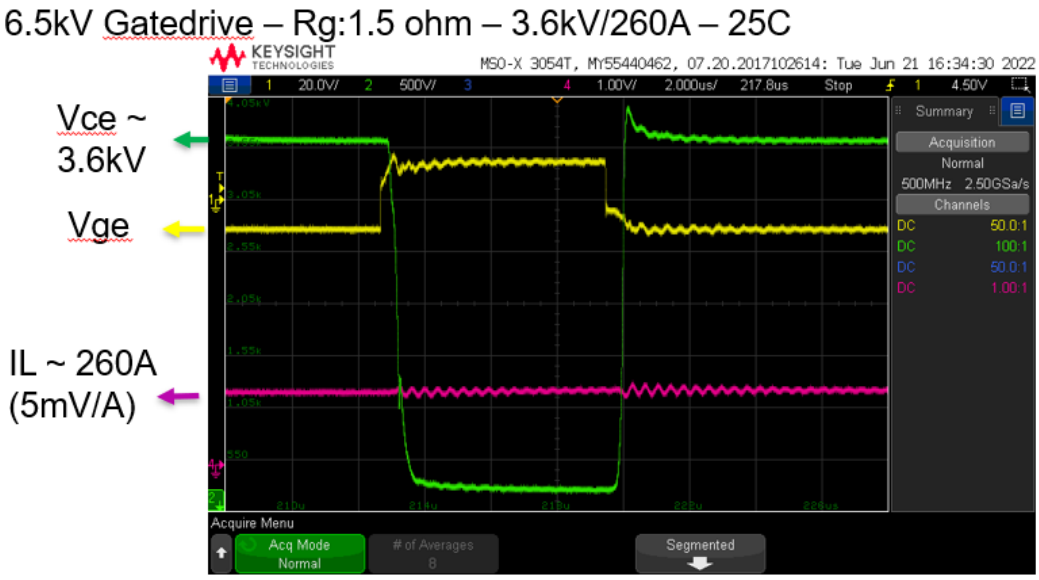



Fig. 41 6.5 kV Si IGBT LinPak switching curves at 3.6 kV/260 A – 25 °C. The gate curve is Vge, the switched current is represented by the inductor current IL, the collector-emitter voltage is represented by Vce.

In order to investigate converter operation, we performed initial tests to check the controller and system behavior under constant switching frequency. Figures 42 and 43 show the 3.3 kV LinPak converter operating with a current of 50 Arms and voltage of 300V.

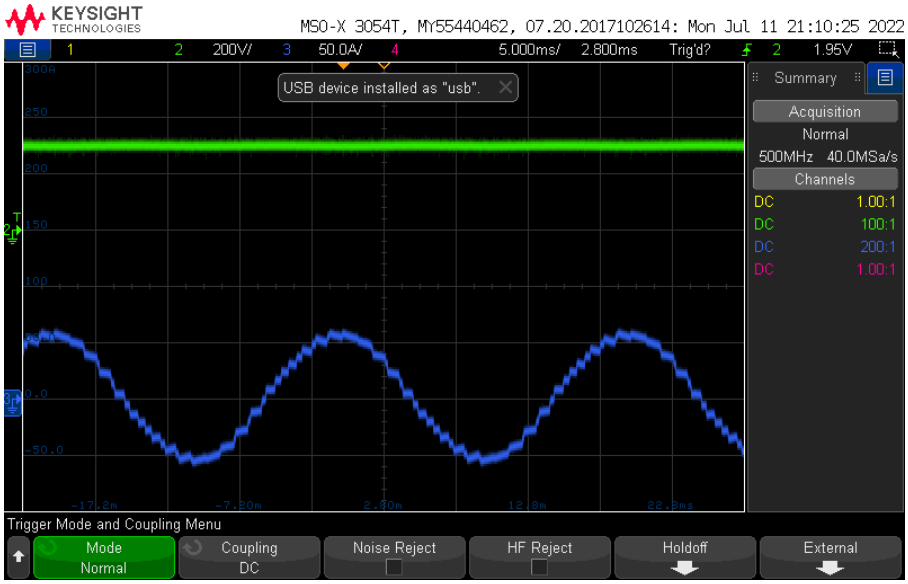



Fig. 42 Inductor load current (sine wave, 50 Hz) and DC link voltage (green - constant DC voltage). Switching frequency of 1 kHz.

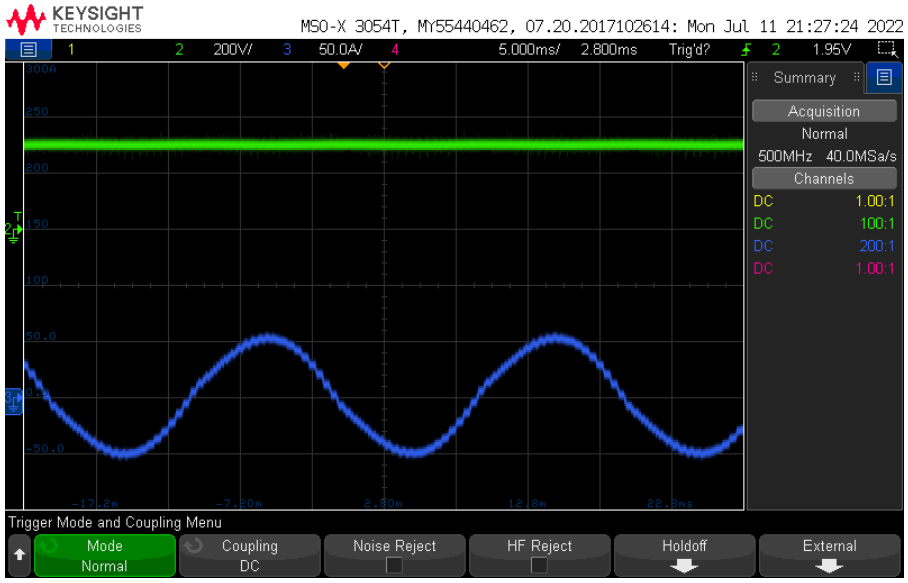



Fig. 43 Inductor load current (sine wave – 50 Hz) and DC link voltage (green – constant DC voltage). Switching frequency of 2 kHz.

In Figure 43 the switching frequency is increased from 1 kHz to 2kHz, with the sine wave improving its harmonics contents as expected. The converter presented stable operation during a 30 min test, validating the proposed controller.

With the support of the FHNW, we have purchased a high performance parameter analyzer that has been developed for fast measurement of WBG converters. We have received recently the equipment and will start performing first characterizations of the Si IGBT MV converter in November 2022.

# 4. Evaluation of results to date

The SiC-MILE project started on January 2022, with a 4-month delay in respect to the project plan, and as such, we have shifted the deliverables accordingly. The updated schedule plan is shown in the table below, where dark green indicate the tasks that have been completed. Besides the time shift, the production of the 6.5kV has delayed because of unexpected efforts on the delivering of the 3.3kV chips. This report has delivered the design, construction and experimental test of the 3.3 kV and 6.5 kV Si-based power converters test bench setups. Initial tests demonstrated that the system could provide clean switching waveforms, low stray inductance and flexibility to test the power modules under distinct operating conditions. The main challenges were to achieve an optimized low stray inductance design of power busbar and gate drives. Furthermore, the optimal components selection presented some challenges to offer a high degree of flexibility in the testing conditions. Some adjustments have been performed in the gate drive and busbar design through extensive testing to achieve an optimal design. The obtained results are on-time with the proposed deliverables in the project plan and enable a smooth project continuation focused on the characterization and SiC setup construction. In addition, the characterization setup with the measurement protocol has also been included. Such testers will be used for power losses and efficiency characterizations of the Si LinPak power modules from Hitachi Energy in distinct operation conditions (e.g distinct switching frequencies and sub-load to full load conditions).

| | | | 2022 | | | | 2023 | | | | 2024 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Q1 | Q2 | Q3 | Q4 | Q1 | Q2 | Q3 | Q4 | Q1 |
| Hitachi / ABB Power Grids | **WP1** | **Chip development** | | | | | | | | | |
| | HA01 | Definition of design | | | | | | | | | |
| | HA02 | Development of integration schemes | | | | | | | | | |
| | HA03 | Development of fab processes | | | | | | | | | |
| | HA04 | Lot 1 - 3.3 kV chips | | | | | | | | | |
| | HA05 | Lot 2 - 3.3 kV chips | | | | | | | | | |
| | HA06 | Lot 3 - 3.3 kV chips | | | | | | | | | |
| | HA07 | Lot 4 - 6.5 kV chips | | | | | | | | | |
| | HA08 | Lot 5 - 6.5 kV chips | | | | | | | | | |
| | HA09 | Lot 6 - 6.5 kV chips | | | | | | | | | |
| | HA10 | Static & dynamic characterization & lot evaluation | | | | | | | | | |
| | HA11 | Life cycle analysis | | | | | | | | | |
| | **WP2** | **Development of packaging demonstrator** | | | | | | | | | |
| | HA12 | Electro-magnetic (EM) Design of the SiC LinPak | | | | | | | | | |
| | HA13 | Selection of the joining technologies for the SiC devices in the module | | | | | | | | | |
| | HA14 | Developing of the packaging processes | | | | | | | | | |
| | HA15 | 3.3 and 6.5kV SiC MOSFET module qualification | | | | | | | | | |
| FHNW | **WP3** | **MV converter demonstrator** | | | | | | | | | |
| | FH01 | 3.3kV Half-Bridge design and construction (Si IGBT) | | | | | | | | | |
| | FH01 | 6.5kV Half-Bridge design and construction (Si IGBT) | | | | | | | | | |
| | FH01 | 3.3kV Half-Bridge design and construction (SiC MOSFETs) | | | | | | | | | |
| | FH01 | 6.5kV Half-Bridge design and construction (SiC MOSFETs) | | | | | | | | | |
| | FH02 | Test bench construction and 3.3 and 6.5kV converter characterization | | | | | | | | | |
| | FH03 | Evaluation of HV SiC in MV drive applications | | | | | | | | | |
| | FH04 | Dissemination | | | | | | | | | |

# 5. Life Cycle Analysis

The LCA Assessment focuses on understudying the energy use/requirements during the manufacturing processes of SiC semiconductors, as well as the resulting environmental impact. All steps in the life cycle of the semiconductor are analyzed from raw material extraction to application, and compared with that of Silicon.

This investigation is particularly relevant for silicon carbide (SiC) semiconductors, as there are some significant differences in the production processes compared to (conventional) silicon semiconductors.

Our approach is to gain a better understanding of the differences in energy demand along the whole life cycle for SiC and Si semiconductors. As such, the energy consumption over the following life cycle will be analyzed.

1. Define the life cycle stages for SiC and Si-based power semiconductors:
    a. Crystal Growth,
    b. Chip Manufacturing,
    c. Packaging,
    d. Application (Traction)
2. Calculate the energy consumption/requirements across the various stages.
3. Calculate the CO2 emission over the lifespan of the semiconductor.
4. Comparison between SiC vs Si with respect to their lifetime energy consumption

# 6. Next steps

This report has reported the Si IGBT-based converter and test setup. The following steps will focus on upgrading the testing workbench to characterize SiC power modules from Hitachi Energy. The main required changes are related to the gate drive design, such as distinct gate voltages and ultrafast short circuit detection. Then, the power loss characterization from Si and SiC technologies will be performed. Such characterization will require an intense R&D effort due to the inherent challenges in accurately characterizing ultra-fast switching devices. Finally, the SiC-based system's potential energy savings in traction applications will be evaluated through validated system simulations with the experimental data obtained.

Regarding the Life Cycle Analysis, initial work will be performed on collecting information about the life cycle stages of SiC power modules. Then, the energy consumption across each manufacturing stage and $CO_2$ emission over the lifespan of the semiconductor will be estimated. Finally, a benchmark comparison to Si technology with respect to their lifetime energy consumption will be analyzed.

# 7. National and international cooperation

This project is a collaboration executed between HITACHI ENERGY and the FHNW in Switzerland.

# 8. Communication

# 9. Publications

Publications will be released during the period of dissemination escribed in the project plan.

# 10. References

[1] N. Soltau et al, “Electric-Energy Saving using 3.3 kV Full-SiC Power-Modules in Traction Applications” in Proc. 2020 15th Int. Conf. on Ecological Vehicles and Renewables Energies (EVER).

[2] F. Forest et al, “Use of Opposition Method in the Test of High-Power Electronic Converters” IEEE Transactions on Power Electronics 53, 530 (2006).

[3] G. Ortiz et al, “Design and Experimental Testing of a Resonant DC-DC Converter for Solid State Transformers” IEEE Transactions on Power Electronics 32, 7534 (2017).

# 11. Appendix