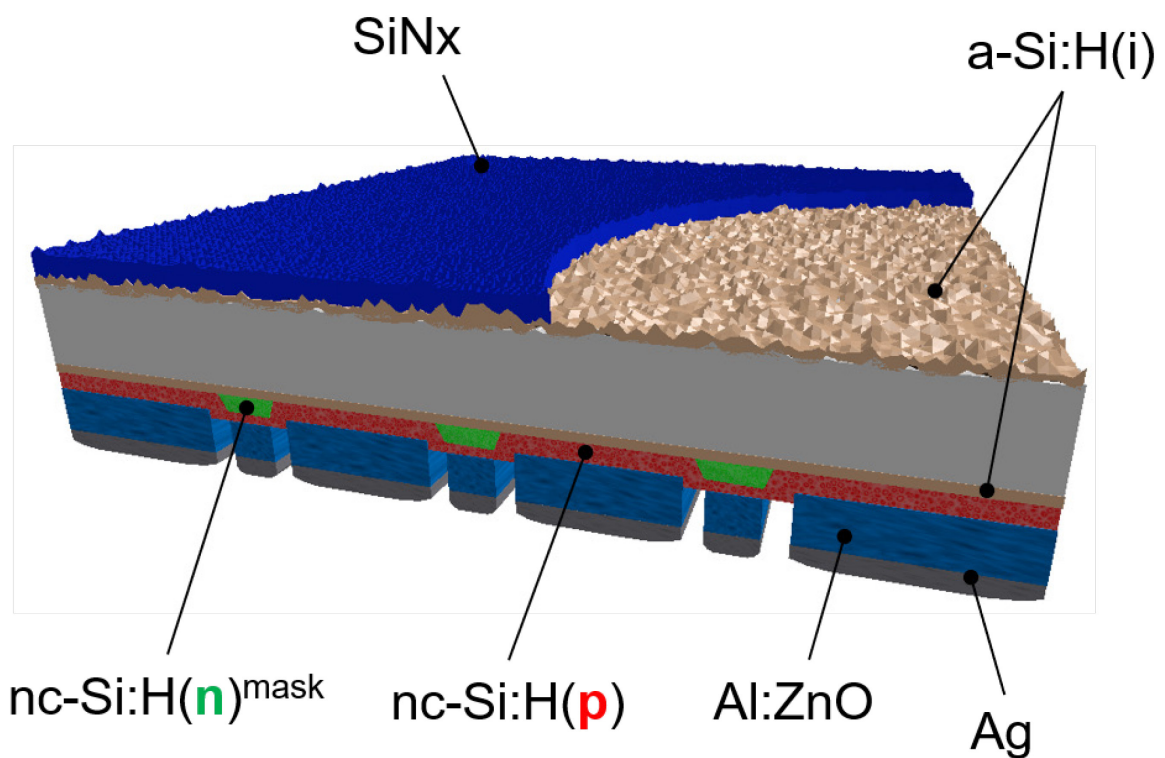




Public report

HALBION

Half bifacial back-contacted silicon heterojunction solar cells



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Summary

The HALBION project aims at nurturing the large-scale deployment of PV electricity by fostering the development of highly efficient solar cells produced at competitive cost. Along these lines, back-contacted crystalline silicon solar cells with passivated contacts demonstrated the highest conversion efficiencies for single junction, crystalline silicon-based solar cells. In spite of these impressive results, and regardless of the materials chosen for the passivated contacts, severe concerns still remain about the cost-effectiveness of such back-contacted solar cell technologies. In the frame of the HALBION project, a route is proposed to decrease the cost of ownership (CoO) of back-contacted amorphous/crystalline silicon heterojunction (BC-SHJ) solar cells by dramatically simplifying the fabrication of the individual devices as well as the module interconnection of these latter, the so-called "tunnel-IBC" technology.

Remarkably, the HALBION project demonstrated tunnel-IBC devices with power conversion efficiencies up to 25.4 % on 200 cm² designated area and 24.4 % at full M2 wafer size. A cost-efficient Ag-free metallization approach for these devices was successfully developed and will be implemented at pilot production level. Indium-free transparent conductive oxides (TCOs) were investigated and integrated into improved rear reflectors demonstrating short-circuit current densities up to 42.5 mA/cm², hence only 0.2 mA/cm² short from the Kaneka's IBC world record. Finally, the HALBION project provided insightful results into the laser cutting of half-IBC solar cells for reducing the interconnection losses at module level.

Importantly, all results obtained in HALBION are valuable steppingstones to be used in the SFOE's P+D SIRIUS project, started 1st of May 2021, aiming at developing a tunnel-IBC pilot line in Switzerland.

Résumé

Le projet HALBION vise à favoriser le déploiement à grande échelle de l'électricité photovoltaïque en encourageant le développement de cellules solaires hautement efficaces et produites à un coût compétitif. Dans cette optique, les cellules solaires en silicium cristallin à contact arrière avec des contacts passivés ont démontré les rendements de conversion les plus élevés pour des cellules solaires à base de silicium cristallin à jonction unique. En dépit de ces résultats impressionnants, et quels que soient les matériaux choisis pour les contacts passivés, d'important défis et interrogations subsistent concernant la rentabilité de ces technologies de cellules solaires à contact arrière. Dans le cadre du projet HALBION, une approche est proposée pour réduire le coût total de possession (cost of ownership CoO) des cellules solaires à hétérojonction de silicium amorphe/cristallin à contact arrière (IBC-SHJ) en simplifiant considérablement la fabrication des dispositifs individuels ainsi que l'interconnexion des modules de ces derniers en utilisant la technologie dite "tunnel-IBC".

De manière remarquable, le projet HALBION a démontré des dispositifs de type tunnel-IBC avec des rendements de conversion de puissance allant jusqu'à 25,4 % sur une surface désignée de 200 cm² ainsi que 24,4 % sur une cellule solaire de taille M2. De plus, une approche rentable de métallisation sans argent pour ces dispositifs a été développée avec succès et sera mise en œuvre au niveau de la production pilote. Des oxydes conducteurs transparents (TCO) sans indium ont été étudiés et intégrés



dans des réflecteurs arrières améliorés présentant des densités de courant de court-circuit allant jusqu'à 42,5 mA/cm², soit seulement 0,2 mA/cm² de moins que le record mondial IBC de Kaneka. Enfin, le projet HALBION a fourni des résultats très intéressants sur la découpe au laser de demi-cellules solaires IBC pour réduire les pertes d'interconnexion au niveau des modules.

Il est important de noter que tous les résultats obtenus dans le cadre d'HALBION constituent des tremplins précieux pour le projet P+D SIRIUS de l'OFEN, qui a démarré le 1er mai 2021 et vise à développer une ligne pilote IBC en Suisse.

Zusammenfassung

Das Projekt HALBION zielt darauf ab, den Einsatz von PV-Strom in grossem Massstab zu begünstigen, indem die Entwicklung hocheffizienter Solarzellen zu wettbewerbsfähigen Kosten vorangetrieben wird. Zu diesem Zweck zeigen rückseitenkontaktierte kristalline Silizium-Solarzellen mit passivierten Kontakten die höchsten Umwandlungswirkungsgrade für kristalline Silizium-Solarzellen mit nur einem Halbleiterübergang. Trotz beeindruckenden Ergebnissen und ganz gleich, welche Materialien für die passivierten Kontakte gewählt werden, bestehen nach wie vor grosse Vorbehalte hinsichtlich der Kosteneffizienz solcher rückseitig kontaktierten Solarzellentechnologien. Im Rahmen des Projekts HALBION wird ein Weg zur Senkung der Gesamtkosten (Costs of ownership, CoO) von rückseitig kontaktierten amorph/kristallinen Silizium-Heteroübergang-Solarzellen (BC-SHJ) vorgeschlagen, indem die Herstellung der einzelnen Zellen sowie deren Modulverschaltung, die so genannte "Tunnel-IBC"-Technologie, drastisch vereinfacht wird.

Im Rahmen des HALBION-Projekts wurden Tunnel-IBC-Solarzellen mit einem Wirkungsgrad von bis zu 25,4 % auf einer Fläche von 200 cm² und 24,4 % bei voller M2-Wafergrösse demonstriert. Ein kosteneffizienter Silber-freier Metallisierungsansatz für diese Zellen wurde erfolgreich entwickelt und wird in der Pilotproduktion eingesetzt. Es wurden Indium-freie transparente leitfähige Oxide (transparent conductive oxides, TCOs) untersucht und in verbesserte Rückseitenreflektoren integriert, die Kurzschlussstromdichten von bis zu 42,5 mA/cm² aufweisen und damit nur 0,2 mA/cm² unter dem IBC-Weltrekord der Firma Kaneka liegen. Schließlich lieferte das HALBION-Projekt aufschlussreiche Ergebnisse über das Laserschneiden von Half-IBC-Solarzellen zur Verringerung der Verschaltungsverluste auf Modulebene.

Alle im Rahmen von HALBION erzielten Ergebnisse sind wertvolle Grundlagen für das am 1. Mai 2021 gestartete BFE-Projekt SIRIUS, das auf die Entwicklung einer Tunnel-IBC-Pilotlinie in der Schweiz abzielt.



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1 Introduction

1.1 General context

Back-contacted crystalline silicon solar cells with passivated contacts demonstrated the highest conversion efficiencies for single junction, crystalline silicon-based solar cells [1]. Despite these impressive results, and regardless of the materials chosen for the passivated contacts, severe concerns still remain about the cost-effectiveness of such back-contacted solar cell technologies. For several years, CSEM together with Meyer Burger Research have been working towards a route to decrease the cost of ownership (CoO) of back-contacted amorphous/crystalline silicon heterojunction (BC-SHJ) solar cells by dramatically simplifying the fabrication of the individual devices as well as the module interconnection of these latter, the so-called “tunnel-IBC” technology [2].

The first objective is reached using a tunnelling electron contact patterned via in-situ shadow mask to fabricate the BC-SHJ devices, and the second one by using the Smart Wire Connection Technology (SWCT) to ensure their module interconnection. Calculations using realistic assumptions show that this approach results in a CoO challenging the one of the currently established PERC technology, thus paving the way towards the successful industrial spread of BC-SHJ devices. Moreover, our tunnel-IBC devices feature indium-free TCO and are being developed towards being silver-free as well, hence ensuring the sustainability of this technology for TW-scale deployment [3].

1.2 Scope of the project & content of this report

The HALBION project aimed at nurturing the large-scale deployment of PV electricity by fostering the development of highly efficient solar cells produced at competitive cost. Along these lines, the workhorse of the HALBION project was the “tunnel-IBC” technology, a very lean yet remarkably efficient back-contacted amorphous/crystalline silicon heterojunction solar cell technology developed by CSEM and Meyer Burger Research. More specifically, the HALBION project was committed to:

- Bring tunnel-IBC solar cells to record efficiency levels, with > 26 % efficiency at lab scale and > 25.5 % efficiency on full size industrial Cz wafers, demonstrating scientific evidences and technological solutions to overcome the actual performance losses;
- Demonstrate the relevance of half tunnel-IBC solar cells, hence potentially paving the way towards high performance IBC modules with very low cell-to-module losses;
- Foster the development of the metrology tools required to accurately measure such innovative devices.

In addition to this scientific and technological knowledge and achievements, the HALBION project reinforced the visibility of the project stakeholders as top-notch institutes in the field of PV by disseminating the project results at national conferences. The HALBION project also provided important innovations that will be considered for future IP protection.

This public report features an overview of the research activities carried out during the course of the project, as well as the major milestones and the deliverables achieved. Finally, this report highlights the main achievements of the whole HALBION project fulfilled over the two years.



2 Activities and results

2.1 Workpackage 2: Building blocks for achieving > 25 % efficiency on full M2 wafer

2.1.1 Aim of Workpackage 2

WP2 (Building blocks for achieving > 25 % efficiency on full M2 wafer) aims at mitigating the remaining loss sources in the current state-of-the-art IBC-SHJ devices. These are namely: (i) the lateral transport losses, (ii) the edge losses, and (iii) the optical and the electrical losses in the rear electrode. Additionally, WP2 targets a strong simplification of the global process flow for the back-end of IBC-SHJ solar cells.

2.1.2 Simulations with guidelines for best suited pitch and gap width (D2.1a)

Procedures & methodology

For the sake of memory, the architecture and the process flow of tunnel-IBC devices are recalled in Figure 1. The accurate evaluation of the series resistance (R_{series}) in tunnel-IBC devices, and its relevant breakdown into separated loss sources, are crucial for a proper mitigation of the transport losses within such devices, and hence for the chase towards higher efficiencies. In the frame of HALBION, several analytical models to evaluate the R_{series} of tunnel-IBC devices have been set up and compared. Using with the analytical model presented in [4], the R_{series} losses breakdown of our certified 25.0 % efficient tunnel-IBC device presented in [5] is depicted in Figure 1.

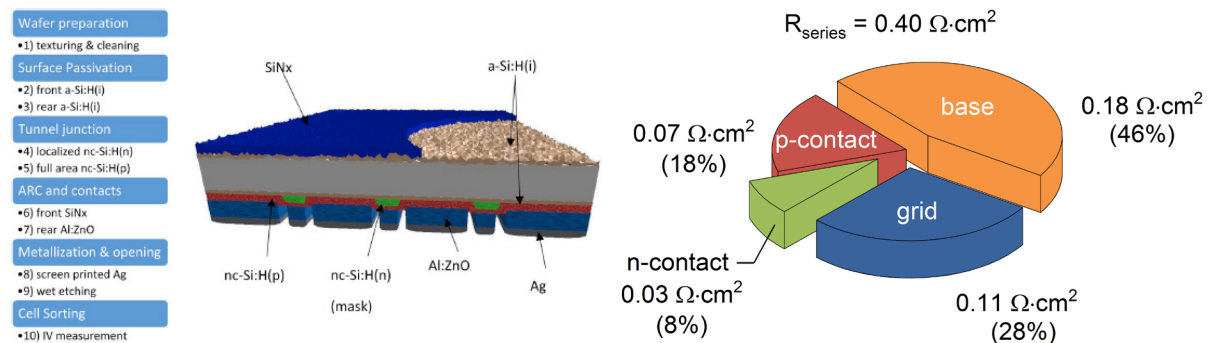


Figure 1. Left: Process flow and sketch of a tunnel-IBC device [7]. Right: Actual R_{series} losses breakdown of the record 25.0 % efficient tunnel-IBC device presented in [5].

Obviously, the major contribution to the overall R_{series} losses owes to the base losses, e.g. the electrical losses owing to the lateral transport of carriers to their contacts. These base losses are directly proportional to the tunnel-IBC pitch: the smaller the pitch, the lower the electrical losses occurring in the base. Still using the analytical model presented in [4], one can assess how much FF gain is expected by reducing the pitch. Along these lines, Figure 2 compares the absolute R_{series} losses and the relative shares of the different loss sources in the case of a 2.50 mm pitch (the one used in the device presented



in Figure 2) and a 1.26 mm pitch (targeted pitch in the frame of HALBION). First and foremost, one can notice that the simulated R_{series} absolute value and its breakdown for the 2.50 mm pitch (Figure 2 left) are in relative good agreement with the values obtained on a real device (see Figure 2). This gives confidence that even if the current R_{series} model does not capture all the physical phenomena ruling the carrier transport within tunnel-IBC devices, it offers a reasonably trustable platform to assess potential R_{series} mitigation solutions. Along these lines, Figure 2 right plots the R_{series} losses in the case the current pitch would be halved to 1.26 mm: in this case, the electrical losses in the base are reduced to $63 \text{ m}\Omega\cdot\text{cm}^2$, and a FF close to 84 % is expected.

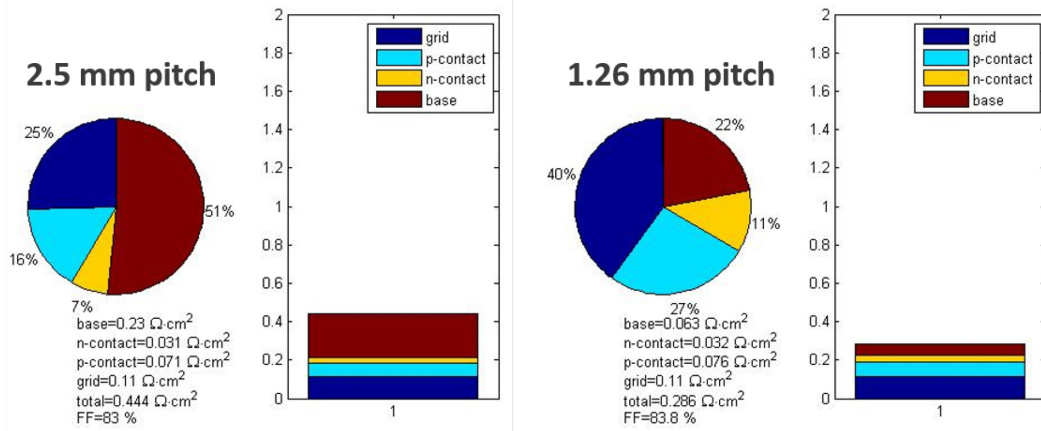


Figure 2. Calculated R_{series} losses breakdown in the case of a tunnel-IBC device with a 2.50 mm pitch (left) and a 1.26 mm pitch (right).

Note that these results obtained with our simple analytical R_{series} model have been – at least qualitatively – validated by state-of-the-art finite elements simulations performed in earlier projects (see e.g. [6]). All of them form our rationale for the reduction of the rear pitch from its current 2.50 mm value towards 1.26 mm.

Challenges in processing tunnel contacts with reduced width

Transfert length method (TLM) measurements were performed to measure the specific contact resistivity (ρ_c) of tunneling electron contacts patterned through shadow masks with varying slit widths (from A, the narrowest to G, the largest slit). The typical measurement setup is depicted in Figure 3, and the experimental results are plotted in Figure 4 and compared to the un-masked case. As evidenced from Figure 4, a dramatic increase of ρ_c is to be seen for narrower shadow mask slit widths. Moreover, regardless of the slit width, the patterned ρ_c value is always larger than the one obtained in the un-masked case. This means that the experimental values used as input data to the R_{series} modeling presented above in Figure 2 are a lower bound of the actual ones, and consequently, that the contact resistance losses obtained from this model are under-estimated.

Attempting at mitigating this detrimental effect, longer deposition times (from t_1 , the shortest, to t_4 , the longest time) were used to compensate the increased shadowing losses caused by the reduction of the shadow mask slit width. The results are plotted in Figure 5. Clearly, a reduction of ρ_c is obtained if a longer deposition time is used for a given slit width. Hence, a $40 \text{ m}\Omega\cdot\text{cm}^2$ ρ_c value seems reachable for the middle D slit. However, longer deposition times eventually induce low lifetime after deposition of the p-type layer. Values as low as 300 μs have been measured, which is clearly incompatible with the high



lifetimes required for 26 % efficient tunnel-IBC devices. Process optimization is ongoing, but these experimental results clearly pinpoint the challenges in obtaining low enough ρ_c values for the tunnel contact when moving towards narrower pitches.

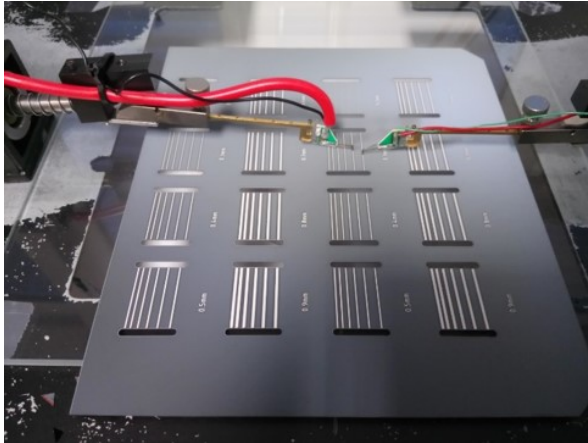


Figure 3. Experimental setup for the measurement of the specific contact resistivity of shadow mask-patterned tunneling electron contacts.

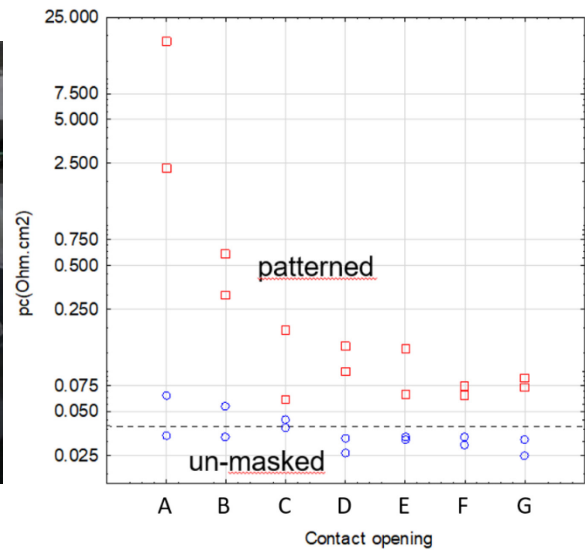


Figure 4. Variation of the specific contact resistivity of patterned tunneling electron contacts as a function of the shadow mask slit width (from A, the narrowest to G, the largest slit), compared to the un-masked case

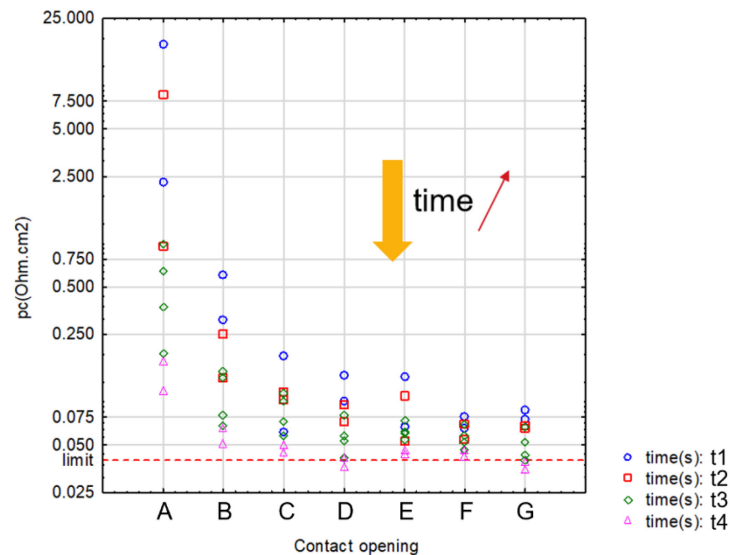


Figure 5. Variation of the specific contact resistivity of patterned tunneling electron contacts as a function of the shadow mask slit width (from A, the narrowest to G, the largest slit), for different deposition times (from t1, the shortest, to t4, the longest time).



Open questions related to the R_{series} model

In addition to the experimental challenges reported above, several questions remain open regarding the validity of our current R_{series} model for tunnel-IBC devices. First, as suggested by one of our recent paper [7], it should be relevant to include in this model the contribution of the lateral transport of the minority carrier (holes here), as well as the current spreading and crowding effects. However, the application of this model to our current tunnel-IBC devices systematically yield an overestimated value of the R_{series} .

Second, the estimation of the FF_0 and the iFF of tunnel-IBC devices has been found to differ notably when calculated using the Bowden approach [8] or when taken from the lifetime curve (see Table 1). This discrepancy is confirmed by photoluminescence (PL) mapping (data not shown). Moreover, the comparison of PL images taken under MPP condition to those taken under low illumination (as requested for the Bowden analysis) reveal meaningful differences. Indeed, as can be seen in Figure 6, the PL signal under the electron fingers appears brighter under MPP load than at low illumination. This possibly signals that the superposition principle is not valid in tunnel-IBC devices (i.e. the short-circuit current density does not equal the photogenerated current, probably because of light shunt and/or other transport issues in tunnel-IBC devices), and therefore estimating the illumination conditions from the J_{sc} might turn erroneous. Last but not least, PL images taken at J_{sc} condition show a clear accumulation of carriers below the electron contact (see Figure 7), which suggest that carriers are not efficiently extracted from our devices. Further work is needed to better understand these experimental finding.

Table 1. Comparison of the FF_0 and the iFF values obtained from the Bowden analysis and from the lifetime curve for a 24.4 % efficient tunnel-IBC device.

Method	Eff. (%)	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF (%)	FF_0/iFF (%)	R_{series} ($\Omega \cdot \text{cm}^2$)
LIV/Bowden	24.4	41.5	731	80.5	84.5	0.71
Lifetime	-	-	-	-	86.0	-

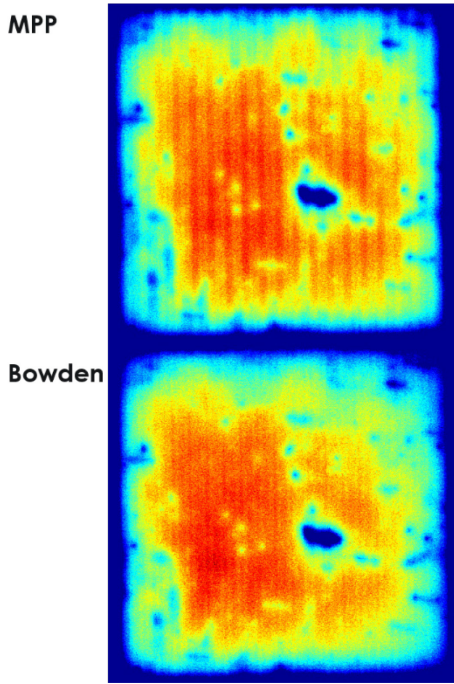


Figure 6. PL images of a tunnel-IBC device taken under MPP condition (top) and under low illumination (bottom).

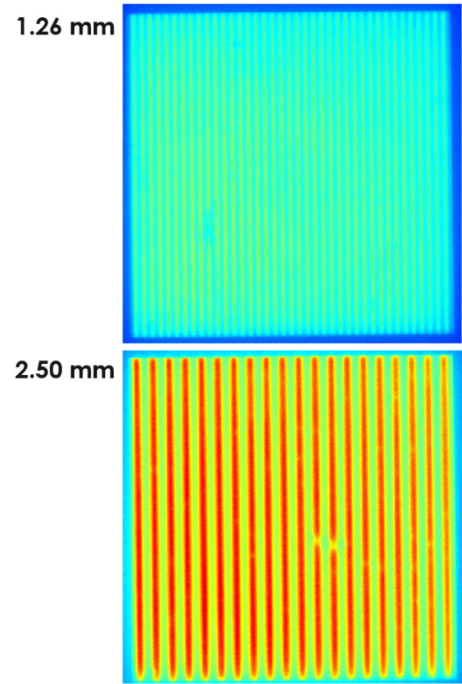


Figure 7. PL images taken at J_{sc} condition for a tunnel-IBC device with a 1.26 mm pitch (top) and 2.50 mm (bottom).

2.1.3 Opening design impact on resulting transferred pattern (D2.1b)

Raman spectrometer for profilometry

A large variety of tools for non-destructive layer thickness measurements of thin film depositions exist in the microelectronic industry, e.g. Spectroscopic ellipsometry (SE) or stylus profilometry just to name some of the most common. However, most of these tools are not applicable in solar cell applications due to the micron-sized textured surfaces of the wafers. The difference in orders of magnitude between the a-Si:H layer depositions of 5-30 nm and the textured surfaces with pyramids of 4-10 μm in height is about 3. In addition, a spatial resolution of the order of 10 μm is required for accurate mapping of deposition stripes with 1 mm in width. One of the only methods for accurate thickness profiling in such situations is the Raman scattering spectroscopy.

Incident photons on a crystalline material can undergo inelastic scattering while interacting with lattice phonons. Those photons are then back-scattered with a different energy than the incident ones, characterised by a Raman frequency shift. Measuring the back scattered light for crystalline silicon results in a sharp peak intensity around 520 cm^{-1} . Absorption in overlying amorphous silicon layers attenuate the intensity of the crystalline Raman signal allowing for mapping of the amorphous silicon thickness. The light absorption in a-Si:H follows Lambert-Beer law described in Equation 1. I_0 is the peak intensity of c-Si without any overlying layers in units of Raman counts and I the measured intensity at any point of the stack.

$$I = I_0 e^{-2\alpha d} \Rightarrow d = 1/2\alpha \ln(I_0/I) \quad (\text{Eq. 1})$$



The absorption coefficient α [cm^{-1}] is linked to the refractive index of the deposited layer as well as the wavelength of the incident laser light. In the frame of this work, a value of $\alpha = 1.852 \times 10^5 \text{ cm}^{-1}$ has been taken from ellipsometry for a-Si:H [9]. d is therefore the thickness of the overlying a-Si:H layer. The factor of two in the exponential comes from the fact that the back scattered light from the c-Si bulk has travelled twice through the overlying amorphous stack. The equation can be solved for the a-Si:H thickness d as shown above. It is important to mention that the resulting thicknesses may deviate from the real thickness due to optical reflections and the fact that absorption coefficient may vary between the different growth types of a-Si:H (amorphous or micro-crystalline). However, conducted SE measurements have shown that the above mentioned value for is in the reasonable range for our stacks.

An illustration of the Raman intensity profiles is given in Figure 8. In the area without a-Si:H deposition (blue in the left image, bottom profile) a clear distinct peak around 520 cm^{-1} with a large number of counts is visible. Regions with deposition through the shadow mask (purple, top profile) exhibit a much weaker crystalline signal. In addition, a large continuous spectrum is visible between 450 cm^{-1} and 500 cm^{-1} since amorphous silicon has no repetitive lattice configuration.

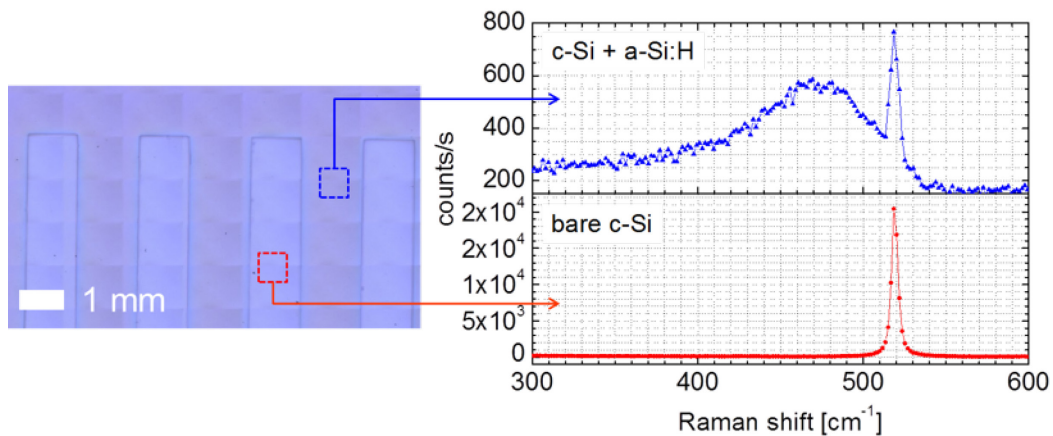


Figure 8. Illustration of Raman spectroscopy for profilometry of thin patterned amorphous silicon layers.

Experimental setup

The measurement setup consists of a MonoVista CRS+ confocal Raman microscope from S&I. Further information on the machine can be found in [10]. A blue laser with a 442nm wavelength combined with an optical magnification lens of x10 has been used. In this configuration, the required acquisition time for accurate profiling was between 20 and 30s. Using an xy-stage, line scans are performed with 10 – 20 μm step sizes. The laser spot diameter with this lens is 9 μm and therefore sufficient for these step size dimensions. A python code has been implemented for platform independent and automated data analysis of the resulting Raman profiles. At each step of the scan, the crystalline peak has been fitted by a Lorentzian function followed by an integration in the range $[510 \text{ cm}^{-1}, 535 \text{ cm}^{-1}]$ to evaluate the peak intensity with reduced noise. Note that such Raman spectrometry profilometry show only sub-nm fluctuations if performed at the same location, making it a very reliable measurement tool for the purpose of this internship. Nevertheless, due to the optical nature of the measurement, light diffraction at the textured pyramid faces causes spatially resolved fluctuations of $\pm 2.5 \text{ nm}$. Therefore, most profiles have



been taken as the average over two or three individual ones on a same deposition stripe but with $\pm 100 \mu\text{m}$ displacement in y direction (considering a profiling direction in x).

Definition of parameters for morphology characterization

For the quantitative evaluation of the cross-section shapes, new characterization parameters were needed. As first, the squareness S_q of a finger profile has been defined as fraction of the integrated finger area and the area of a perfect rectangular shape. S_q can be written as:

$$S_q = 1/Lh \int f(x)dx \quad (\text{Eq. 2})$$

where L is the width of the patterned finger, h is the thickness at the finger centre and $f(x)$ is the function containing the profile points. Therefore, the squareness ranges between 0 and 1. The optimal finger profile with optimal depositions would result in S_q equal to unity. Experimentally the obtained values range between 0.8-0.95.

As a second characterization method, the edges of the deposited fingers have been fitted on one side using an inverse exponential function h_{fit} as follow:

$$h_{\text{fit}}(x) = h \cdot (1 - e^{-x/p}) \quad (\text{Eq. 3})$$

where $p [\mu\text{m}]$ becomes the fitted parameter. A small value of p reflects a sharply increasing finger coverage whereas a large value represents a strongly tapered finger profile.

Numerical simulations

An equivalent model has been built for a PECVD chamber using the COMSOL Multiphysics Simulation software. The concept is to simulate the gas transport in the chamber as purely diffusive and do not consider the physics and reactions happening in the plasma core. It can be shown that this approach, although being a very crude approximation, leads to a reasonable representation of the real situation [11]. This takes away the complexity of simulating plasma systems while still resulting in accurate trends for deposition properties. The PECVD chamber is modelled by a two-dimensional cross section representing the boundary domain as illustrated in Figure 9. The top surface consists to a large fraction of the shower head represented as a gas inlet of SiH_4 and H_2 . Both side walls of the chamber are gas outlet surfaces. Within the 2D surface, the chemical decomposition of $\text{SiH}_4 \rightarrow \text{Si} + 2 \text{H}_2$ occurs with a certain probability. Each surface of the boundary has a particle flux [$1/(\text{m}^2\text{s})$] of Si radicals that can be multiplied by a deposition efficiency, or sticking coefficient, in order to obtain the effective flux contributing to the deposition. This quantity can further be related to a deposition rate of solid a-Si:H on a given surface by dividing by its mass density. Since the difference in density between amorphous and crystalline silicon is found to be only 1.7%, a value of $4.9 \times 10^{22} \text{ cm}^{-3}$ has been considered [12]. Multiplying the resulting deposition rate by the actual deposition time results in thickness profiles which turn out to have very good accordance in order of magnitude to real measurements. A finite element non-linear solver then finds the stationary solution to the fluid equations considering the above-mentioned boundary conditions and using a fine spatial mesh.

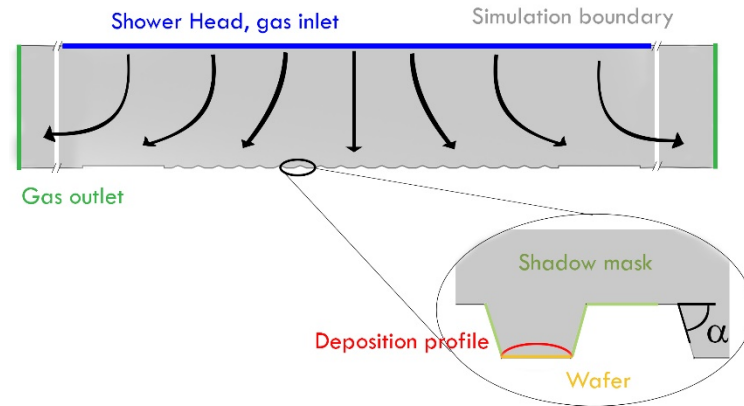


Figure 9. Scheme of simulation boundary, nomenclature and flow with definition of the side wall inclination angle α .

Dependence on mask finger slit width and pitch

Three shadow masks were investigated. The mask dimensions are listed in Table 2 and the resulting profiles of the nc-Si:H(n) layer is shown in Figure 10a. Central deposition height as well as squareness values for the different masks are illustrated in Figure 11a and Figure 11b.

As first observation one can see that the central thickness increases linearly for all masks though with slightly increasing rate when increasing the slit width, proving a nearly constant deposition rate. Moreover, the deposition is lower for both masks vT1 and vT2 with smaller slit width, in agreement with what has been found in [9]. However, an unexpected observation is that reducing the finger pitch (for a given slit width) results in a reduction of deposited thickness (compare vT1 and vT2 in Figure 11a). In terms of squareness, no clear dependence can be drawn with deposition time. Nevertheless, smaller slit widths show overall lower squareness values.

In simulation, the slit width has been varied between 300-900 μm as shown in Figure 10b while the mask finger width is kept constant at 1.6 mm. One can observe that the thickness trend is equal to the experimental situation even though the quantitative increment differs (~50% thickness when going from 900 μm to 500 μm). The simulated squareness appears independent of the slit width and remains quantitatively low at around 70%.

Table 2. Dimensions of three masks under investigation at CSEM.

Design	ID	Pitch (mm)	w_p (μm)	w_n (μm)
Large pitch	vD1	2.500	1600	900
Small pitch	vT1	1.260	760	500
Intermediate pitch	vT2	1.700	1200	500

w_n (resp. w_p): width of the electron (resp. hole) collecting fingers.

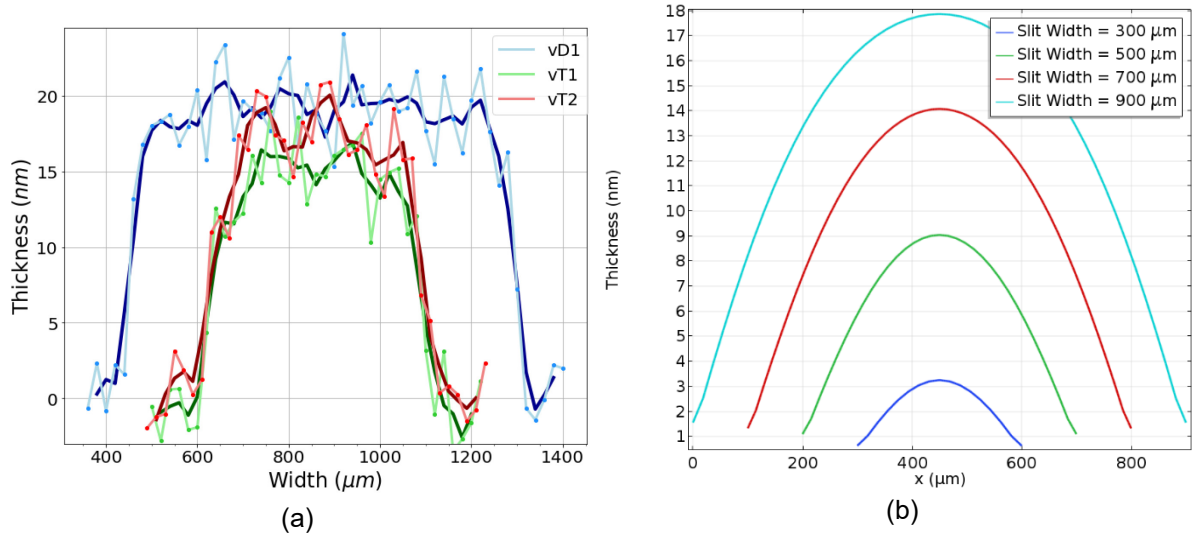


Figure 10. Measured (left) and simulated (right) cross-section of IBC fingers as a function of the aperture of the IBC mask.

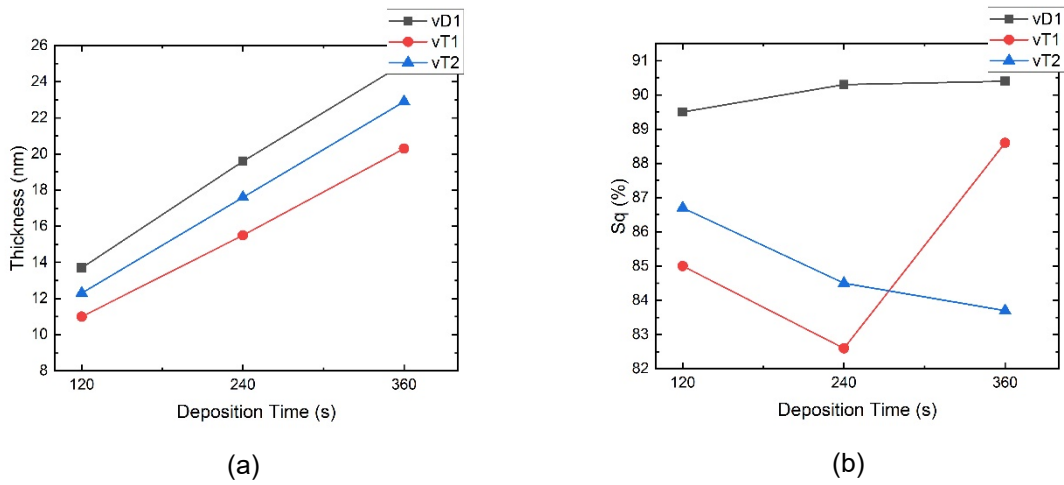


Figure 11. Variation of the patterned layer thickness (a) and squareness (b) as a function of the mask geometry.

Additionally, the impact of the mask thickness was studied using the COMSOL simulation. Figure 12a shows the resulting profiles while Figure 12b displays the resulting trends in terms of thickness and squareness. It is visible that reducing the mask thickness, subsequently the step height, increases the central deposition height and more importantly, clearly increases the squareness in a squared dependence. Nevertheless, the deposition at the very edge continues to be mostly unaffected and remaining at a few nanometers.

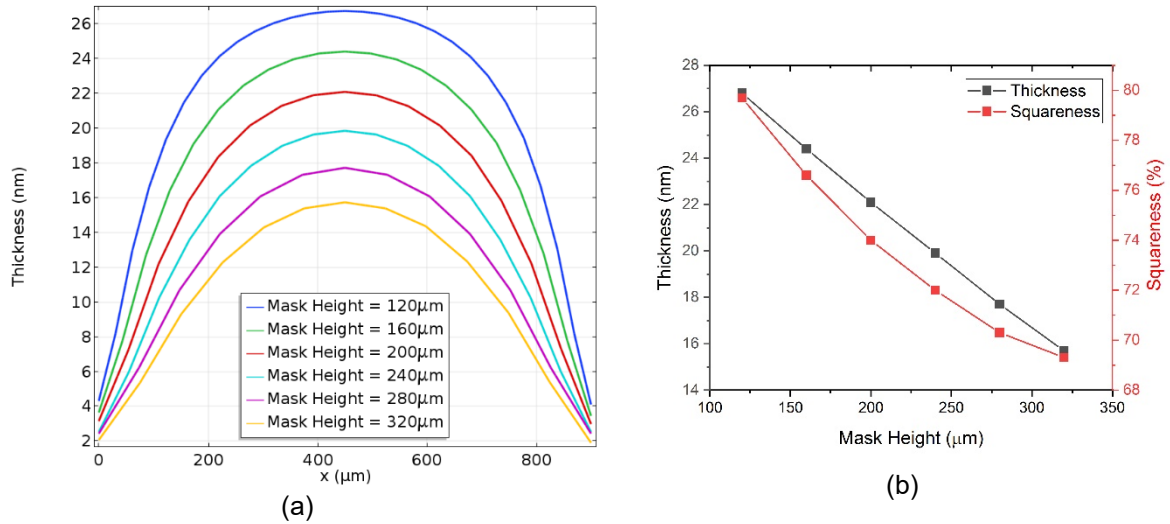


Figure 12. Simulation profiles (a) and profile parameters (b) as a function of the mask thickness.

2.1.4 Matrix compiling and comparing the optical, electrical, and patterning properties of various materials for the TCO/metal rear electrode of IBC-SHJ devices (D2.3a)

Task 2.3a aims at thoroughly screening indium-free TCO materials for the rear electrode of IBC-SHJ devices, and rating them regarding their optical losses, their selectivity and contact properties, as well as their ease of patterning. In this regard, Boron-doped Zinc Oxide (BZO) is investigated and compared to the actual indium free Aluminium Zinc Oxide (AZO) used inside the rear reflector of CSEM and MBR IBC solar cells. This TCO is developed with the aim to target a higher optical response than AZO to engineer bifacial IBC solar cells.

Deposition process and material properties

BZO layers are deposited by low pressure chemical vapor deposition (LPCVD). During the deposition, the substrate is heated by an aluminum hot plate and the gases used are diethylzinc (DEZ, $\text{Zn}(\text{C}_2\text{H}_5)_2$), vapour H_2O and diborane (B_2H_6) diluted to 1% in argon (Ar). The doping is augmented by increasing the amount of diborane, such as the higher the flow rate, the stronger the doping. The doping is given

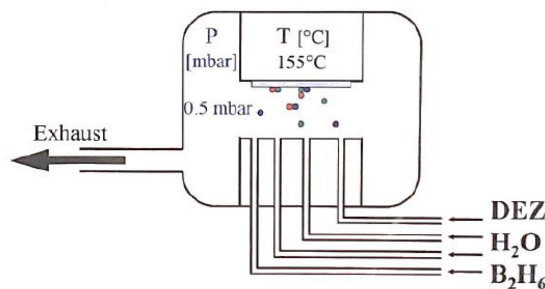


Figure 13. Schematic description of the BZO deposition by LPCVD.



by the ratio (B_2H_6/DEZ) and this value is typically between 0 and 2 [13]. A schematic description of BZO LPCVD deposition system is given in **Figure 13**. In parallel, AZO layers are deposited by RF physical vapor deposition (PVD) with a Al_2O_3ZnO 2/98 wt% target. The doping of the AZO is varied with the oxygen (O_2) quantity in the deposition gases, such as the higher the O_2 quantity, the lower the doping. The O_2 quantity is hereafter referred with the ratio of Ar/O_2 .

Table 3 shows the materials properties of the BZO and AZO layers developed with different doping (AZO with 100/0 to 100/5 of Ar/O_2 and BZO from 11 to 56 of B_2H_6/DEZ). The sheet resistance of AZO layers is always higher than BZO layers and go up to a very high value of 50'000 Ohm/sq. BZO layers presents very low Rsh values down to 7 Ohm/sq. Looking at the mobility, as expected AZO layers present very low values with a significant diminution among the O_2 quantity increase. In contrast, BZO present high mobility values between 39-43 cm^2/Vs . However, to reach such low Rsh and high mobility, BZO layers feature very high thickness between 2300 – 3800 nm. This could explain the higher absorptance of BZO layers compared to AZO.

Table 3. Material properties (thickness, sheet resistance (Rsh), mobility, doping and absorptance) of the different AZO and BZO layers developed.

		Thickness (nm)	Rsh (Ohm.sq)	Mobility (cm^2/Vs)	Doping (cm^{-3})	Absorptance @1200nm (%)
AZO	100/0	145	65	13	5.00E+20	9
	100/1.5	152	300	8	2.00E+20	4
	100/3	137	48000	0.5	1.80E+20	0
	100/5	115	50000	1	1.50E+20	0
BZO	56	2300	7	39	1.00E+20	13
	37	2400	9	32	9.00E+19	9
	11	3800	14	43	3.00E+19	4.5

Integration in IBC solar cells

The BZO layers with the three different dopings of 11, 37 and 56 were integrated in actual IBC solar cells and compared to the reference AZO layer. First, the etching of the BZO layers was studied and compared to AZO etching condition. It was found that all the BZO layers was easily etched with the same chemical solution of 0.1% HCl than used for AZO with only slightly longer etching time. Thus, the ease of patterning BZO layer was validated at this stage. Second, the complete IBC cells were characterized under LIV measurements and the the resulting IV parameters are presented in **Figure 14**. It is observed that the three BZO layers lead to significantly lower J_{sc} which is explained by the higher absorptance of these layers which is mainly due to their important thickness. The FF is significantly impacted by the BZO doping with an increase of the FF with the doping augmentation presenting a gain up to 30.8%_{abs}. This demonstrates the importance of the BZO doping to provide high selectivity and low series resistance. Interestingly, similar V_{oc} than AZO was reached with the highest doped BZO layer. Despite low J_{sc} and FF which put in evidence that the trade-off between conductivity and J_{sc} was not released with BZO, an efficiency of 21.1% is obtained with BZO 56. This result evidences the proof of concept of IBC solar cells integrating BZO layers inside the rear reflector.

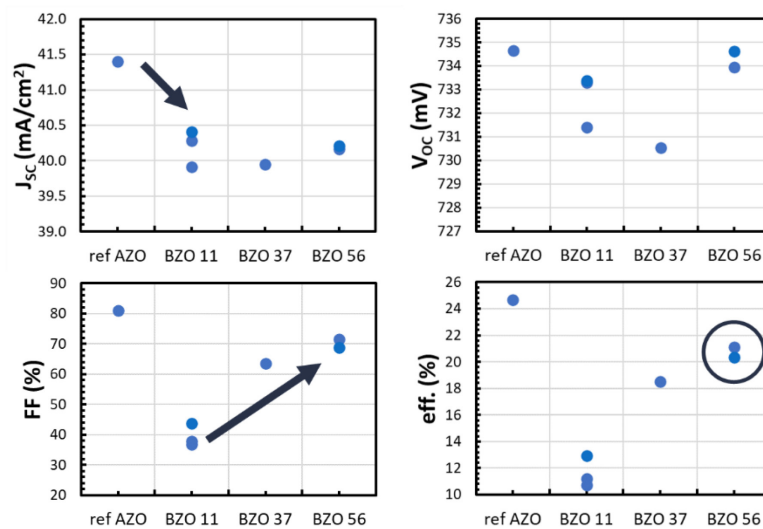


Figure 14. IV parameters of IBC solar cells integrating AZO reference layer and BZO layers with three doping referred as 11, 37 and 56.

2.1.5 Material and method for a white rear reflector demonstrating IBC-SHJ devices with $J_{sc} > 42$ mA/cm² (D2.3b)

This task aims to investigate various methods to increase the optical response of the rear reflector of IBC solar cells. To do this, the infrared reflectivity of the AZO/Ag rear stack as well as materials and methods for integrating a white rear reflector are investigated.

Improved AZO/Ag rear reflector

To improve the optical response of the AZO/Ag rear reflector, the first approach under investigation was to improve the reflectivity of the silver rear layer. The screen-printed silver layer (hereafter referred to as Ag2) is known to present a higher absorptance and lower reflectance than the silver layer deposited by PVD (hereafter referred to as Ag1). To address this issue, an additional Ag1 layer was deposited between the AZO and the Ag2 layers to improve the reflectance of the device while keeping high contact quality. To fabricate such devices, first a full area Ag1 layer was deposited on the top of the full area AZO layer. Second, inkjet printing ink was deposited on top to define the n and p-type finger pattern and the AZO/Ag1 layers were etched away. Finally, the ink was removed, and the silver grid was printed resulting in the architecture presented in Figure 15.

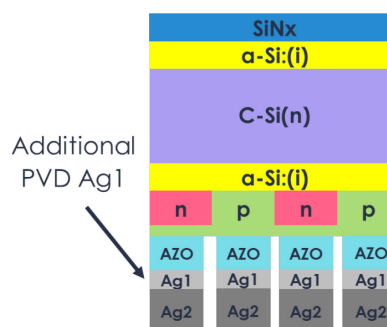


Figure 15. Schematic cross section of IBC cell with additional PVD silver (Ag1) between the AZO and the silver print (Ag2).



Figure 16 presents the IV parameters of standard IBC cells with AZO/Ag2 rear stack (referred as std) and of IBC cells with the additional Ag1 (referred as PVD Ag). Thanks to the additional Ag1 layer, a J_{sc} gain of about 0.7 mA/cm^2 is obtained compared to standard IBC cells (including AZO/Ag2 rear reflector). In addition, the FF and V_{oc} are similar for both types of IBC cells, demonstrating that the additional PVD Ag layer allow to keep good contact quality at the rear side of the device. Based on these results, further improvements were conducted and an IBC cells with the improved rear reflector stack AZO/Ag1/Ag2 demonstrated a very high current of 42.31 mA/cm^2 along with a high efficiency of 25.25% (see Figure 17). These results demonstrated the significant potential of silver deposited by PVD to improve the IR response of the rear silver grid. However, the methods presented here requires four additional process steps which render the industrialisation of such solution challenging.

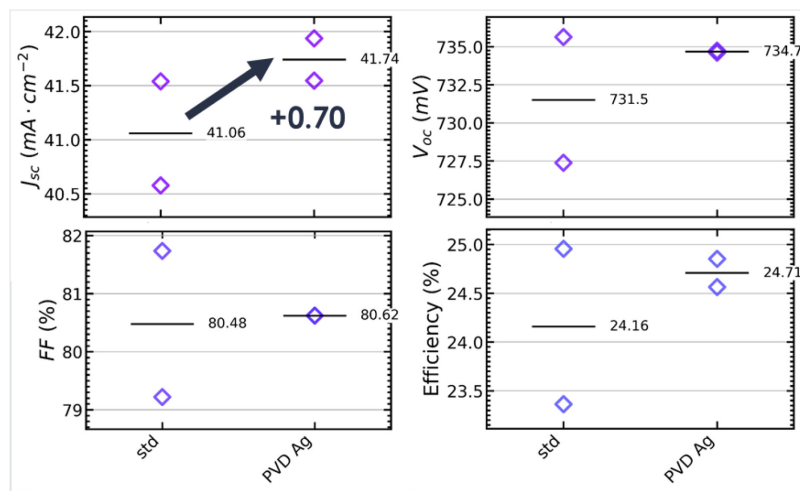


Figure 16. IV Parameters of standard IBC cells with AZO/Ag2 rear stack (referred as std) and of IBC cells with the additional Ag1 (referred as PVD Ag).

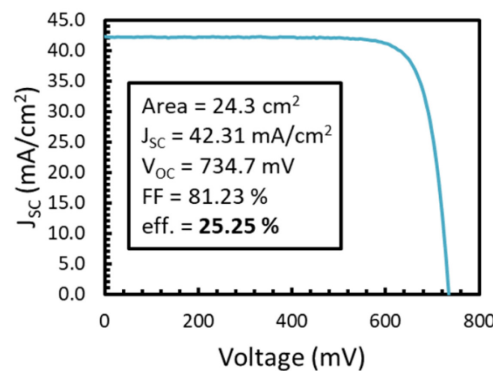


Figure 17. IV curves and parameters of the best IBC cells integrating the AZO/Ag1/Ag2 improved rear reflector.



White rear reflector:

The second approach under investigation to improve the optical response of the rear reflector was the integration of a white material layer in between the rear silver grid gaps which represent about 12% of the cell area. The deposition of the additional white layer was performed using a white paint with a high reflectance response and an appropriate brush. This advanced architecture is presented in Figure 18.

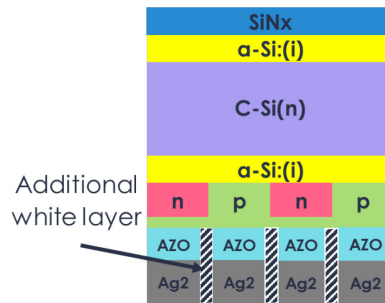


Figure 18. Schematic cross section of IBC cell with additional white layer inside the gaps between the metallic silver grid.

Figure 19 presents the IV parameters of three IBC cells A, B and C measured before and after the application of the white rear reflector material as well as a reference cell (no white rear reflector). A J_{SC} gain between 0.22 – 0.26 mA/cm² is present for the three cells A, B and C, demonstrating an improved rear reflectance thanks to the additional white layer. The FF and V_{OC} values are found to be constant resulting in an efficiency increase driven by the gain in J_{SC} . The IV curves of the best IBC cell A are presented in Figure 20 for a full area of 25.04 cm² and a designated area of 24.5 cm². This cell demonstrates the highest J_{SC} obtained during the HALBION project, with a J_{SC} going up to 42.47 mA/cm² and is only 0.2 mA/cm² short from the Kaneka's IBC world record.

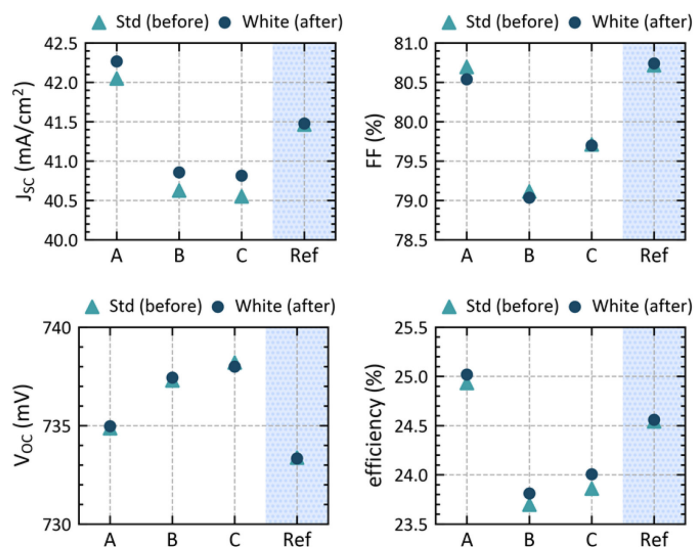


Figure 19. IV parameters of the cells A, B, C before and after the white rear reflector as well as of the reference cell (no white rear reflector).

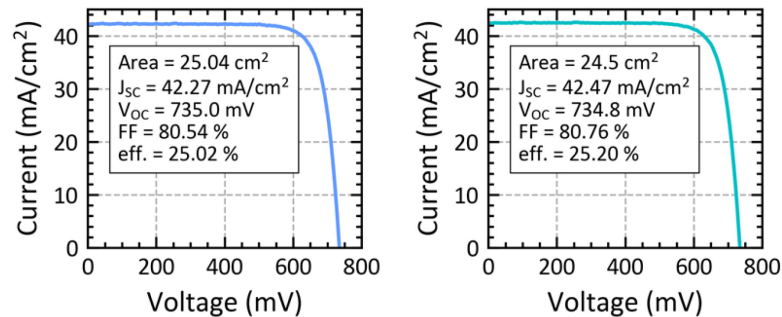


Figure 20. IV curves of the best white rear reflector cell on full area of 25.04 cm² and a designated area of 24.5 cm².

2.2 Work package 3: Half IBC-SHJ solar cells & modules developments

2.2.1 Aim of work package 3

WP3 (Half IBC-SHJ solar cells & modules developments) aims at assessing the technological feasibility and the economical relevance of half IBC-SHJ solar cells and modules, and, if relevant, developing the process flows and methods to fabricate such devices.

2.2.2 Comparison of various process flows and methods for half IBC-SHJ cells fabrication and choice of the most relevant one, clear roadmap for edge losses mitigation in half IBC-SHJ cells (D3.2a)

The investigations and developments presented in the deliverables of the task 3.1a highlighted the relevance and the promising results of ½ IBC cells and module. Based on these achievements, task 3.2a aims to further investigate and improve the process flows and methods for half IBC-SHJ cells fabrication.

LSC VS TLS wafer cutting

First, a comparison was made between our in-house laser process with commercial LSC and a supplier TLS laser process regarding the laser cutting losses from 2 different SHJ cell manufacturers. In addition, an effective characterization approach for a full-area iFF image on cells was developed by measuring the photo-luminescence (PL) with combinations of different illuminance levels and durations. This iFF mapping can quantify the different degrees of damage to the laser cutting areas and observe the dependencies of different settings of laser processes. Figure 21 (left) shows the SEM cross section of

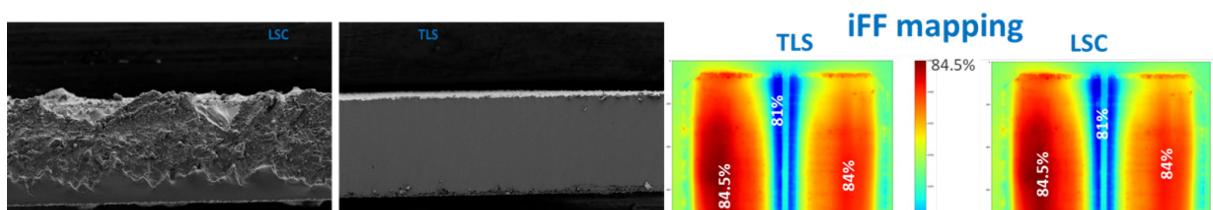


Figure 21. SEM cross section (left) and iFF mapping (right) for TLS and LSC laser cutting.



LSC and TLS wafer cutting and it is observed that LSC and TLS lead to quite different sectional profiles: when cutting with TLS, a flat cross-section is found on the sample.

Then, the two LSC and TLS laser cutting were compared using two different SHJ cell manufacturers (hereafter referred as A and B). The results are shown in Table 4, in the form of the IV key data after cutting minus the initial IV results before laser cutting (ΔX , where $X = V_{oc}, J_{sc}, FF, \eta$). To protect the rear side emitter, the laser process started on the front of the cells. In both types of cutting, the greatest losses were in the FF, and the losses in efficiency are driven by FF. These FF losses at cut edges were identified on our developed iFF mapping presented in Figure 21 (right). The cold color in the picture means less iFF and the opposite warm color means high iFF. Finally, both laser cuttings result about -0.35% efficiency losses with no significant differences. However, TLS with flat cutting cross section can be beneficial in low breakage rate on module level.

Table 4. Laser cutting losses comparison between LSC and TLS on 2 different SHJ cell manufactures.

Cell type	Laser cut type	ΔV_{oc} (mV)	ΔJ_{sc} (mA/cm ²)	ΔFF (%)	$\Delta \eta$ (%)
Cell manufacture A	LSC	-0.2	-0.19	-1.15	-0.41
Cell manufacture B		-0.86	-0.15	-0.8	-0.34
Cell manufacture A	TLS	-0.93	-0.14	-0.94	-0.36
Cell manufacture B		-0.81	-0.11	-0.96	-0.35

Δ is shown the absolute difference in 4 major IV parameters of 'post cut- initial'

Laser power optimization

Second, the LSC laser process has been optimized to obtain minimum FF and efficiency losses. In one experiment, the laser power has been decreased from batch 4 (B4) to batch 1 (B1). The strong correlation between laser power and the iFF at cutting edges is evidenced in Figure 22. The iFF values in blue marked area for all five samples have been quantified in five profiles from cutting edge to middle of the cell in Figure 22. All these results have proven the iFF mappings is a reliable characterization approach to quantify the FF and efficiency losses. With almost fully optimized process, the cutting losses can be minimized to -0.14% average and best of -0.11% in efficiency losses.

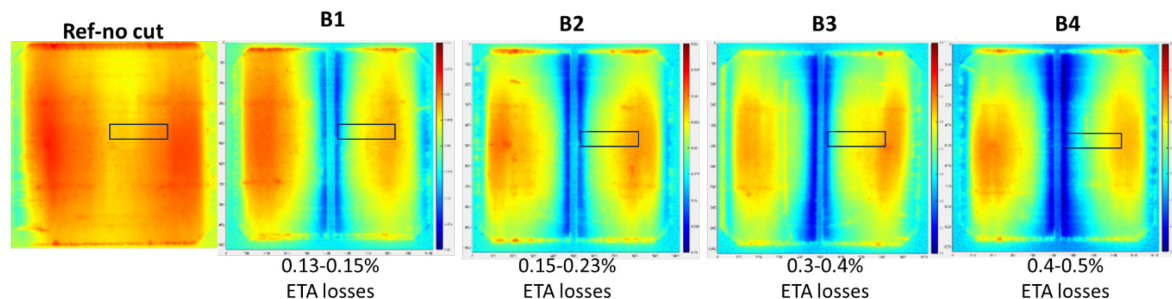


Figure 22. iFF mapping of reference w/o laser cutting, B1-B4 have increased laser power and impact on the corresponded iFF mappings.

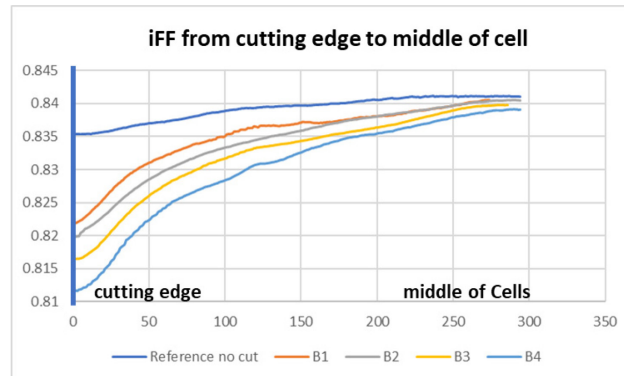


Figure 23. iFF profiles of blue marked region from cutting edge to middle of cells of the five samples in Figure 22.

Laser cutting step

Third, using the B1 laser condition, wafers were cut from as-cut wafers in half and then processed into cells (referred as C1). A special wet cassette for half-size wafers was used in this group. In addition, a thin 3 mm shadow bar was used in the middle of the PVD tray to act as an isolation mask for these half size wafers. As reference group, the full-area cells were cut in half at the end with the B1 laser condition (referred as C2), and this group was measured before and after cutting IV in order to identify the cutting losses. Finally, half-cells were tested with and without a 3 mm (1.5 mm for each edge) black tape covering the cut area during the IV test. This simulated the overlapping occurring in the “seamless” isolated half-cell modules presented in Figure 24.

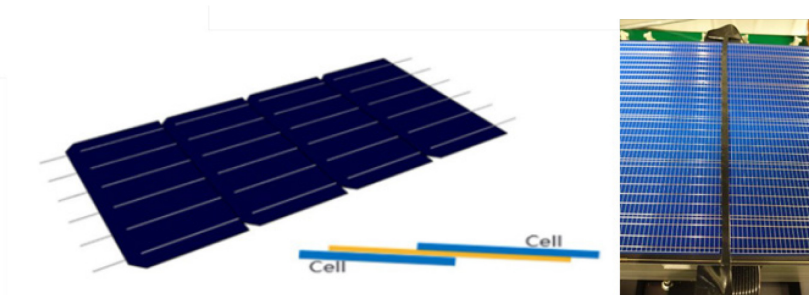


Figure 24. ‘Seamless Soldering’ with shingled half-cell string design (LONGi Solar) [14] and a simulation of 3mm black tape covered on the cutting region at IV tester for this configuration.

Figure 25 shows the iFF mapping of half-cut on as-cut wafer (left) and half-cut on finishes cell (right). It is observed that the cutting region in B1 has been fully recovered/passivated by the intrinsic a-Si layer during the PECVD process. In addition, the IV parameters presented in Table 5 show that the FF of C1 wafer is significantly higher than C2 wafer. To simulate a ‘Seamless ’ shingled half-cells in module, a 3mm width black tape was covered on the cutting edges. It has deactivated the negative impact of the damage by laser half-cutting. The FF has been increased, even more significant on C2 wafer. Without the shadow area induced by the black tape, the J_{sc} of C1 wafer has been improved strongly and it drove an approximate +0.2%abs efficiency gain.

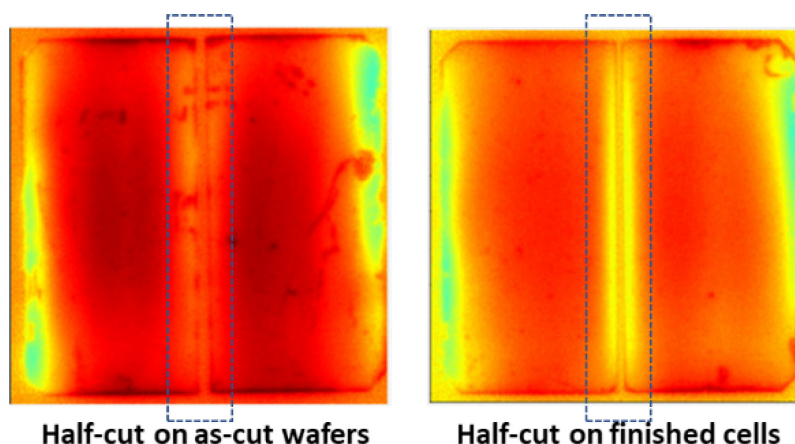


Figure 25. iFF mapping of half-cut on as-cut wafer (left) and half-cut on finished cells(right).

Table 5. IV parameters of half cut on as-cut wafers vs half-cut cells, with and w/o 3mm black tape for the IV tester.

Cell type	IV measurement	Area (cm ²)	V _{oc} (mV)	J _{sc} (mA/cm ²)	FF (%)	<i>h</i> (%)
C1-Half cut on as-cut wafers	w/o 3mm tape	244.33	735.2	37.75	78.9	21.90
C2-Half cut on finished cells			732.3	38.11	78.4	21.88
C1-Half cut on as-cut wafers	with 3mm tape	239.6	735.5	38.05	79.3	22.20
C2-Half cut on finished cells			731.7	38.12	79.0	22.03

Conclusion

A reliable iFF mapping to characterize the damage of laser cutting losses has been demonstrated. No significant cutting losses between non optimized LSC and TLS processes were observed. With fully optimized LSC process, the cutting losses in efficiency can be controlled in -0.14% range. By doing half-cut on wafer level, the cutting edge was mostly recovered/passivated by PECVD intrinsic a-Si layer, and it was proven in iFF mapping. This approach has shown potential benefits in the shingled half-cell module design.

2.3 Work package 4: Full & half IBC-SHJ solar cells fabrication

2.3.1 Aim of work package 4

WP4 aims to process high efficiency IBC solar cells by combining the different developments and improvements of WP3 and WP2 and to demonstrate cells on full wafer area with > 25.5% efficiency and >26% efficiency on 25cm².

2.3.2 Demonstration of a tunnel-IBC device with 25% and 25.5% efficiency on full wafer (D4.1a,c)

Results and status

Both deliverables were not achieved mainly due to handling problems and process instabilities. Despite these issues, the highest full area M2 wafer IBC solar cell was measured at 24.4% with a high FF of



81.1 %, V_{OC} of 742 mV and J_{SC} of 40.55 mA/cm² (see Figure 26) which validate the MBR masking technology up to the wafer edges. Note that this IBC cell was not optimized for record purpose but reflect the level of the full wafer area IBC baseline. The main causes which limit the efficiency are the multiple manipulations of the cells performed by manual handling and with different tweezers which mainly impact the wafer edges. These damages are clearly observed with PL measurements for which strong PL signal loss on the wafer edges are observed. These detrimental effects will be strongly reduced within the SFOE's SIRIUS P+D project (full automated PECVD system).

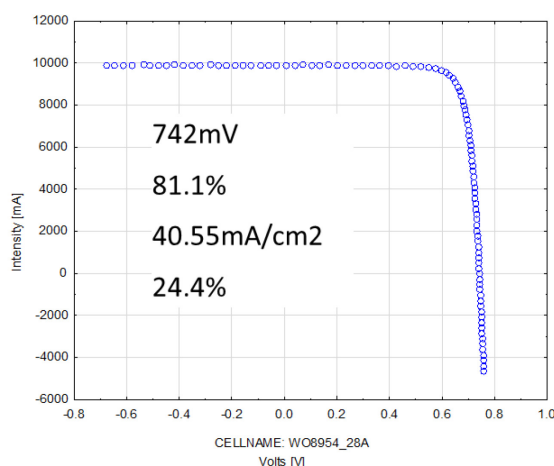


Figure 26. IV curves and cell parameters of the highest efficiency full area wafer IBC solar cell.

2.3.3 Demonstration of a tunnel-IBC device with 26% efficiency on 25 cm² (D4.1b)

Results and status

The highest results of small area IBC solar cells obtained during the HALBION project are presented on Table 6. The deliverable of 26% was not achieved however the most efficient small area IBC solar cells processed during the HALBION project presents a value of 25.25% and the highest J_{SC} presents a remarkable value of 42.47 mA/cm². These results confirm further the high performance of tunnel-junction architecture using hard mask patterning. The main challenges to target 26% efficiency arise from on one hand the small amount of IBC solar cells per batch of process and on second hand the detrimental impact of the multiple manual handling along the different process steps. These issues will be tackled within the SIRIUS project by providing a large number of solar cells per batch, advanced big data analysis and system automation.

Table 6. IV parameters of the best small area IBC cells of the HALBION project.

Study	Area	J_{SC} (mA/cm ²)	V_{OC} (mV)	FF (%)	Efficiency (%)
White rear reflector	24.50	42.47	734.8	80.76	25.20
Silver PVD	24.30	42.31	734.7	81.23	25.25



3 Evaluation of results

3.1 Status of deliverables and timing

Overall, the HALBION project has progressed well, in spite of the delays encountered due to the COVID-19 crisis and lockdown. Out of the 25 deliverables over the full HALBION project period, 22 were successfully fulfilled and the remaining three deliverables were not totally fulfilled but demonstrate already impressive results and important solutions for further efficiency improvement which are already further investigated with the SIRIUS project which started on the 1st of May 2021. This project is already pushing further the promising results of the HALBION project and investigate solution to tackle the remaining and following challenges.

3.2 Major outcome of the HALBION project

Halbion project has been run successfully with almost all deliverables achieved.

Highlights:

- 25.4% certified IBC cell on 200 cm² area.
- 24.4% full area M2 wafer IBC cell.
- Good understanding on the electrical shading effect on our IBC cells, confirmed by simulations.
- Good characterizations of the n-type finger profile by Raman measurements.
- Indium free TCO investigation and further improvement of the rear reflector using AZO.
- J_{sc} up to 42.47 mA/cm² achieved with the combination of improved AZO/silver rear stack and white rear layer integration.
- Optimization and better comprehension of the method for laser cutting half-IBC cells.

Lowlights:

- Technology upscaling to full half-cell up to only 24.4%, mainly due to edge effects.
- Detrimental impacts of manual handling still limiting the IBC solar cells efficiency.



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Publications related to the project

- K. Eberhard, « Caractérisation de TCOs pour application dans les cellules IBC », Bachelor thesis, Haute Ecole Arc ingénierie, 2020
- B. Paviet-Salomon *et al.*, « The tunnel-IBC technology: a cost-effective approach for back-contacted silicon heterojunction solar cells & modules », Best Poster Award at the 21st PV Tagung, Bern, Switzerland, 2021.