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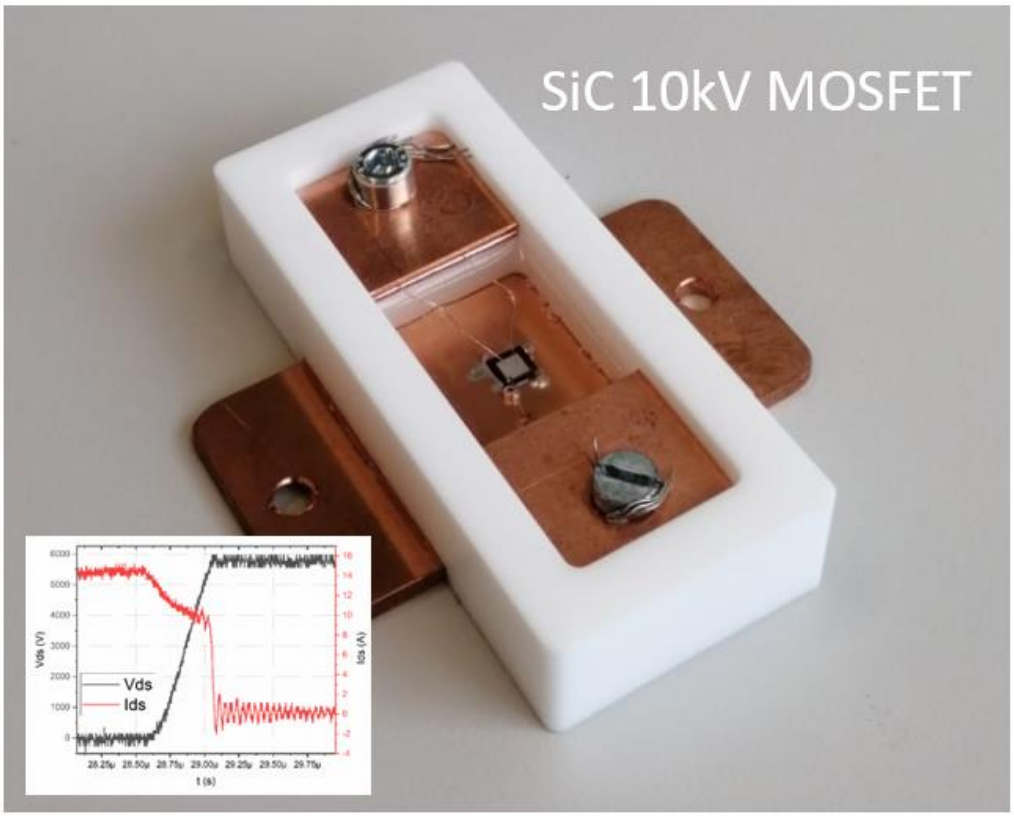
AMPERE

Advanced Materials for Power Electronics Devices



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Summary

In the project AMPERE, HITACHI-ENERGY and the FHNW have developed advanced HV SiC device technologies beyond state-of-the-art. We have focused our efforts to develop technology platforms comprising design simulations, microtechnology processes, process integration schemes and characterization systems for 6.5 and 10 kV SiC switches and diodes. For these HV classes, SiC has strong potential to enable higher efficiency, lower size footprint converters with reduced number of levels, thereby, challenging current state-of-the-art Si IGBT based technologies. The devices fabricated in AMPERE are the first ones made in Switzerland, and as such a great technology step for the Swiss power electronics industry. This included high voltage SiC PiN diodes and MOSFETs, featuring enhanced performance and reliability. The project also supported the development of infrastructure development in Switzerland, that will further allow the development of the technology towards industrial products. The potential is underpinned by the strong collaboration and expertise of the involved partners. The results will now be used for the development of new HV device technologies, but also provide a basis for the development of new power electronics topologies and applications.

Main findings

In AMPERE, we have investigated comprehensively scientific and technological aspects of HV SiC devices. The targets were to deliver device technology platforms and laboratory demonstrators that would allow for an assessment of technology readiness and potential applications.

1) We have demonstrated both bipolar and unipolar switches and diodes, delivering technology platforms comprising design simulations, microfabrication processes and integration routers for the fabrication for 6.5 and 10 kV SiC PiN diodes and MOSFETs. Remarkably, we have shown that the 6.5 and 10 kV SiC PiN diodes and MOSFETs fabricated in Switzerland in the AMPERE project, exhibit safe operation area capability, reliability to temperature and humidity, and significantly lower switching losses than their Si device counterparts.

2) We have also assessed the potential benefits of HV SiC IGBTs, demonstrating the most important aspects of its design rules and also the challenges and possibilities for its fabrication.

3) Furthermore, we have established unique dynamic and reliability characterization systems for HV devices, which will pave the way for future developments of the technology.

The analysis of HV SiC devices will not only give the foundation for HV WBG power semiconductors manufacturing in Switzerland, but also for the analysis and development of new power electronics topologies and applications.

Contents

1 Introduction

1.1 Background information and technology landscape

The increasing need of modern societies for energy efficiency, connectivity and mobility has been the key driving-force for the development of superior power management sustainable solutions. These applications are, for example, consumer electronics, household appliance, industrial traction systems, public transportation, electric vehicles, renewable energy integration, grid systems and so forth. As the energy demand from industrialized countries increases along with a push to replace nuclear power by clean renewable sources, reducing overall energy consumption through efficient power management is a major concern for economic, security and environmental interests.

Power electronics (PE) are the key building block for an efficient power management, and the backbone technology for power electronics is based on semiconductor devices. Power electronics employ solid-state switches and diodes in different topologies to enable functionalities such as conversion of energy. Such solid-state switches, referred as power semiconductors, are responsible for most of innovation and breakthroughs of power electronics, and thus, power semiconductors play major role for enabling energy efficient applications. The technology challenge in such devices is to optimize current density and voltage blocking with minimum energy losses, high reliability and enough safe operation area margins (SOA).

Among the available WBG semiconductors, SiC is the most promising for high-efficiency power conversion applications due to their excellent properties that yield a larger figure of merit than for Silicon. SiC offers significant reduction of on state resistance for similar breakdown voltage. It also enables high-efficiency power devices operating at higher temperature and high frequencies.
There are already commercially available WBG-based switches and diodes that are gaining every year more market share over state-of-the-art Si solutions, by offering lower conduction and switching losses and higher operation frequency.

At HV (>6.5kV), diodes and MOSFETs with silicon carbide (SiC) are expected to show great performance advantages as compared to those made with other semiconductors. This is primarily because SiC has an order of magnitude higher breakdown electric field than conventional materials, and an electron mobility only 20% lower than silicon. A high breakdown electric field allows the design of SiC power diodes with 10 thinner higher doped epi-layers for equivalent voltage blocking. The 4H polytype of SiC is particularly suited for vertical power devices because of its higher vertical mobility.

Its larger bandgap is also expected to result in a much higher operating temperature and higher radiation hardness. The thermal conductivity of n SiC is approximately 3.3 W/C-cm at room temperature, which is 2–3 higher than Si. High voltage (3 kV) Si PiN diodes made using conventional semiconductor materials are restricted to 50 kHz and 120°C, thereby severely limiting the availability of advanced electronic hardware used for utility applications, energy storage, pulsed power, intelligent machinery and solid state power conditioning. HV SiC devices can enable the footprint reduction of power electronic systems, for example, from 3 levels converters using 3.3kV devices to 1 level using 10kV devices, which brings a series of technology and financial advantages for applications.

1.2 Power semiconductors

Most of power electronic topologies are based on a switch (MOSFET, JFET, etc) and an anti-parallel freewheeling diode. Both of these devices comprise an active area for current conduction in on-state and a junction termination area (Figure 1), which is responsible for the device blocking capability in off-state, where the semiconductor is reverse biased. Performance improvement of these devices is based on increasing current density, and reducing switching losses. Those are, in turn, achieved by optimizing the substrate properties (thickness, doping, lifetime, defect density), fabrication processes (quality of interfaces, resistance of metallization contacts, channel carrier mobility, implantation induced defects, etc) and the device design.

Beyond performance, most of high power electronics applications such as grid systems, transportation, industrial drives and many other demand strict reliability requirements. In the case of the power semiconductors components, critical failure mechanisms are activated by the applied high voltage combined to the high temperature operation, which are significantly enhanced in high humidity environmental conditions. Improvement of reliability in those devices is a requirement for its successful implementation, and allows reduced long-term in-service degradation, lowering maintenance needs and costs of grid systems.

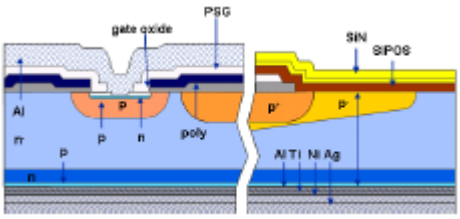


Figure 1. (left) Schematics of an IGBT active area, and (right) junction termination area.

1.3 Purpose of the project

The goal of the AMPERE project is to advance significantly the development of the wide bandgap (WBG) semiconductor silicon carbide (SiC) high voltage power semiconductor devices, such that it can enable the next generation of energy efficient power electronics distribution transformers and medium voltage drives, representing a potential energy saving in Switzerland of ~3.6TWh, roughly 5% of the total energy consumption [1]. To this aim, SiC advanced microfabrication and device designs platforms have been established and integrated for the demonstration of 6.5 and 10kV diodes and switches.

1.4 Objectives

In order to achieve the aforementioned goal, the following specific objectives have been defined:

1. To develop simulation based designs of 6.5 and 10kV SiC MOSFETs and PIN diodes featuring enhanced performance and ruggedness
2. To screen and to assess best technology approaches for fabrication of the 6.5 and 10kV SiC MOSFETs and PIN diodes
3. To develop processing and integration schemes for the fabrication of 6.5 and 10kV SiC MOSFETs and PIN diodes
4. To characterize the novel devices (performance and SOA) and assess its best power electronics application

2 Procedures and methodology

2.1 SiC PiN diode development

In order to gain understanding of HV design rules, particularly of epi layers and terminations, the first part of AMPERE has focused on the development of the HV PiN diode designs. Diodes are excellent platforms to develop these features since they do not add active area complexities and challenges of siwtshes [].

2.1.1 Wafer optimization for HV SiC PiN diodes

In order to reach a desired blocking voltage during reverse bias, the semiconductor epilayer has been optimized in term of thickness and doping concentration. In the current work, for the first target of 6.5 kV devices, parameterized simulations have been done by TCAD 2D simulation. Figure 2a shows the simulated device structure that's included two electrode (anode and cathode), a highly phosphorous doped N-type SiC buffer layer, a lowly phosphorous doped N-type SiC epi layer and a highly aluminium doped P-type SiC anode layer. The code is implemented in a parameterized manner that allows one to easily varying the doping concentration and thickness of each layer. However, in the current investigation where the epilayer information is important, thickness and doping concentration of anode layer and buffer layer are fixed as (1.5 µm; 1×10^{19} cm^{-3}) and (1 µm; 1×10^{18} cm^{-3}), respectively.

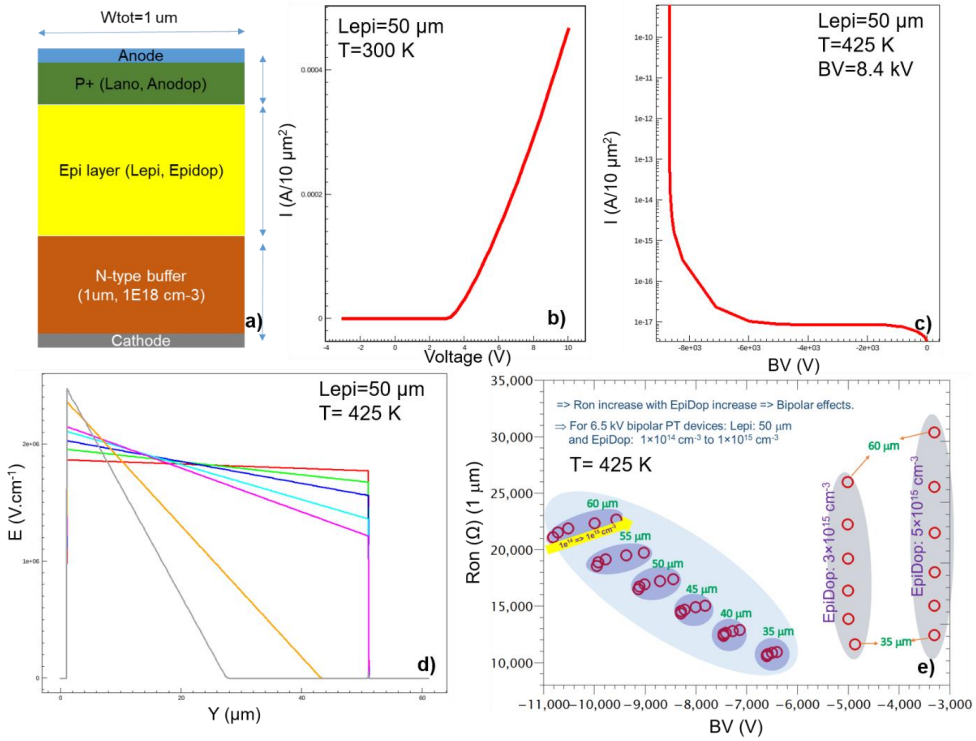


Figure 2: *a) simulation set-up for the epilayer optimization for SiC bipolar devices; b) I(V) characteristic of the SiC PiN diode in the forward bias regime; c) I(V) characteristics of the SiC PiN diode in the reverse bias regime; d) Electric field distribution in a 50 µm thick epilayer at different epilayer doping concentration; e) Breakdown voltage versus the ON-resistance normalized to 1 µm² obtained by parameterized simulation at different epilayer thickness and doping concentration.*

Figure 2b represents the RT forward ON-state characteristics of the SiC PiN diode with an epi layer thickness 50 µm and doping concentration 1×10^{15} cm^{-3}. Due to wide bandgap nature of 4H-SiC (Eg=3.4 eV) the device is open at $V_{ak}\geq3$ V. In this simulation, the incomplete ionization of dopants as well as mobility dependent on doping concentration and temperature have been taking into account. No special carrier lifetime engineering is implemented in this stage.

Figure 1c represents the blocking characteristics of the SiC PiN diode with an epi layer thickness 50 µm and doping concentration 1×10^{15} cm^{-3} at 425 K. With the current epi spec, a parallel blocking voltage of 8.4 kV has been obtained by simulation. For blocking voltage simulation, multiplication factor has been considered as the driven factor [3]. Furthermore, the up-to-date impact ionization coefficients from Niwa et al. [9] have also been implemented.

From blocking voltage simulation, electric field distribution inside the device have been extracted. Figure 2d represents the electric field distribution along the thickness of the device. As one can see from the figure, the electric field depend on epilayer doping concentration. The boundary between punch-through device and non-punch through device can be observed. It can be concluded that, for 6.5 kV device application, a doping concentration in epilayer $N_{epi}\leq 1\times10^{15}$ cm^{-3} is required for the PT devices. As we target also the higher rated blocking devices, e.g. 10 kV devices, epilayer optimization simulations for

this voltage class has also been performed. From TCAD simulation (not shown), an epilayer thickness of 90 µm and doping concentration 8×10^{14} cm^{-3} have been optimized for 10 kV class devices.

Figure 2e summarizes the epilayer optimization simulation for 6.5 kV devices. This epilayer optimization is general and can be used for either PiN diode devices or IGBT devices. However, as this simulation is only considered the parallel planes blocking capability, a certain margin are required to take into account. In reality, as the size of the top electrode is generally much smaller compared to the bottom electrode, electric field can be localized at the edge of the top electrode. Such a localized electric field is well-known to induce the premature breakdown event. In order to limit the localized electric field induced premature breakdown, peripheral protection structures are required to redistribute the electric field at the top side electrode. In the following section, we introduce the peripheral protection structures for 6.5 kV PiN diode and 10 kV PiN diode obtained by TCAD simulation.

2.1.2 Termination design for 6.5 kV SiC PiN diode

Peripheral protection structure of the power semiconductor chips are required for redistributing electric field to prevent the localized electric field induced premature breakdown event. For the aforementioned purpose, in this AMPERE we have investigated a peripheral structure combined of the mesa structure, a junction termination extension (JTE) of 230 µm with five field guard rings (FGRs) separated at different distances, a 30 µm transition layer between JTE and FGRs and a 1.5 µm SiO_2 oxide passivation layer. As similar to the epilayer optimization simulation, the simulated structures were implemented into TCAD simulation in a complete parameterized manner that allows one to easily modify the structure parameters.

Figure 3a represents the electric field distribution inside the optimized peripheral protection structure for the 6.5 kV SiC PiN diode. From the epilayer optimization simulation, an epi thickness of 50 µm and epi doping concentration of 1×10^{15} cm^{-3} has been introduced. For eye guiding purpose, the peripheral structure is also highlighted with the red dashed square in this figure. Highlighted electric field distribution in the peripheral structure with a higher magnification is shown in Figure 3b. Figure 3c represents the electric field along the cutline AA' in Figure 3b. The above three figures demonstrated that peripheral protection structure has successfully redistribute the electric field from the anode region.

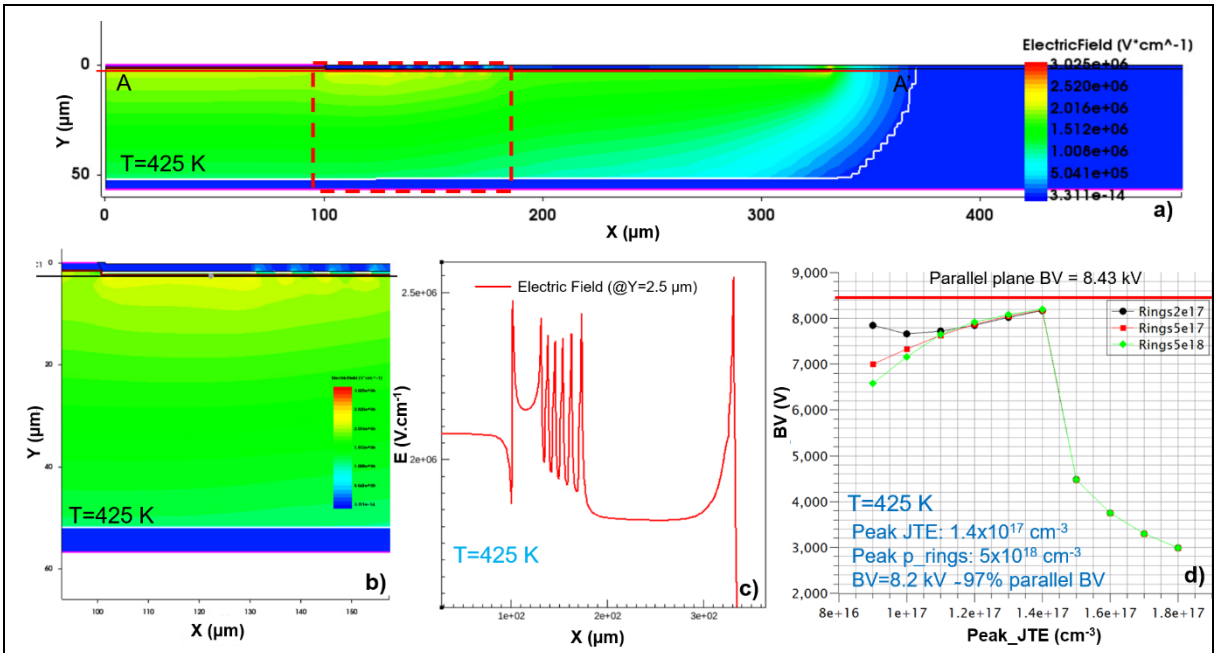


Figure 3: *a) Electric field distribution in the 6.5 kV PiN diode with the peripheral protection structures; b) Electric field distribution in the peripheral protection structure; c) electric field distribution along the cutline AA'; d) Breakdown voltage versus JTE doping values at different fixed FGRs doping values.*

The parameterized simulations are summarized in Figure 3d. At different fixed FGR doping values (2×10^{17} cm^{-3}, 5×10^{17} cm-3, 1×10^{18} cm^{-3} and 5×10^{18} cm^{-3}), the doping value of JTE is changing from 9×10^{16} cm^{-3} to 2×10^{17} cm^{-3} with an interval of 1×10^{16} cm^{-3}. The corresponding breakdown voltages are plotted on Y-axis. From the parameterized simulations, at the optimized JTE and FGR doping value, a breakdown voltage of 97% parallel plan breakdown voltage has been obtained.

2.1.3 Termination design for 10 kV SiC PiN diode

10 kV PiN SiC devices require much more robust terminations, which become even more critical during dynamic switching. The combination of mesa, JTE, FGRs and oxide passivation is also employed in the design of the 10kV device terminations. However, the number of rings as well as the distance between rings were changed in an optimized manner that allows electric field to efficiently redistribute from anode electrode for this voltage class.

Figure 4a represents the electric field distribution in the simulated structure. The peripheral protection structure is highlighted by the dashed red line for the eye guiding purpose. The higher magnification that highlighted the electric field distribution at peripheral structures are shown in Figure 4b. Figure 4c represents the electric field along the cutline BB' in Figure 4c. The above figures indicate that peripheral protection structure has efficiently redistributed the electric field from the anode region and prevented the localized electric field peak.

Figure 4d represents the breakdown voltage versus JTE doping value at different fixed FGRs doping values. With the optimized JTE doping value and FGRs doping value, a breakdown voltage of 94% of the parallel breakdown voltage value is obtained.

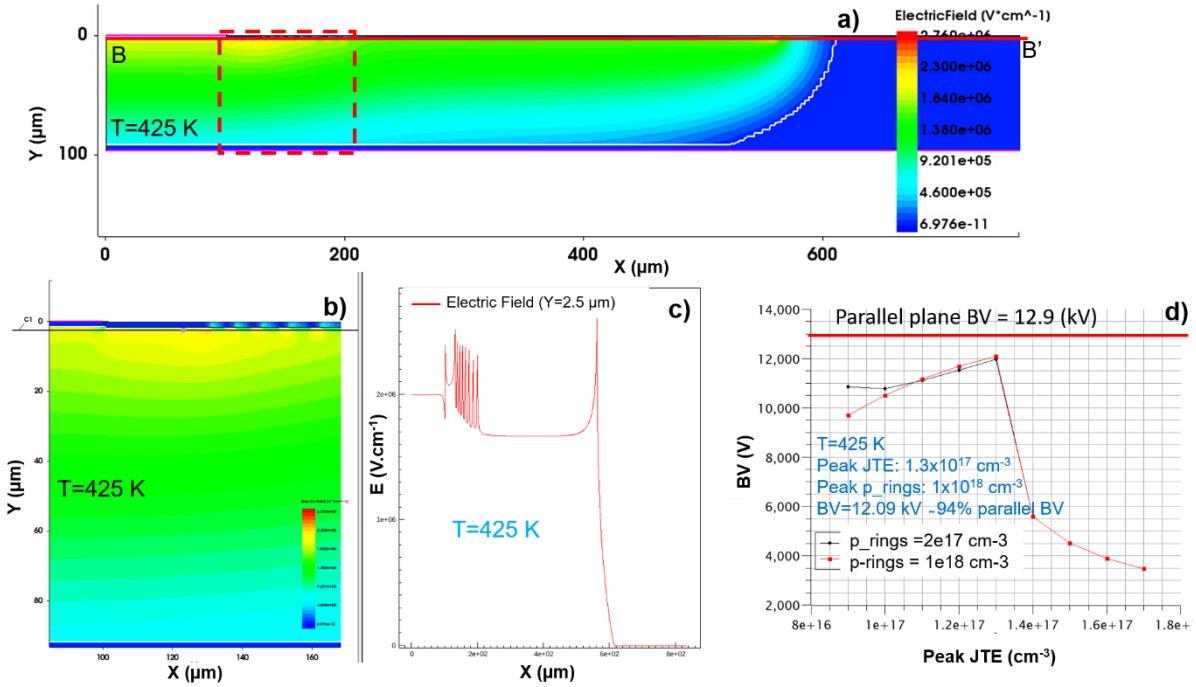


Figure 4: *a) Electric field distribution in the 10 kV PiN diode with the peripheral protection structures; b) Electric field distribution in the peripheral protection structure; c) electric field distribution along the cutline AA'; d) Breakdown voltage versus JTE doping values at different fixed FGRs doping values.*

2.1.4 Process development for HV SiC PiN diodes

After defining the proper design for the SiC PiN diodes, we have proceeded with the fabrication of the devices [2].

Figure 5a presents the cross-section of a PiN diode. The drift and anode layers (1.3 µm, 5×10^{18} cm^{-3}) are epitaxially grown on an n+ SiC substrate. Along with SiC layers, the device also includes top and bottom electrodes, the termination area, passivation and protective layers.

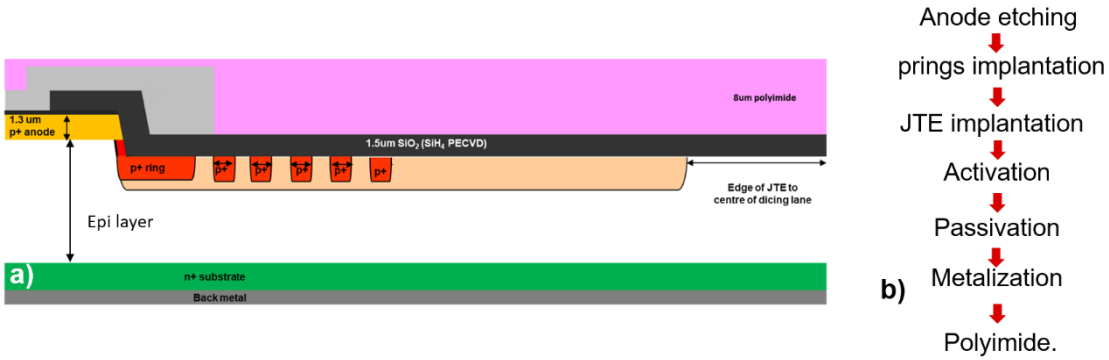


Figure 5: a) Cross-section structure of HV SiC PiN diode, b) Flow of the fabrication process.

Figure 5b shows schematically the process flow used for the fabrication of the HV SiC PiN diodes. The sequence starts by selectively etching the anode layer, followed by p-ring implantation and JTE implantation. The wafers are then activated before the deposition of passivation, metallization and protection layers. Mesa structure are formed by using reactive ion etching. A thick photoresist layer resulted from low RPM spin-coating is used as the mask for mesa etching. Figure 6 shows a SEM image of the etched mesa structure confirmed the anode layer and about 200 nm of epilayer have been etched away. An angle of approximate 30° is also formed, as shown in Figure 3. This angle is important to enhance the implantation efficiency at the transition region between anode and mesa layer.

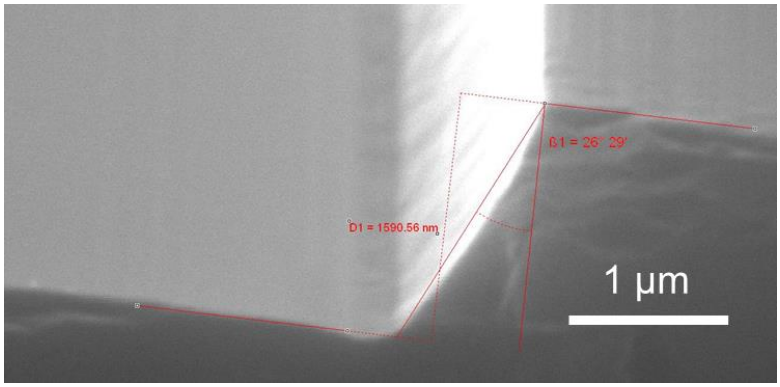


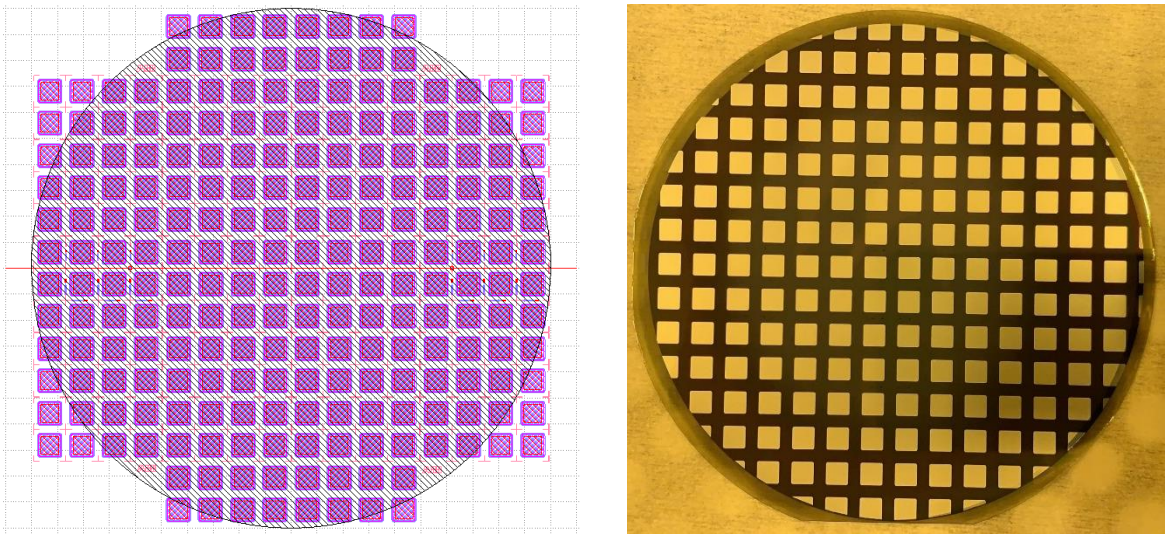
Figure 6: SEM image of etched mesa structure confirmed a 1.5µm deep SiC etching and an angle of 30°.

The termination area is then realized by two level implantations: a highly doped p-rings and a more lowly doped JTE implantations. A 1.3µm thick layer of SiO_2 is used as the hard mask for ion implantation. The dopant activation is done at 1700°C in 30 min in a vacuum chamber. A 1.5µm thick layer of PECVD SiO_2 is used as the passivation layer. The passivation layer in the active area is then etched away prior to ohmic contact formation and thick electrode deposition on the front side and backside of the device. The ohmic contact is formed by annealing at 1000°C during 10 min. Silicon Nitride and polyimide layers will be deposited in last stages as the protective layers to target reliable device operation under high humidity conditions. For the current fabrication approach, two wafers targeting 6.5 kV rated devices and two 10kV wafers were processed in parallel. The details of the PiN diodes lot are summarized in table 1.

	Wafer 1	Wafer 2	Wafer 3	Wafer 4
Wafer code and voltage class	K764-21 – 6.5kV	CN4N07502517 – 6.5kV	CN4N07502508 – 10kV	CN4N07502511 – 10kV
Epi specs	50µm/1.2e15cm^{-3}	6µm/1.2e15cm^{-3}	80µm/9e14cm^{-3}	80µm/9e14cm^{-3}
Epi anode specs	1.3µm/1e19cm^{-3}	1.3µm/1e19cm^{-3}	1.3µm/1e19cm^{-3}	1.3µm/1e19cm^{-3}
Top contact metal	Ti/Al	Ni	Ti/Al	Ni
Pad/chip size	4.2x4.2mm^2	4.2x4.2mm^2	4.2x4.2mm^2	4.2x4.2mm^2
Edge termination	JTE with p+ rings	JTE with p+ rings	JTE with p+ rings	JTE with p+ rings
Top passivation	SiO2 and polyimide	SiO2 and polyimide	SiO2 and polyimide	SiO2 and polyimide

Table 1: Summary of the first fabrication lot and its splits.

Figure 7 shows an image of the mask as well as of a fabricated wafer.



(a) (b)

Figure 7: (a) Image of the mask layout and (b) of a fabricated wafer

2.2 Design and device fabrication of HV SiC MOSFETs

The most critical part of AMPERE was the development of the MOSFET chips. MOSFETs features gate oxide structures that are very sensitive to overall processes, and integration mistakes can result in lower channel carrier mobility. Also, these devices features sub micrometer structures that have to be carefully fabricated in order to provide at the same time robustness and performance [3]. The integration methods have been based on HITACHI-ENERGY proprietary IP.

Both 6.5 and 10kV SiC MOSFETs feature a planar cell design and JTE with p+ rings termination design based on those featured in the 6.5 and 10 KV SiC PiN diodes previously reported in 2019 [2].

In the active area, optimization of the on-state resistance has been performed by adjusting the channel resistance (i.e., reducing the channel length), and the JFET resistance (i.e., reducing the cell pitch). Moving towards short-channel devices improves the performance of SiC MOSFETs, but on the other hand, may cause Short-Channel Effects (SCEs) as well as reduced short-circuit capability.

Short-Channel Effects cause the decrease of the threshold voltage, the deterioration of subthreshold characteristics and the Drain-Induced Barrier Lowering (DIBL) with the associated punch-through behavior. While these effects have been previous investigated silicon-based lateral and vertical devices, the understanding of SCEs in the short-circuit behavior of SiC MOSFETs is lacking. In order to reduce SCEs while improving blocking capability, we have implemented retrograd channed designs. The retrograde channel is achieved by using a lightly doped channel profile near the surface and then gradually increasing the doping concentration with the P-base depth. As such, carrier mobility is improved while the blocking voltage is maintaned because of reduced depletion of the p-well. Additionally, latch-up is suppressed because in retrograde designs the P-base region can be highly doped. Further, optimization of retrograde channel devices has been investigated to understand the influence on the failure mode involving the breakdown of the gate oxide in SiC MOSFETs, which is by far the most common short-circuit failure mode reported in the literature.

The SiC MOSFETs channels were then optimized for channel length, peak doping concentration, and channel depth. The variation of such parameters have an influence on the static characteristics of the device and therefore also on the short-circuit operation.

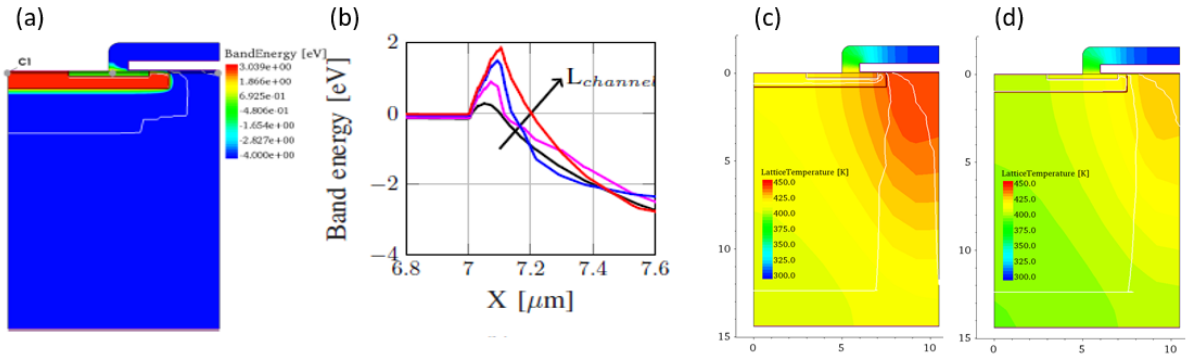


Figure 8. Effect of the channel length (Lch) on a SiC power MOSFET having a uniform channel doping profile: (a) 2D plot of the conduction band potential (b) conduction band potential along the channel, (c) temperature distribution in the SiC MOSFET after a 5 µs short-circuit event the uniform channel SiC MOSFET, and (d) the retrograde channel SiC MOSFET.

Drain Induced Barrier Lowering (DIBL) is one of the most important SCEs, where the drain and the channel-surface potential overlap, reducing the source-to-gate barrier in short channel devices, thereby shifting the threshold voltage. The physical length of the overlap between the drain potential and the surface potential of the channel is typically quantified by the natural length λ, sometimes also referred as screening length. The larger the natural length, the strongest will be its impact on the surface potential of short channels. For single gate planar devices, $\lambda = \sqrt{\frac{\varepsilon_s t_s t_{ox}}{\varepsilon_{ox}}}$, where ε_s/t_s and ε_{ox}/t_{ox} are the permittivity/thickness of the semiconductor and the gate oxide, respectively. Fig. 8a shows the 2D plot of the conduction band potential and the cut location along the horizontal axis. Fig. 8b presents the surface potential for different channel lengths, showing that the barrier lowers for shorter channels. The channel length L_{ch} has been varied between 0.1 µm and 1 µm. Note that the dielectric constant of SiC is just about 20% lower than in Si devices, and the oxide thickness in SiC is also smaller than in Si MOSFETs.

In result, the threshold voltage of the MOSFETs featuring uniformly doped channel, thus loosing blocking capability. The retrograded channel design implemented in our devices suppress the undesirable SCEs.

Further, a lower saturation current is observed for the device having the retrograde channel doping profile, due to the smaller V_{th} shift variation. The smaller short-circuit current results in lower junction temperatures, as presented in Fig. 8(c) and 8(d). Note that for SiC MOSFETs, in order to keep the threshold gate voltage low, a thinner oxide layer is used. This is more sensitive to high drain voltage levels and can result in a gate leakage current, which is further increased by a high-temperature rise during the short circuit event. Furthermore, the SiC MOSFET cell structure is much thinner and narrower compared to Si devices, therefore the short-circuit energy is relatively higher and can easily lead to thermal runaway.

Vertical planar 6.5kV power MOSFETs were fabricated on 4H-SiC (0001) wafers with a lowly nitrogen doped epitaxial layer deposited on a high conductivity n-type substrate. The pitch was optimized to reduce the current limiting effect driven by an increase of JFET effect, which is counter balancing the channel width in conjunction with a high cell density. The process flow for the cell formation is based on a self-alignment process described on the patent US2018/0286963A1, and summarized in Figure 9.

The active area process flow comprises forming the retrograded channel/p-well followed by a self-aligned implantation of the N+ source. The contact to the p-well is then etched and ion implanted. After formation of the carbon cap, which protects the SiC surface during activation, the wafer is annealed at high temperature. After cleaning, the gate oxide layer is formed followed by deposition and formation of the poly-Si gate contact and Ni-based silicidation of all necessary contacts. Finally, the passivation layer is formed followed by metallization and formation of the polyimide layer. Cleaning steps were not added in the present description for confidentiality reasons.

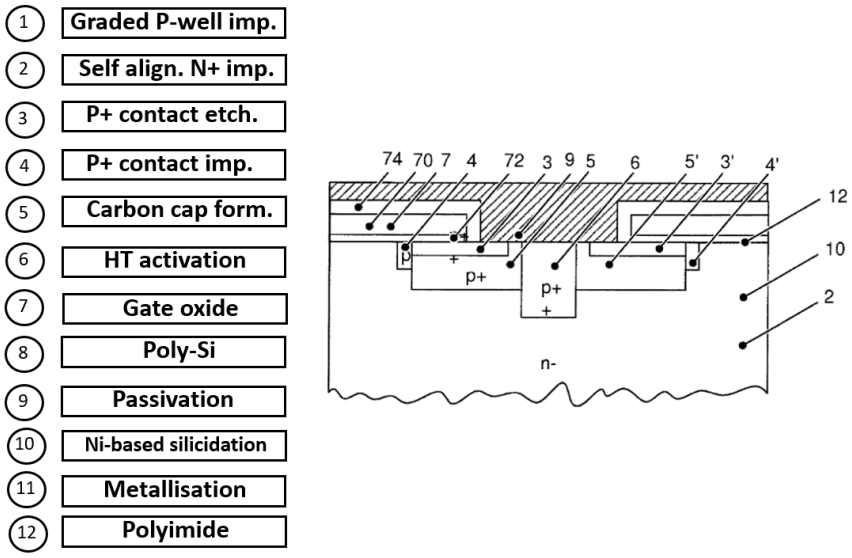


Figure 9. Process flow for the HV SiC MOSFETs (right) and schematics of the cell design (left)].

2.3 HV Semiconductor characterization

Whereas static measurement have been performed in standard semiconductor parameter analyzers, dynamic testing requires customized equipment not commercially available, especially for high voltage devices. These type of equipment is scarcely available worldwide, even because a handful of countries have access to HV SiC devices. Building these facilities in Switzerland represents a key enebler for such technologies. In the following, we describe the development of equipment used for the characterization of switches and diodes developed in AMPERE.

Dynamic tester

In order to characterize the devices hard-switching performance, a double pulse tester (DPT) has been built at the FHNW. Figure 10 shows the DPT system and the designed packaging to perform the soldering and wire-bonding of the DUTs and diodes. Figure 11 shows the DPT working principle, in which two pulses are applied on the DUT (Device under test) gate (Vgs signal as demonstrated in Figure 10). The first pulse sets the switching current according to the pulse duration, inductance value and voltage bias. Then, the DUT is turned off and subsequently turned on, allowing the acquisition of the devices switching curves with an oscilloscope. The designed DPT can perform switching up to 7.0 kV and 60 A, and thus a state-of-the-art test platform to characterize HV semiconductor chips in a wide voltage range. The devices switching performance were characterized under room temperature conditions (25°C), gate voltage swing of -10V up to +15V and gate resistance of 50 Ω. The DPT loop stray inductance, including the parasitic inductance from all components and busbar, is around 200 nH.

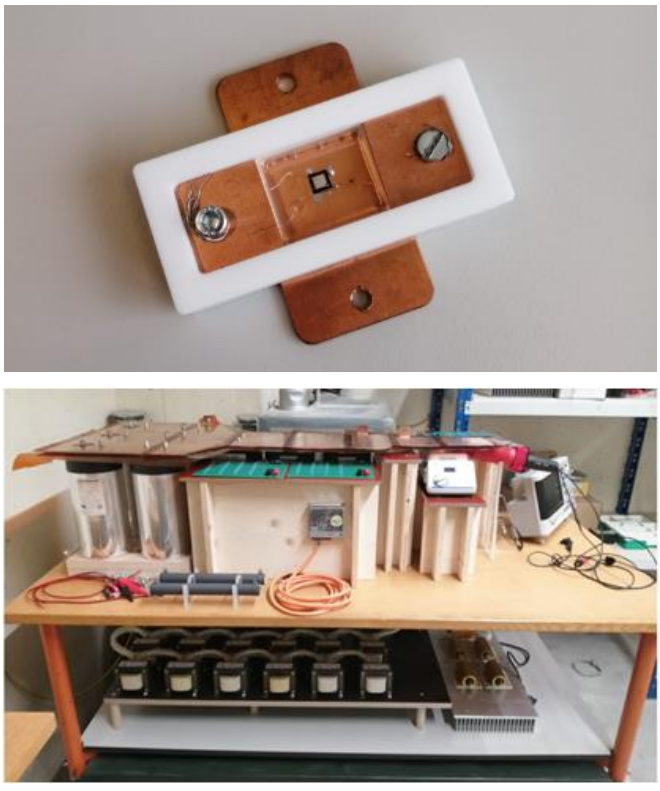


Figure 10: Test packaging with a 10kV bonded PiN diode (top) and DPT system used in the characterization of switching losses.

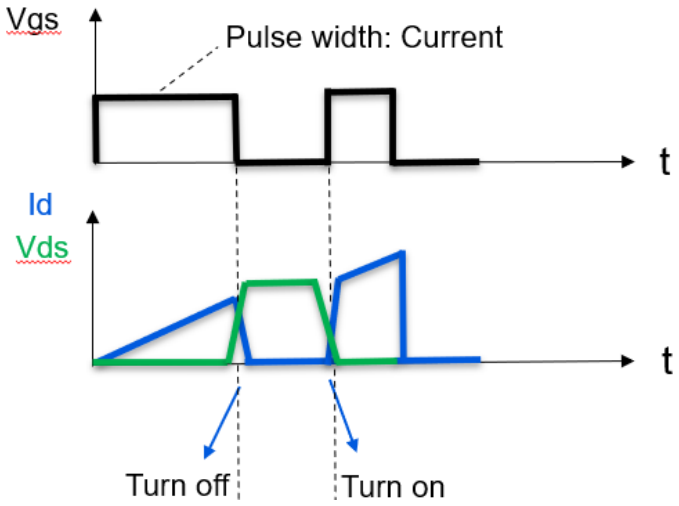


Figure 11: Vgs signal generation and DUT switching curves.

H3TRB characterization

The High Humidity, High Temperature and High Voltage Reverse Bias test (H3TRB) is a state-of-the-art experiment to assess the long-term ruggedness of semiconductors under harsh environmental conditions. This test is performed with the DUT submitted to a reverse bias of 80% from the device rated voltage, an ambient temperature of 85 C, relative humidity of 85% and test duration of 1000 h. Figure 5 shows the H3TRB system built at FHNW. This system comprises 16 channels that allow the test of 16 DUT simultaneously. Furthermore, it can handle up to 8 kV of DC link voltage for the investigation of up to 10 kV rated devices.

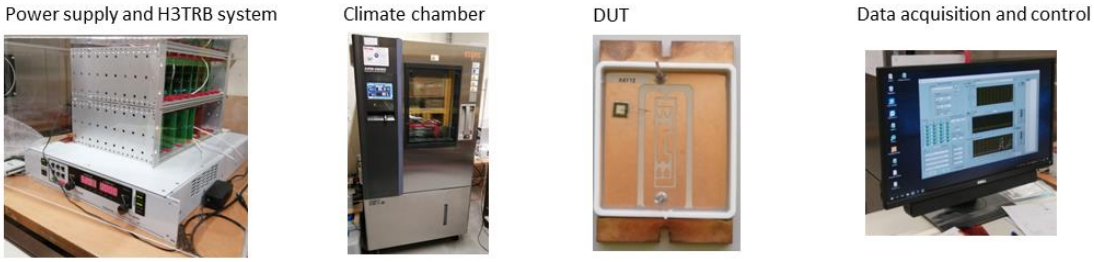


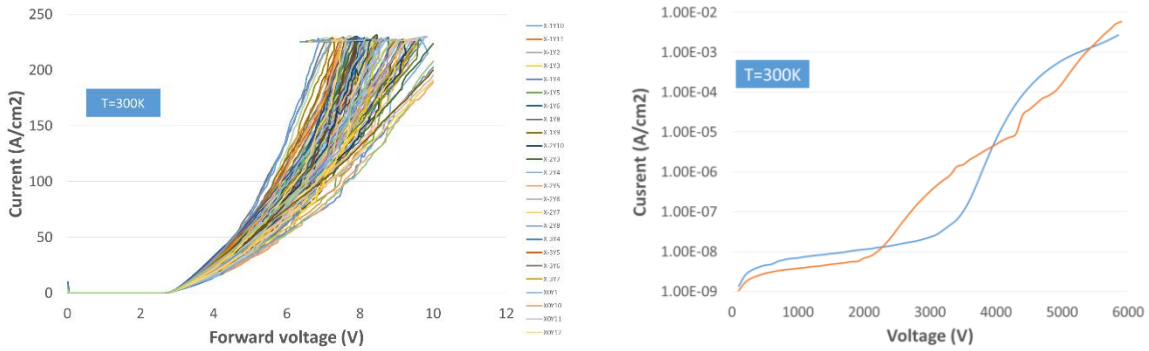
Figure 12: from left to right: H3TRB power electronics system, the climate chamber, the bonded 6.5kV SiC PiN diode DUT, and the control software.

Prior to testing, the chips are soldered to a DBC substrate and covered with silicone gel, as shown in Figure 12. The DUT is then placed inside the climate chamber and further connected to the H3TRB system through high voltage cables. The system has internal switches controlled individually by external software that interrupts the current flow in case of the DUT sudden failure, thereby allowing the test to be continued without the failed device removal. Furthermore, the control software is responsible for leakage current continuous acquisition. In case of DUT failure, the system has internal protection to avoid the loss of the data acquisition device.

3 Results and discussion

3.1 HV SiC PiN diodes static characterization

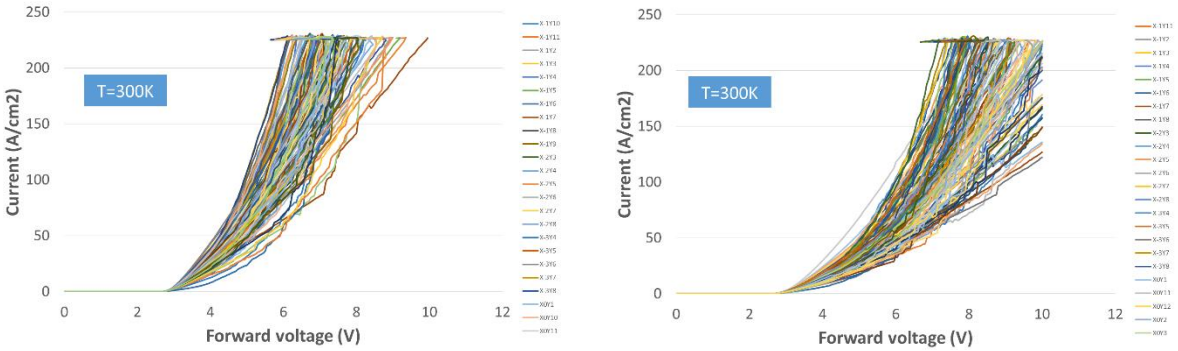
The electrical characteristics of 6.5kV-rated PiN diodes on wafer 1 are shown in Figure 13 (wafer level measurements) [2]. Figure 13 (a) shows the on-state characteristics, while blocking is depicted in figure 13(b). A large current spread in the IV is observed in output characteristic. This can be explained by the absence of a full metal stack at the back of the wafer. Once the wafers will be fully finished, the spread in the current is expected to decrease. Preliminary blocking measurement also show that the diodes are able to block at least 6kV, therefore showing that the JTE-based edge termination is working reasonably well.



(a) (b)

Figure 13 Forward output and blocking characteristics of PiN diodes on wafer 1

The forward output characteristics of the 10kV wafers (wafer 3 and wafer 4) are shown in figure 14, measured at 300K. Here, the initial results show that a Ti/Al ohmic contact would work better than a Ni one, but more analysis is needed to confirm this conclusion.



(a) (b)

Figure 14 Forward output characteristics of (a) wafer 3 and (b) wafer 4, at T=300K

The blocking IV of a 10kV PiN diode from wafer 4 is shown in figure 15. The maximum voltage measured was 9100V, which is the highest blocking voltage measured on a SiC device at ABB CH-CRC.

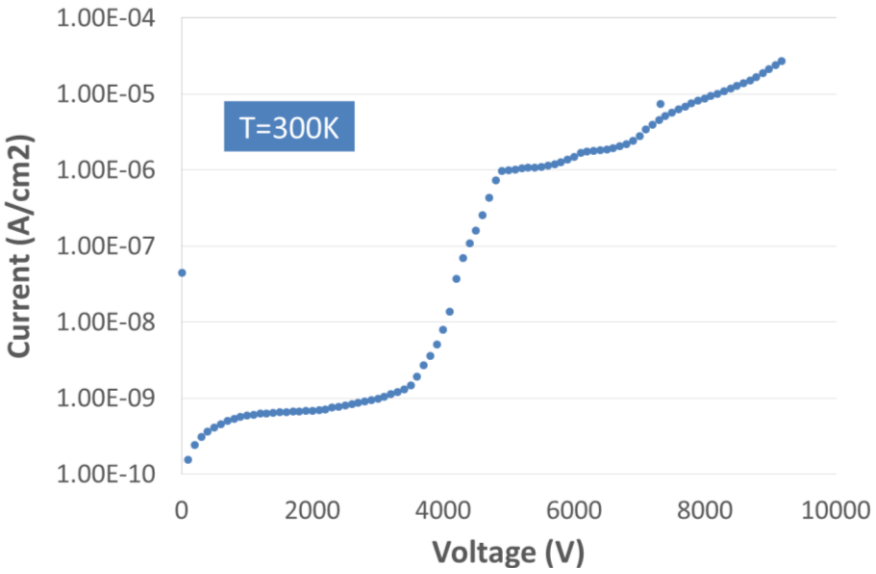


Figure15 Blocking IV of a 10kV-rated PiN diode on wafer 4

3.2 Design of HV SiC IGBTs

As part of the investigation of HV SiC devices, we have developed designs and potential fabrication approached for HV SiC IGBTs [2]. Although the availability of wafers for the fabrication of such devices and not readily available at the moment, we have here addressed all major challenges in terms of predicting performance, and defining design rules and integration approaches. We expect these results will be very valuable when the market of HV SiC develops volume.

One of the most challenging issues with SiC IGBT is the lack of p+ substrates. Therefore, the most viable approach is to fabricate a p-channel SiC IGBT on the well-established n+ substrate. However, p-channel IGBTs are inferior compared to n-channel IGBTs. In this section, we discuss different possible fabrication scenarios of an n-channel SiC IGBT. In order to fabricate an n-channel IGBT, a p+ collector layer is needed. The main difference between fabrication scenarios is coming from the approach to form the p+ collector layer. The p+ collector layers can be formed by either epitaxial growth or ion-implantation. Figure 16 represents the epitaxial approaches to form collector layer, in a more standard process and in a flipped-wafer process. Standard process is employed by Wolfspeed and is represented in Figure 6a. In the standard process, the p+ collector layer is epitaxially grown on the n+ substrate, followed by growing n-buffer layer, n-drift layer and the current spreading layer. The substrate is subsequently removed by a grinding process prior to the top MOS-cell fabrication process. Using the approach, the MOS-cells are processed on Si-face of SiC (in a very similar fashion to SiC MOSFETs). The flipped-wafer process is shown in Figure 6b. In this process, first the n-current spreading layer is grown, followed by the n-drift region and the buffer layer. The epitaxial p+ collector layer is the last grown layer, as the top-most layer. The n+ substrate is then removed by a grinding process. The wafer is then flipped over prior to the MOS-cell processing. Employing this approach, the MOS-cells will be process on the C-face of SiC and should result in higher channel mobility values as compared to the Si-face. This process has been employed by Purdue University and AIST.

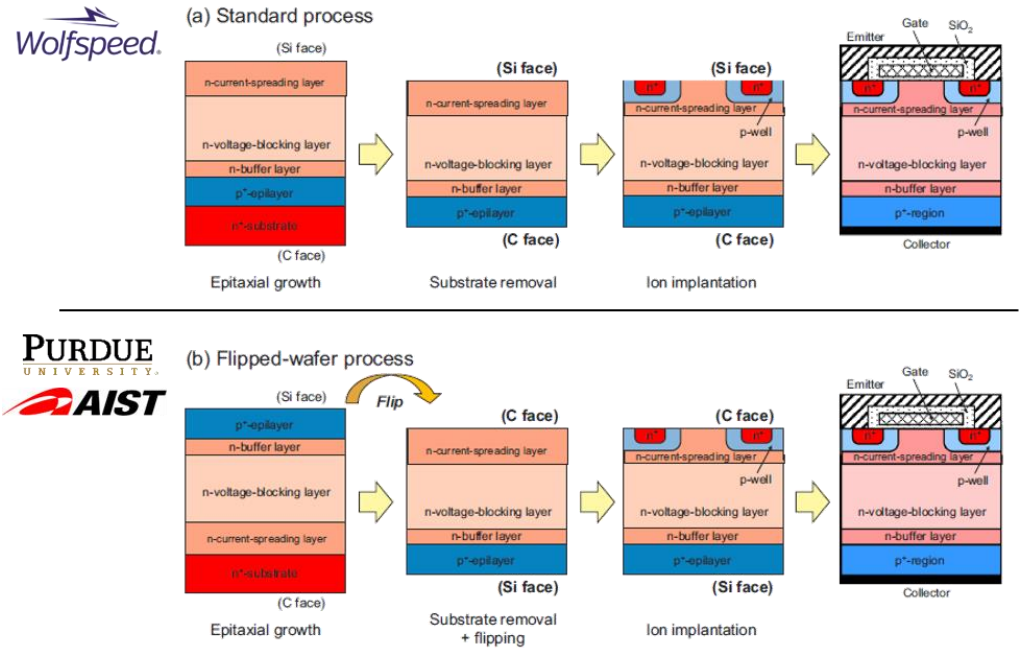


Figure 16: SiC IGBT fabrication approaches (a) the more standard approach and (b) the “flip wafer“ approach.

Figure 17 shows the implanted approaches to realize the collector layers of an n-channel SiC IGBT. Figure 17a represents the more standard approach. Here, the n-buffer, n-drift and n-current spreading layers are grown epitaxially on top of the n+ substrate. This is followed by processing the top side MOS-cell. The n+ substrate is then grinded away and the p+ collector region is formed by ion implantation and laser activation. This approach is employed by UnitedSiC.

The flipped-wafer approach is depicted in figure 17(b). In this approach, similar to flipped-wafer process of epitaxial collector, the n-current spreading, n-drift and n-buffer layer are grown on n+ substrate. The process is then followed by removing n+ substrate and flipping the wafer over. The p+ collector layer is formed by ion-implantation. This approach has been demonstrated by Rensselaer Institute.

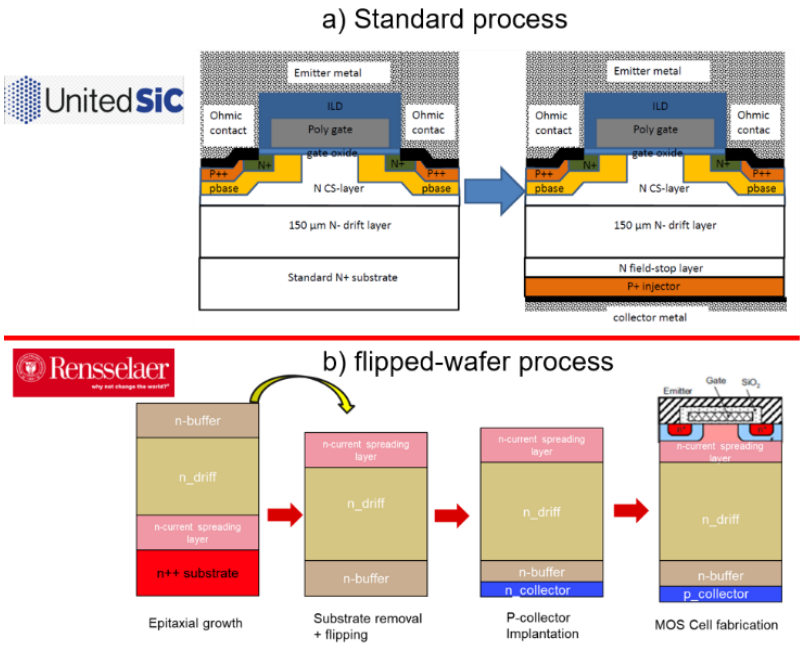


Figure 17: Implanted approaches to realized the collector layers of n-channel SiC IGBT.

3.3 IGBT Investigation results

N-channel 4H-SiC IGBTs are amongst the highest voltage-rated power devices reported. However, due to the lack of high quality p+ SiC substrates, the fabrication of n-type SiC IGBTs is challenging. Epi-type collector and implanted collector approaches have been proposed for the fabrication of n-type SiC IGBTs. A detailed investigation considering different fabrication approaches as well as structural and physical parameters is required for an improved understanding of the cost/performance challenges that UHV SiC IGBTs are facing.

For the TCAD simulation, a $2\times10^{14}cm^{-3}$–doped epi layer with a thickness of 200µm has been used, targeting blocking voltage values around 20kV. A SiC MOSFET-like top cell design has been employed with a pitch of 15µm. For the MOS channel, we considered l_{ch}=0.5µm with the MOS interface being formed on the Si face. Figure 18a represents the schematic structure of the investigated device. Inversion layer mobility values of $38cm^2/Vs$ have been used. Niwa's impact ionization coefficients and incomplete ionization effects are employed. The JFET region and holes barrier layer are not considered at this stage. All simulations have been performed at 425K. Figure 18b summarizes the main parameters used in the simulations. In order to compare different designs for ON-state characteristics, V_{CE} at different fixed current level (e.g $20A/cm^2$ and $50A/cm^2$) are plotted on the same curve.

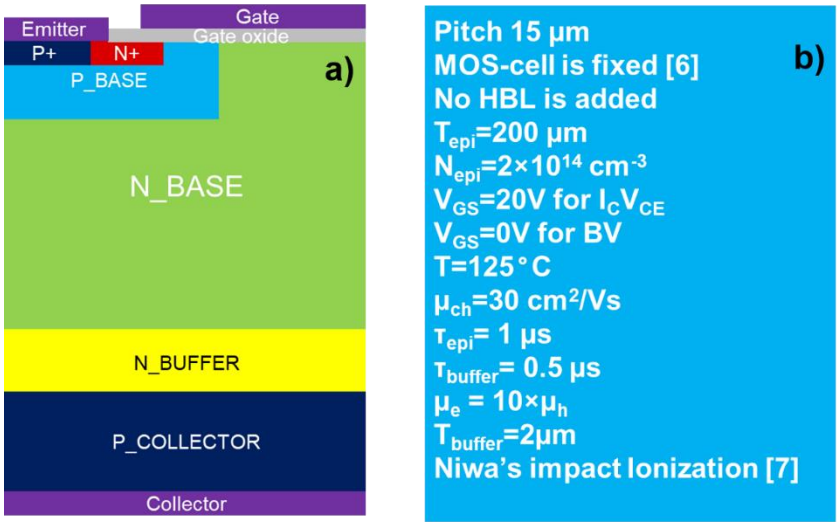


Figure 18: a) Schematic cross-section of the investigated device; b) list of the main parameters used in the simulations.

3.3.1 Collector Design Considerations

In order to investigate the effects of collector layer based on different fabrication approaches, implanted collector and epitaxial collector with different thickness and doping concentration were simulated. Figure 19a shows that an implanted collector ($t_{collector}$=0.8 µm) is far inferior (regarding on-state losses) compared to the epi-collector ($t_{collector}$=20µm). The optimum collector thickness (for $N_{collector}$=2×10^{19}cm^{-3}) is found to be around 20µm, as shown in Figure 19b. By increasing the collector thickness beyond 20µm, no further improvement is observed. From a cost perspective, this is an important result as the epitaxial growth of thicker p+ layers (≥20µm) would only be needed for wafer handling purposes during the fabrication flow.

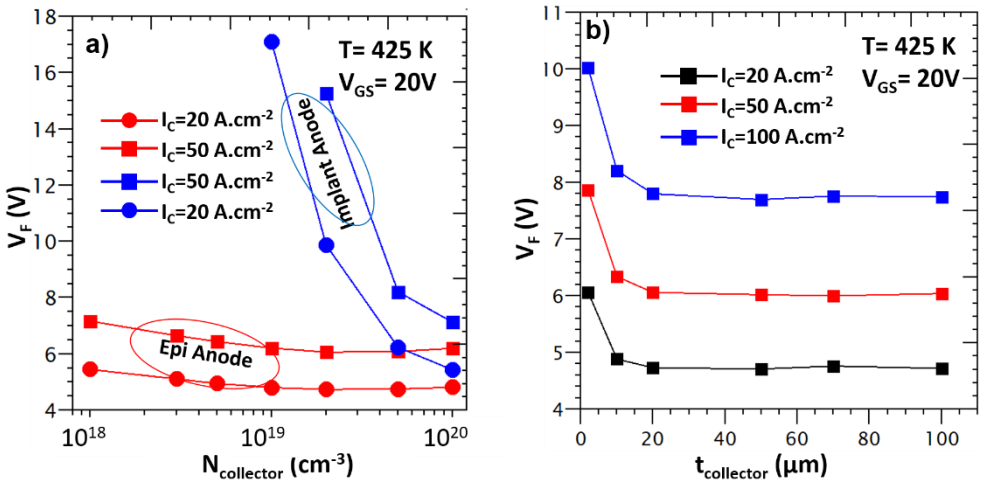


Figure 19: a) Static loss (V_F) at different collector doping concentrations for both epi collector and implanted collector designs, considered at three current levels (I_C=20Acm^{-2} and 50 Acm^{-2}); b) Static loss (V_F) at different collector thickness values, considered at three current levels (I_C=20Acm^{-2}, 50 Acm^{-2} and 100Acm^{-2}).

3.3.2 Buffer Design Considerations

The optimization of the buffer layer is shown in Figure 20a and Figure 20b (for $t_{collector}$=20µm, $N_{collector}$=2×10^{19}cm^{-3}), at two current density levels (I_C=20Acm^{-2} and I_C=50Acm^{-2}). A normalized BV/BV$_{max}$ ratio is used to highlight the variation of breakdown voltage. While the buffer doping does not affect significantly the static losses, it has however a strong impact on the IGBT blocking capability (Fig. 10a). On the other hand, a 5 times increase in the buffer thickness leads to about 0.5-0.9V increase in V_F with negligible impact on device blocking (Fig. 20b).

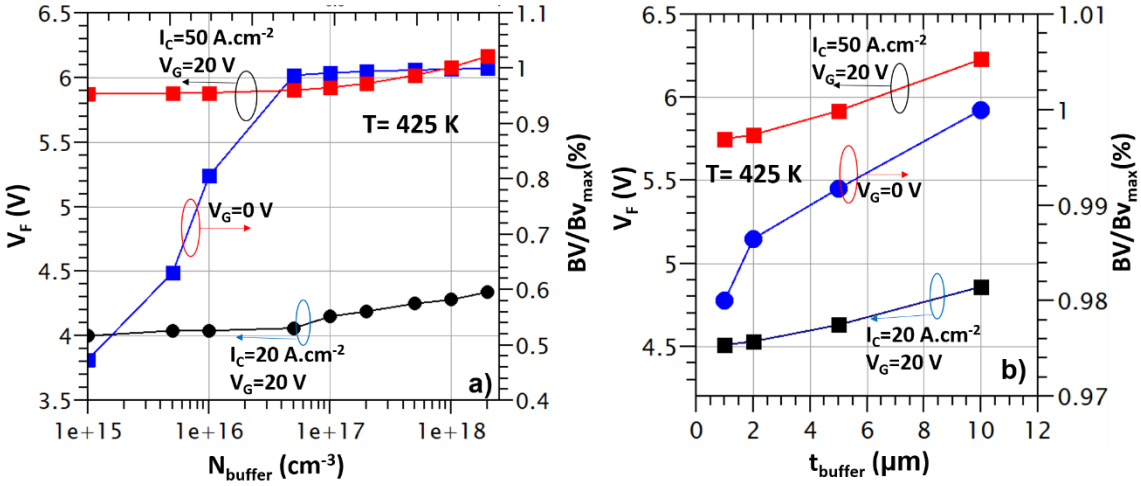


Figure 20: a) Statics loss V_F and BV/BV$_{max}$ variation for different buffer doping concentration values; b) V_F and BV/BV$_{max}$ variation for different buffer thickness values.

3.3.3 Minority Carriers Lifetime Considerations

For a 2µm layer, increasing the minority carrier lifetime in the buffer region up to 0.8µs has little impact on the output characteristics (Fig. 21a). The variation of minority carriers lifetime in the epi region has a much stronger effect on the static losses (Fig. 21b) compared to its counterpart in the buffer region.

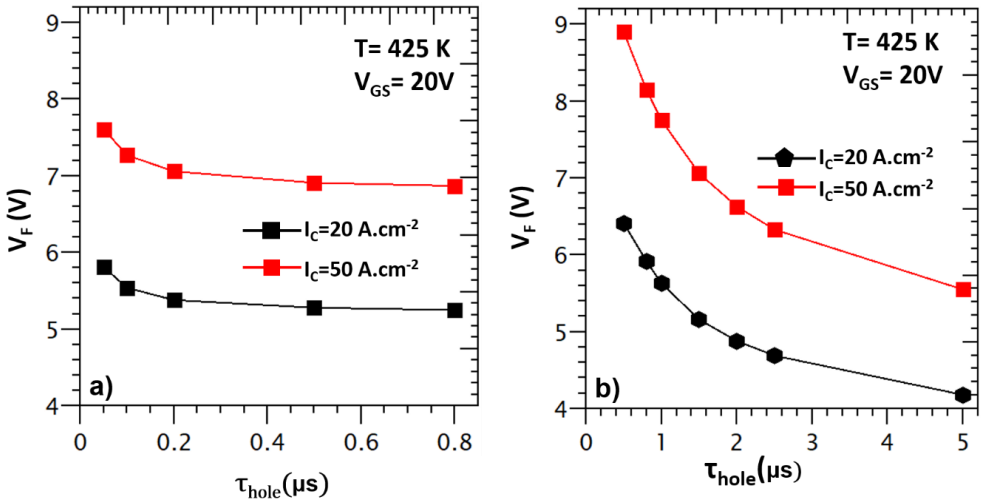


Figure 21: a) Static loss V_F for different buffer carrier lifetime values (for τ_{epi}=1µs); b) V_F at different drift layer carrier lifetime values (for τ_{buf}=0.5µs).

3.3.4 Switching Characteristics

The IGBT turn-off waveforms, for different buffer thickness are depicted in Figure 22a. The load current was 20Acm^{-2} and V_{DClink}=7.5kV (a load inductor of 0.1µH and a gate resistor of 33Ω were used in the mixed-mode simulations). The gate swing was from +20V down to -15V. A 2µm thin buffer device experiences a significantly slower turn-off process as compared to the thicker buffer designs (tbuffer≥5µm). Figure 22b represents the effect of minority carriers lifetime in buffer region on the turn-off losses (for T_{buffer}=2µm and T_{buffer}=10 µm). It is shown that the buffer thickness has sizeable impact on the switching characteristics of the device.

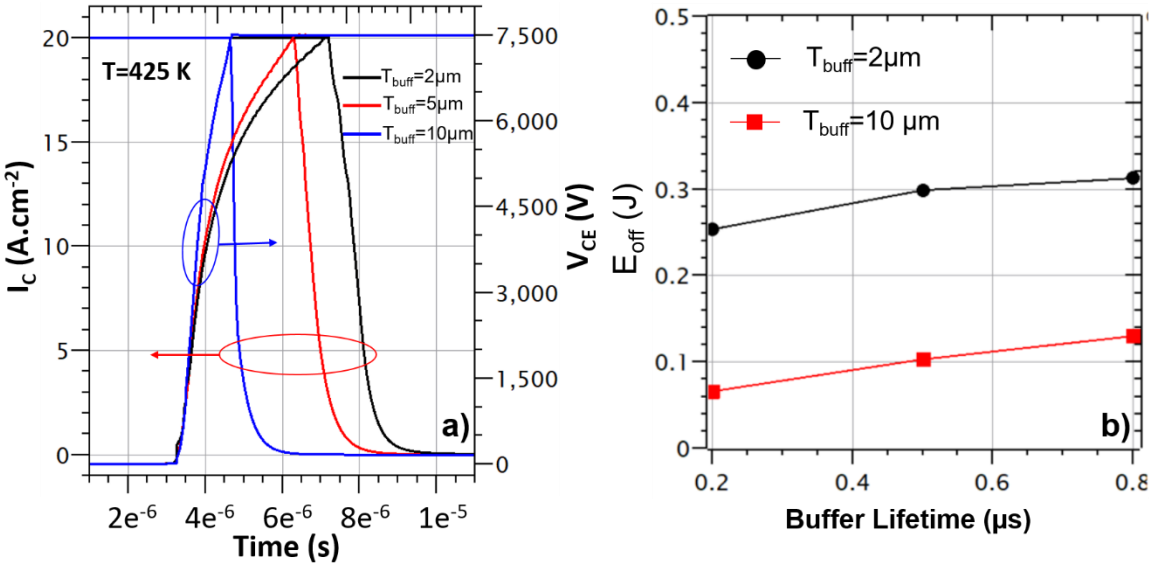


Figure 22: a) Turn-off waveforms in the inductive clamped switching for different buffer thickness values. V_{GS}=-15V to 20V; b) The SiC IGBT turn-off losses extracted for different buffer lifetime values (for τ_{buffer}=2µm and τ_{epi}=1µs).

In summary, the static and turn-off performance of SiC UHV IGBTs has been extensively investigated. In view of both static and dynamic behavior, some design rules for collector and buffer regions become apparent towards an improved cost/performance trade-off for UHV SiC IGBTs.

3.4 HV SiC MOSFET static characterization

Figure 23a shows the static ID-VD characteristics of 6.5kV fabricated MOSFETs at a junction temperature (Tj) of 25°C and a gate voltage of VG=15V [3]. The 6.5kV SiC MOSFETs provide at INOM up to 1V reduction of on-state voltage compared with 6.5kV rated commercial IGBTs. At similar power density of ~130W/cm^2, the nominal current for the MOSFET is 45A/cm^2, thus improving current density by 20% at lower losses.

In Figure 23b, the body diode conduction in the third quadrant is demonstrated for VG=-5V. The body diode of the 6.5kV MOSFET has a turn on threshold of around -2.5V for negative VG. At the rated diode current of 75Acm^{-2} a comparable voltage drop to commercial Si PiN diodes can be observed. For a fair comparison to 6.5kV Si PiN diodes, we have to point out that by using the bidirectional functionality of the MOSFETs more diode area (~3x) is available in the module than it would be the case with separate diodes. Figure 23c displays the reverse bias IV characteristics of the 6.5kV SiC MOSFET with VG=0V. The blocking voltage is increased by applying a VG of -5V in normal reverse bias operation.

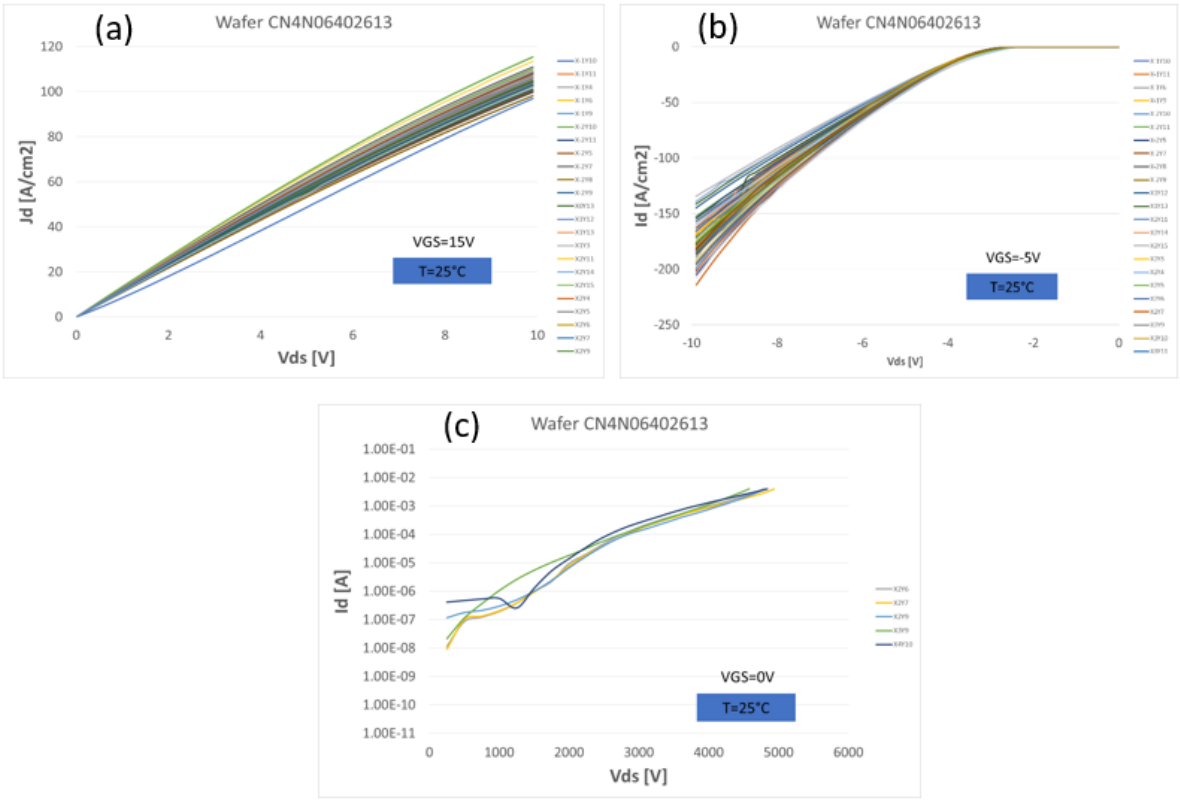


Figure 23. IV characteristics of the 6.5kV SiC MOSFET at T=25°C showing the (a) output characteristics at VG=15V, (b) body diode forward characteristics at VG=-5V and (c) the reverse bias characteristics at VG=0V.

The static IV characteristics of the 10kV SiC MOSFET is shown in Figure 24. Figure 24a shows the output characteristics of 10kV fabricated MOSFETs at an ambient temperature (Ta) of 25°C and a gate voltage of VG=15V. For this voltage range, there are no similarly rated Si IGBTs to attempt a comparison. At a power density of ~130W/cm^2, the nominal current for the MOSFET is about ~30 A/cm^2.

Figure 24b displays the 10kV MOSFET body diode conduction at VG=-5V in the third quadrant showing a turn-on threshold of -2.5V for VG=-5V. At the rated diode current of 75Acm^{-2} a comparable voltage drop can be observed for all diodes. For a fair comparison to 6.5kV Si PiN diodes. Figure 6c displays the reverse bias IV characteristics of the 10kV SiC MOSFET with VG=0V. Because of technical issues, we have characterized the devices only until 3kV. The full reverse bias characterization including the dynamics characteristics will be performed in the last phase of the project.

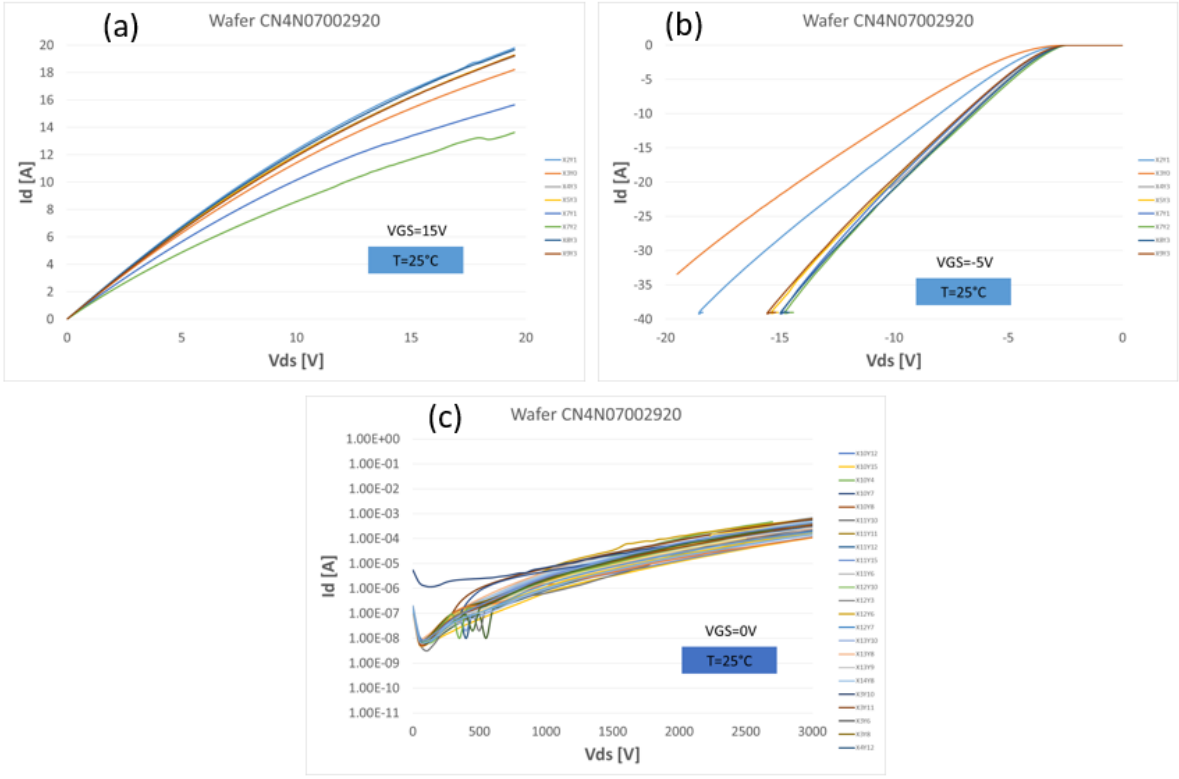


Figure 24. IV characteristics of the 10kV SiC MOSFET at T=25°C showing the (a) output characteristics at VG=15V, (b) body diode forward characteristics at VG=-5V and (c) the reverse bias characteristics at VG=0V.

The transfer characteristics for this 10kV SiC MOSFET wafer are shown in figure 25, at 25C. The devices have a positive threshold voltage of around 2.3V. It is expected that this value will decrease by about 1V at 125C.

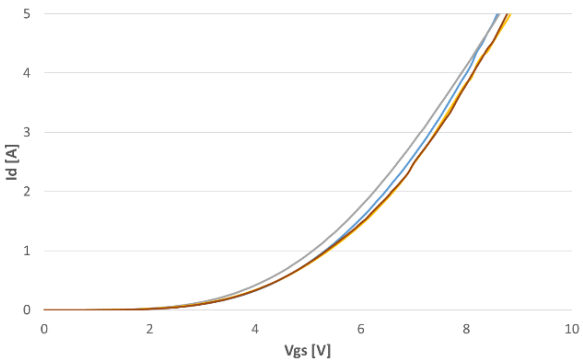


Figure 25. The transfer characteristics of the 10kV SiC MOSFET at T=25°C.

Recent blocking measurements reveal that the 10kV MOSFETs, after being initially characterized only up to 3kV, are able to support at least 6kV at V_{GS}=0V (fig. 26). As can be noticed the leakage current levels between the 3kV and higher voltage measurements are very similar. The high voltage

measurements were stopped as the current clamp of 4 mA was reached. While it is obvious that the edge termination will probably need further optimization, these results are nevertheless encouraging as they demonstrate the transfer of the edge termination design from the PiN diodes lot to the MOSFET lot was reasonably successful.

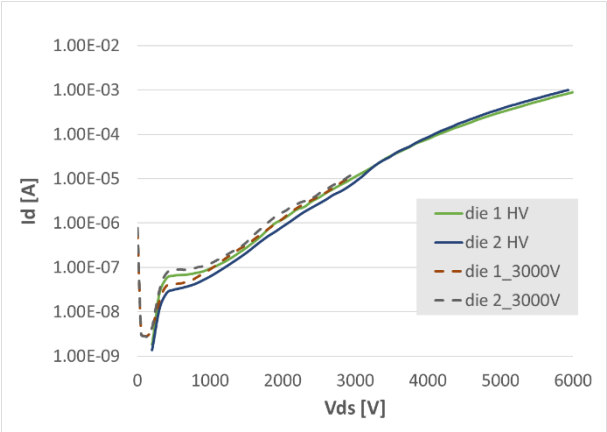


Figure 26. Blocking IV characteristics of 10kV SiC MOSFETs; two dies are shown for measurements performed up to 3kV and 6kV, respectively.

3.5 Comparison between 6.5 kV Si IGBT/6.5 kV SiC PiN Diode, 6.5 kV Si IGBT/6.5 kV SiC JBS Diode & 6.5 kV Si IGBT/6.5 kV Si PIN Diode – Static and Dynamic performance

SiC components with 6.5 kV voltage rating and above are of primary interest for power electronics applications such as distribution transformers and medium-voltage drives. SiC diodes in particular are an essential component to SiC switches in such applications, especially when reverse-blocking components (IGBTs) are involved. In addition, MOSFETs also benefit from the implementation of antiparallel diodes. Especially in medium voltage range, bipolar diode devices (p-i-n) offer better performance compared to unipolar devices (JBS) due to conductivity modulation when high current operation is encountered. In this section, we compare the static and dynamic performance of the 6.5 kV SiC PiN diode with that of SiC JBS and a silicon diode in terms of an application with a 6.5kV Si IGBT. 6.5 kV SiC PiN diodes were fabricated using 4H-SiC wafers consisting of 50 µm epilayer and a 1.3 µm thick anode with a doping concentration of 1e19 cm^{-3}. Ti/Al metal layers were used as Ohmic contact to the anode. The periphery of the diodes was protected using a Junction Termination Extension (JTE) and 5 embedded p+ guard rings. The MESA angle was optimized such that the walls are also implanted with p+. The normalized forward characteristics at 25°C of a 6.5 kV PiN diode is shown in Figure 27A along with the forward characteristics of 6.5 kV SiC JBS and silicon diode. It could be seen that at a current density of 100 A/cm^2 the SiC PiN diode has a forward voltage of ~ 3.8 V, whereas SiC JBS and silicon diode reach a current density of 100 A/cm^2 at a forward voltage of ~ 6.5 V and ~4.3 V, respectively. Hence, SiC PiN diode offers a clear advantage when operating at higher current densities (above 100 A/cm^2). For current densities less than 40 A/cm^2, SiC JBS and silicon diode depict a lower forward voltage drop, due to the higher knee voltage of SiC PiN diode. The reverse blocking characteristics of these diodes at room temperature are shown in Figure 27B. It can be seen in the graph that SiC PiN diode has the lowest leakage current up to 6 kV. The silicon diode reveals a lower reverse leakage than SiC JBS diode throughout the whole range studied. The dynamic performance of these diodes has been analysed by switching them with 6.5 kV silicon IGBT at room temperature. Figure 27C shows the IGBT turn-on wave form using the SiC JBS, SiC PiN and the Si diode. The IGBT has been switched at a dc link voltage of 4.4 kV and a current of 20 A. As expected, the IGBT turn on current overshoot differs when switched with different diodes. IGBT current overshoot is ~90 A when switched together with silicon diode. Current overshoot is ~28 A and ~37 A when switched with SiC JBS and PiN diode, respectively. The turn-off characteristics of silicon diode, SiC PiN and SiC JBS diodes when switched together with 6.5 kV silicon IGBT at a dc link voltage of 4.4 kV and current of 20 A is shown in Figure 27D. It could be seen that current overshoot during diode turn off was very high (~65 A) for silicon diode due to reverse recovery. The current overshoot for both SiC JBS (~10 A) and PiN diode (~15 A) was low compared to the silicon diode. The overshoot was very low for SiC JBS due to the absence of minority carriers. There was not significant difference in the turn off characteristics of IGBT when switched with a silicon diode, SiC PiN or JBS diodes (not shown).

The power losses of silicon IGBT during turn on, when switched with different diodes is shown in Figure 27E. It can be seen that the power losses of the IGBT are very high when switched with silicon diode and it was more than twice than the losses of IGBT switched with SiC diodes. Again, the power losses of the IGBT switched with SiC JBS diode was the lowest. The calculated power losses of IGBT during turn on and turn off with different diodes is shown in figure 28. It could be seen that the IGBT turn on losses when switched with silicon diode (~85 mJ) was more than twice when switched with SiC diodes (~41 mJ). There was not much difference in the turn-off losses of IGBT when switched with different diodes. The loss from SiC diodes (~<2 mJ) was very low compared to silicon diode (~10 mJ). Considering the higher operating current density, low leakage and better dynamic characteristics, SiC PiN offers the superior solution among the diodes studied. *Last, but not least, all devices reached SOA.*

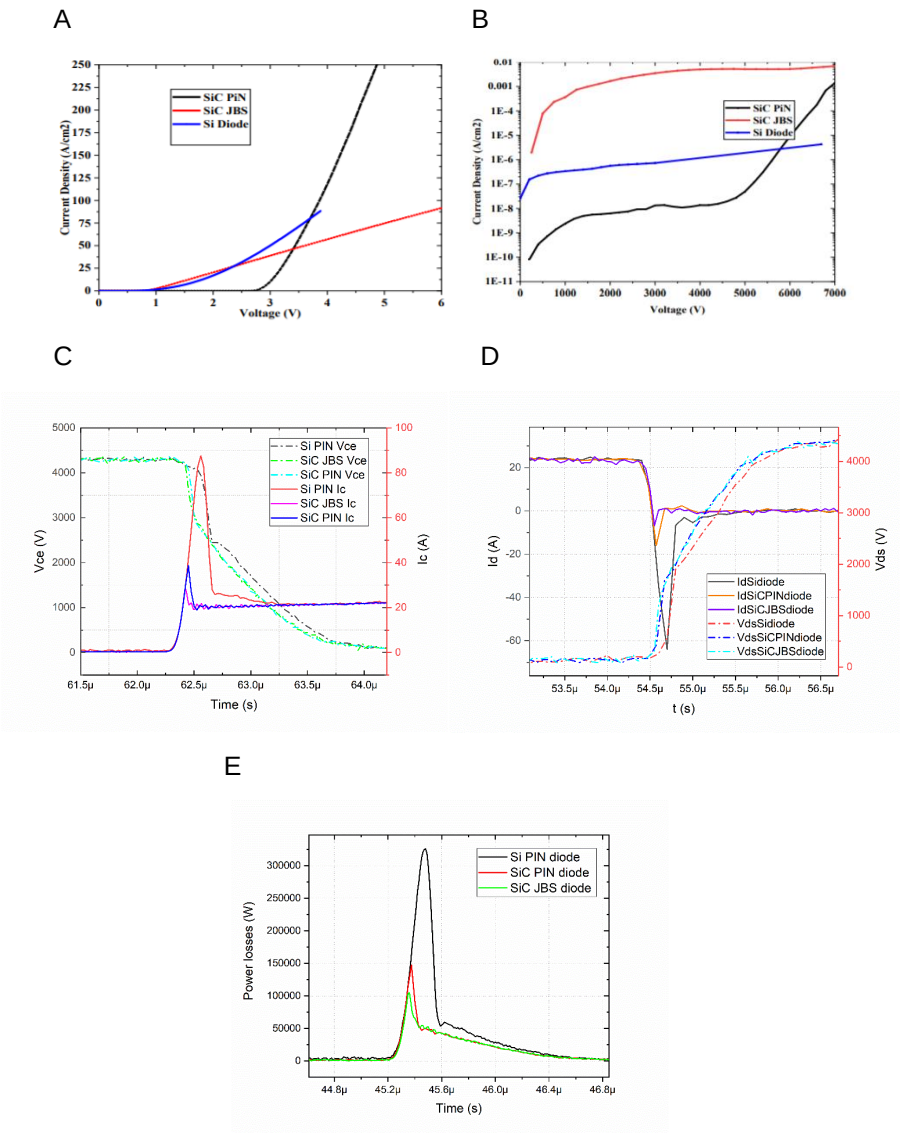


Figure 27: A) Comparison of forward characteristics of 6.5 kV SiC PIN & JBS diodes with Si diode, B) Comparison of reverse characteristics of 6.5 kV SiC PIN & JBS diodes with Si diode C) 6.5 kV Si IGBT characteristics when turned on with Si PIN, SiC PIN and SiC JBS diodes and, D) 6.5 kV Si PIN, SiC PIN and SiC JBS diodes characteristics when turned off with a 6.5 kV Si IGBT, E) Comparison of power losses of 6.5kV Si IGBT during turn-on, when switched with SiC PiN, SiC JBS or silicon diode.

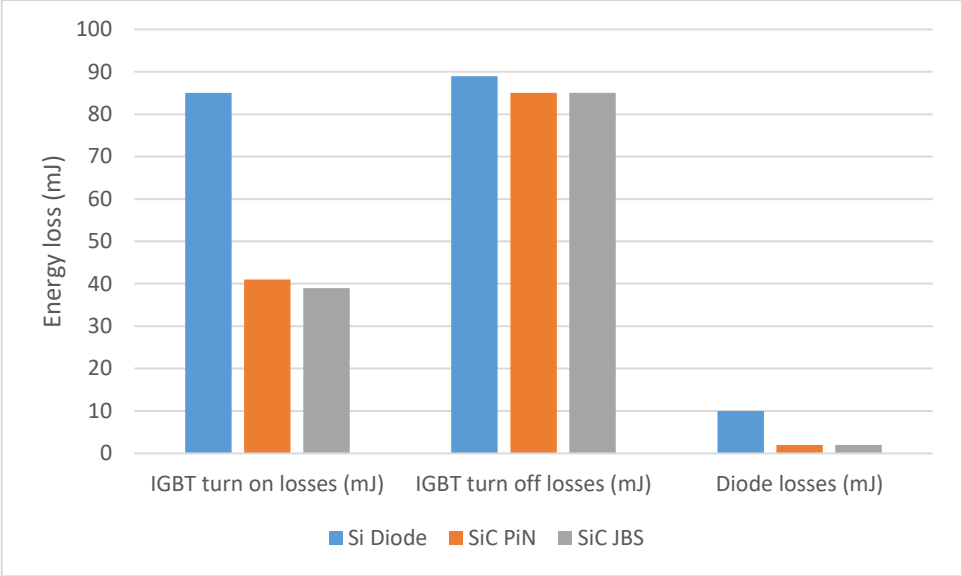


Figure 28: Comparison of energy losses in the 6.5kV Si IGBT switched with Si PiN, SiC PiN and SiC JBS diodes.

3.6 Comparison between 6.5 kV SiC MOSFET/6.5 kV SiC PiN Diode & 6.5 kV SiC MOSFET/6.5 kV SiC JBS Diode– Dynamic performance

Dynamic performance of full 6.5 kV SiC configurations have also been investigated in the DPT. The replacement of Si IGBTS by SiC MOSFETs offers some advantages by substantially decreasing the switching losses and reducing the conduction losses at lower power output levels. Two different configurations were tested under nominal voltage of 3.6 kV and current of ~12 A: 6.5 kV SiC MOSFET/6.5 kV SiC PiN Diode & 6.5 kV SiC MOSFET/6.5 kV SiC JBS Diode.

Figures 29A-B show the MOSFET turn-off characteristics from both configurations with a switching time of approx. 400 ns. Figures 29C-D show the SiC MOSFET turn-on curves and SiC diodes turn-off curves, respectively. The diodes reverse recovery currents could be extracted from these curves, with the SiC PIN diode presenting a higher reverse recovery current peak (~5 A) than the SiC JBS diode (~0 A). Such fact was already stated in Figure 29 and discussed previously.

Regarding the switching times, from Figure 29C, the 6.5 kV SiC MOSFET/6.5 kV SiC PIN Diode configuration presented a switching time of approx. 600ns, which is smaller when compared to the 6.5 kV Si IGBT/6.5 kV SiC PiN Diode configuration (higher than 1 µs – Figure 29D). This fact was already expected since SiC MOSFETs present lower switching losses when compared to silicon devices. The 6.5 kV SiC MOSFET/6.5 kV SiC JBS Diode configuration presented a higher switching time because the SiC MOSFET used in this test has a higher pitch than the SiC MOSFET used with the SiC PiN diode. Extracted losses are similar for the MOSFETs with JBS and PiN diodes as shown in figure 30 and thus those devices can be selected based on application. For HV application where sub-load regime is predominant, the SiC JBS diode will deliver lower conduction losses, while in full load, the PiN will exhibit superior performance.

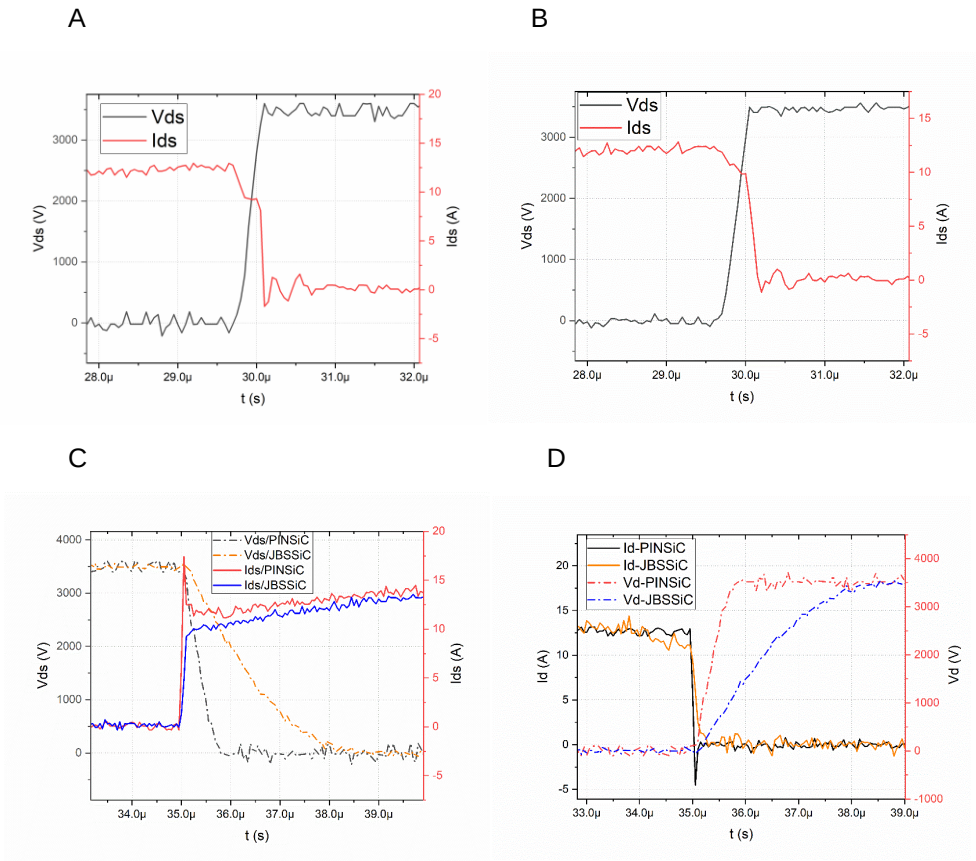


Figure 29: A) 6.5 kV SiC MOSFET characteristics when turned off with 6.5 kV SiC PIN diode, B) 6.5 kV SiC MOSFET characteristics when turned off with 6.5 kV SiC JBS diode, C) 6.5 kV SiC MOSFET characteristics when turned on with 6.5 kV SiC PIN and SiC JBS diodes and, D) 6.5 kV SiC PiN and SiC JBS diodes characteristics when turned off with a 6.5 kV SiC MOSFET.

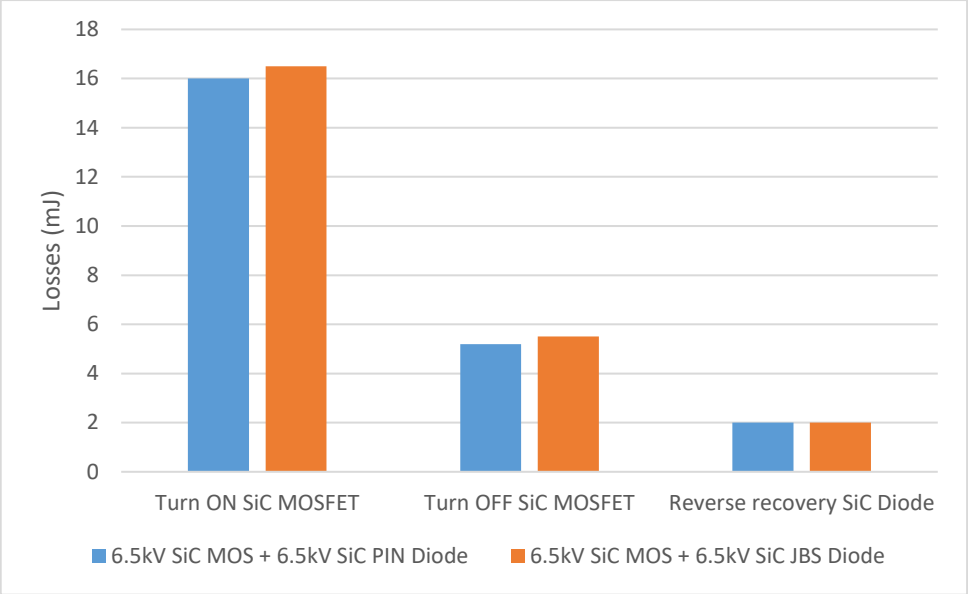


Figure 30: Comparison of energy losses in the 6.5kV SiC MOSFETs switched with SiC PiN and SiC JBS diodes.

Finally, in order to compare the potential of the SiC MOSFET + PiN technology with Si IGBTs + PiN, the switching losses are shown in Figure 31. The SiC HV combination has more than 5 times lower turn-on losses, 18 times lower turn-off losses and about 5 times lower reverse recovery PiN diode losses. In terms of switching losses, 6.5 kV SiC devices outperform Si significantly, and it is therefore of great potential for high frequency MV drive applications.

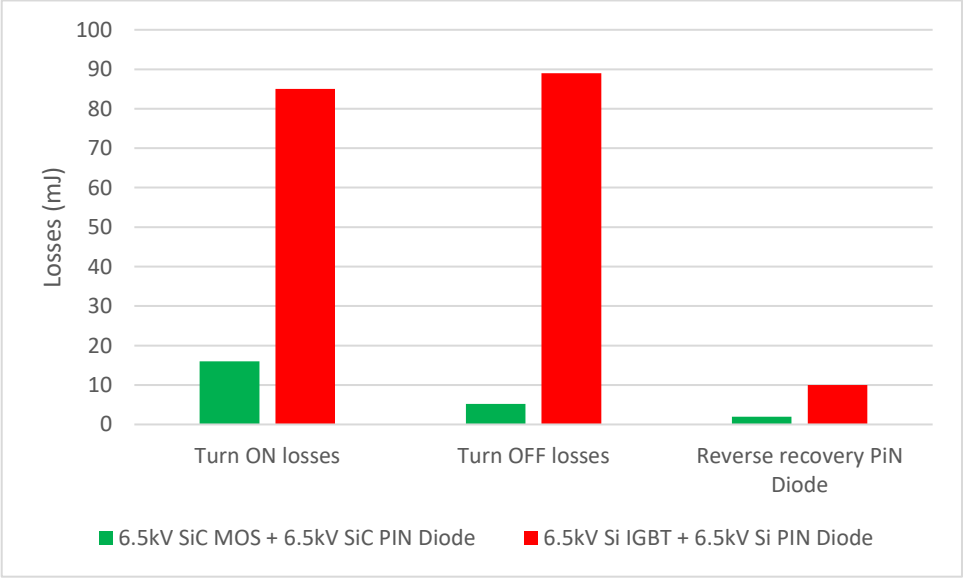


Figure 31: Comparison of energy losses in the 6.5kV SiC MOSFETs switched with SiC PiN and SiC JBS diodes.

3.7 H3TRB – 6.5 kV SiC PIN Diode

The termination ruggedness from the fabricated 6.5 kV SIC PiN diodes has been evaluated in a H3TRB test. Four diodes were submitted to a reverse bias of 5.2 kV (80% of 6.5 kV), an ambient temperature of 85 C and 85 % relative humidity. The diodes were identified with the following codes: X0X1, X0Y10, X2Y1 and X9Y4. The results indicated in Figure 32A show that two diodes successfully passed through the test (X0X1 & X9Y4), enduring the 1000 h without sudden failure. It is also important to mention that these two devices did not present leakage current increase during the test as well as no dendrites growth, as shown in Figure 32B from a microscopy photo captured after the test. Both characteristics are indicatives of no chip blocking degradation. Two diodes presented a termination failure during the test (see Figure 31C), with the X2Y1diode failing in the first 30 minutes and the X0Y10 diode failing after 150 h from the test beginning. The premature failure from these diodes is related to external factors, such as the presence of particles in the termination and not to the device termination design.

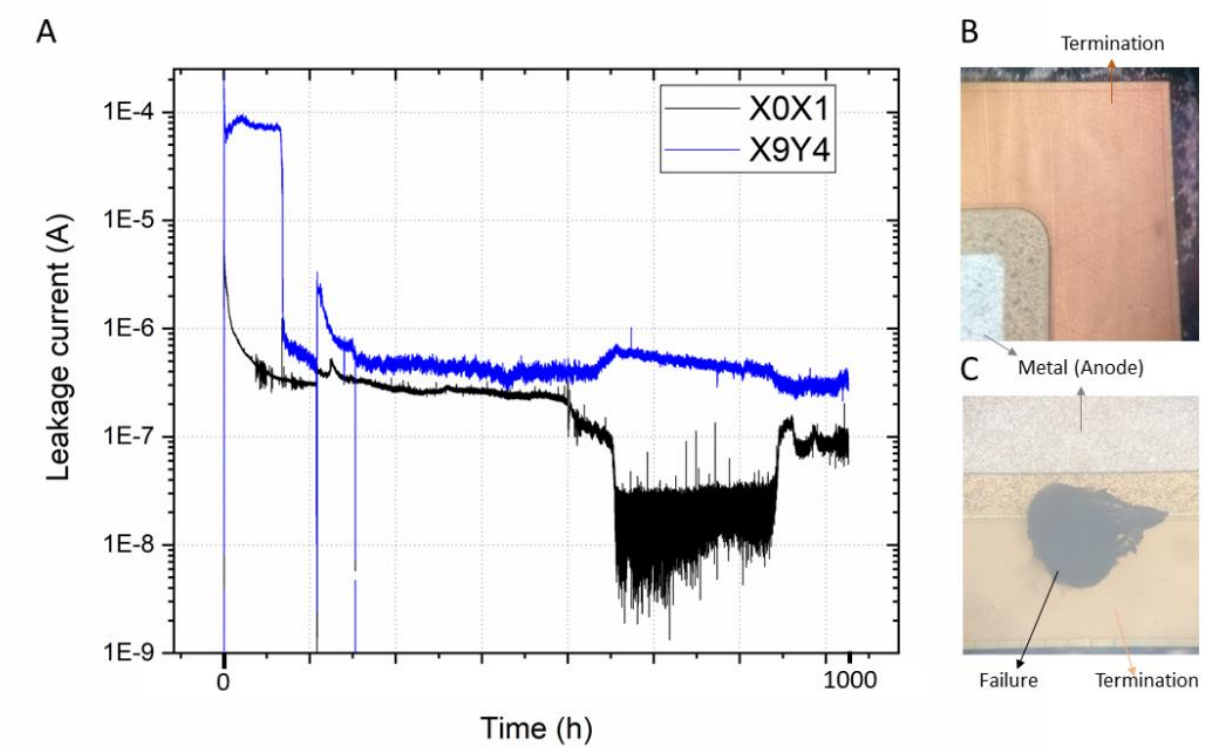
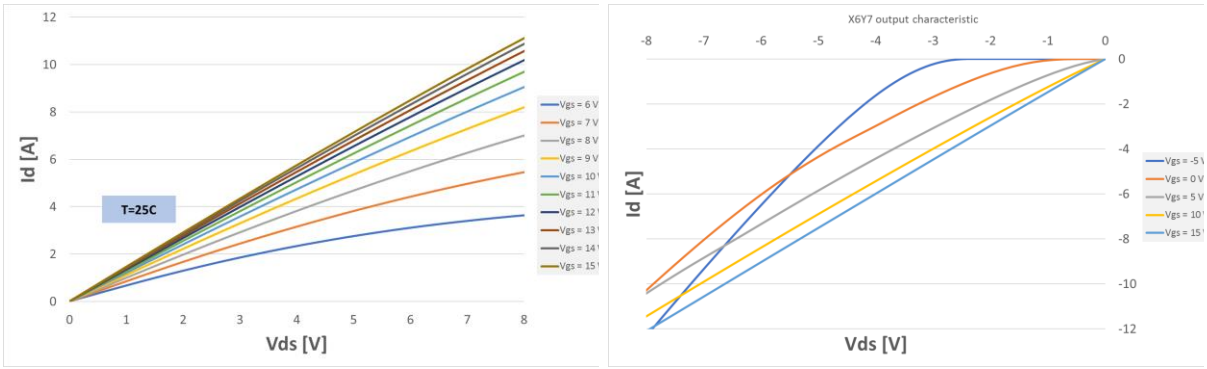


Figure 32: A) Leakage current of the tested 6.5 kV PiN diodes during H3TRB test, B) X9Y4 device termination microscopy photo after 1000 h of test, C) X2Y1 device termination microscopy photo after failure.

3.8 10 kV SiC MOSFET/10 kV SiC PiN Diode – Dynamic performance

Medium voltage power electronic applications like grid-tie converters and solid-state transformers are excellent candidates to implement 10 kV SiC devices in their topologies to enhance electrical and thermal converter performance. Hitachi ABB Power grids (HAPG) designed and fabricated 10 kV SiC MOSFETs and PIN diodes. The static characteristics (1st and 3rd quadrant operation) of a 10kV SiC MOSFET are depicted in figure 33, showing both the MOSFET output characteristics 33(a) and body diode characteristics 33(b). The dynamic behavior of the 10kV SiC MOSFET/PiN diode combination was characterized at the DPT from FHNW under a nominal voltage of 6 kV and switching current of about 10 A, as demonstrated in Figure 34.



(a) (b)

Figure 33 (a) Forward IV characteristics of a 10kV SiC MOSFET and (b) 3rd quadrant IV characteristics of a 10kV SiC MOSFET

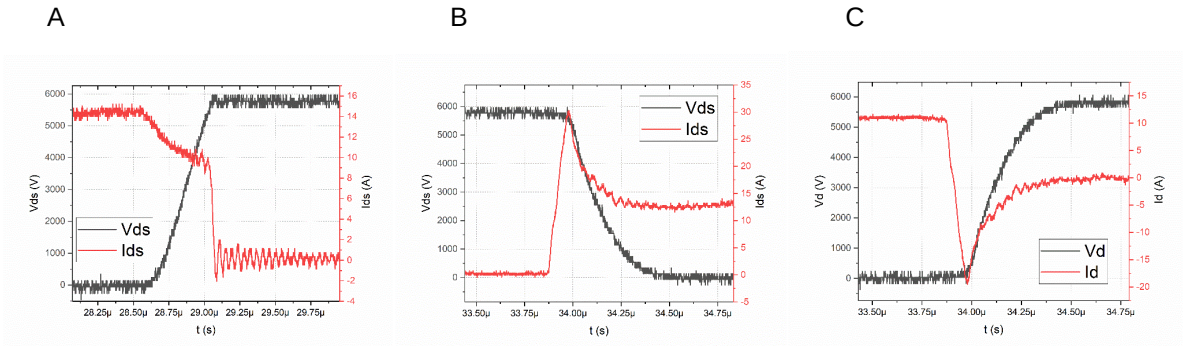


Figure 34: A) 10 kV SiC MOSFET characteristics when turned off with 10 kV SiC PIN diode, B) 10 kV SiC MOSFET characteristics when turned on with 10 kV SiC PIN diode, and C) 10 kV SiC PIN diode characteristics when turned off with 10 kV SiC MOSFET.

The turn-off characteristic from the MOSFET device presented current ringing due to the fast switching and circuit parasitic (Figure 34A). From the MOSFET turn-on waveform (Figure 33B) and PIN diode turn-off waveform (Figure 34C) is possible to extract the maximum PIN diode reverse recovery current of approx. 20 A and a MOSFET turn on switching time of ~300 ns. The waveforms indicate proper operation of the devices and validate the proposed 10 kV device design. Figure 35 depicts the energy losses extracted from the switching curves for the SiC 10kV MOSFETs and PiN diodes.

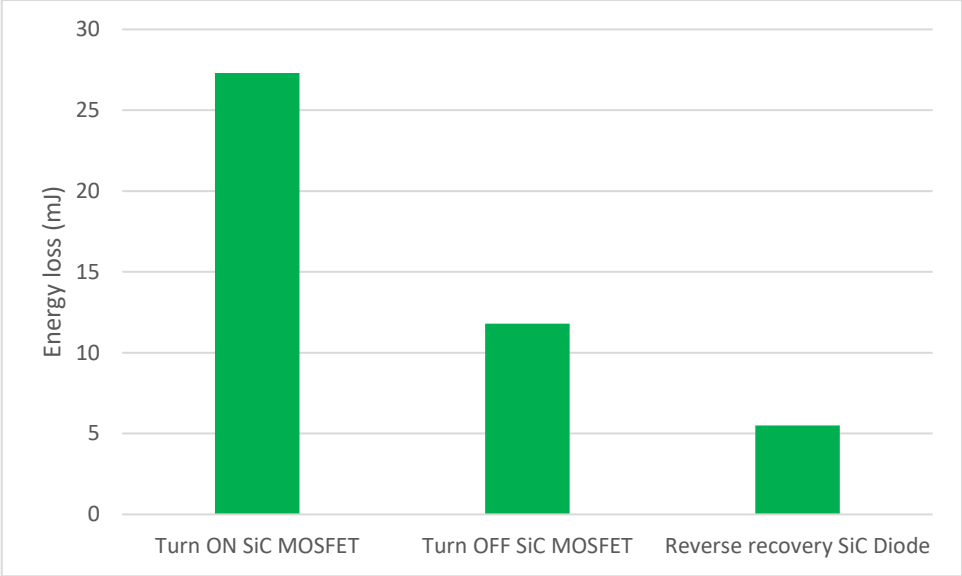


Figure 35: A) 10 kV SiC MOSFET characteristics when turned off with 10 kV SiC PIN diode, B) 10 kV SiC MOSFET characteristics when turned on with 10 kV SiC PIN diode, and C) 10 kV SiC PIN diode characteristics when turned off with 10 kV SiC MOSFET.

4 Conclusions

In the project AMPERE, HITACHI-ENERGY and the FHNW have developed advanced HV SiC device technologies beyond state-of-the-art. We have focused our efforts to develop technology platforms comprising design simulations, microtechnology processes, process integration schemes and characterization systems for 6.5 and 10 kV SiC switches and diodes. For these HV classes, SiC has strong potential to enable higher efficiency, lower size footprint converters with reduced number of levels, thereby, challenging current state-of-the-art Si IGBT based technologies. The devices fabricated in AMPERE are the first ones made in Switzerland, and as such a great technology step for the Swiss power electronics industry. This included high voltage SiC PiN diodes and MOSFETs, featuring enhanced performance and reliability. The project also supported the development of infrastructure development in Switzerland, that will further allow the development of the technology towards industrial products. The potential is underpinned by the strong collaboration and expertise of the involved partners. The results will now be used for the development of new HV device technologies, but also provide a basis for the development of new power electronics topologies and applications.

5 Outlook

As an outlook, the results achieved in AMPERE will be used to established more energy efficient WBG power semiconductor in the research and manufacturing landscape of Switzerland. The devices and characterization achieved in this project will further provide valuable information for the development of new power electronics topologies and applications. Among those applications, we expect the knowledge gained in this project to contribute to the development of MV drives for industrial motors and traction, as well as HVDC, railway and ships. These applications consume significant energy, and the incorporation

of HV SiC devices will make them more efficient. The results obtained in this project will lay the foundation for the development of new HV products according to market development. Hitachi Energy Semiconductors is working towards the first R&D samples of 3.3 and 6.5kV-rated SiC modules. The first SiC-based products in these voltage ranges are expected towards the second half of 2023.

6 National and international cooperation

The project partners are the FHNW and Hitachi Energy in Switzerland.

7 References