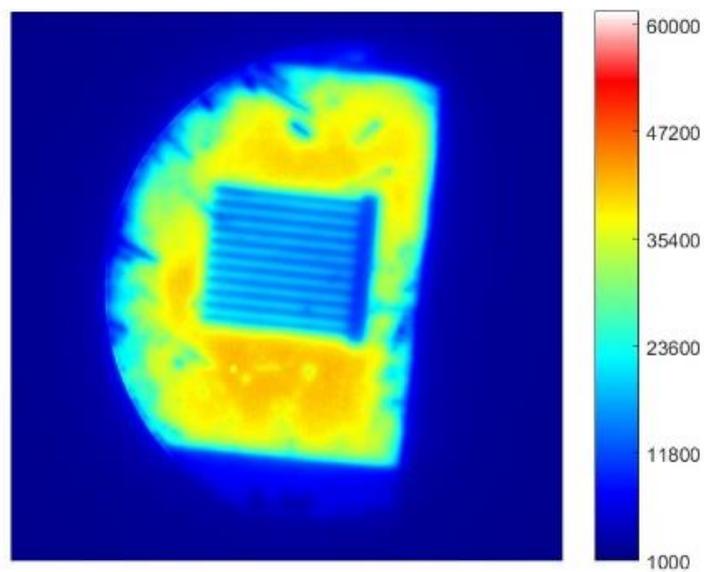




Final report

CHES

Silicon solar Cells with High Efficiency integrating paSSivating contacts: materials and processes





Date: 26.02.2021

Place: Bern

Publisher:

Swiss Federal Office of Energy SFOE
Research Programme Photovoltaics
CH-3003 Bern
www.bfe.admin.ch
energieforschung@bfe.admin.ch

Agent:

Ecole Polytechnique Fédérale de Lausanne (EPFL)
Photovoltaics and Thin Film Electronics Laboratory (PV-Lab)
Maladière 71b
CH-2000 Neuchâtel
pvlab.epfl.ch

Authors:

Andrea Ingenito, PV-Lab, andrea.ingenitio@epfl.ch
Audrey Morisset, PV-Lab, audrey.morisset@epfl.ch
Franz-Josef Haug, PV-Lab, franz-josef.haug@epfl.ch
Christophe Ballif, PV-Lab, christophe.ballif@epfl.ch

SFOE head of domain: Stefan Oberholzer, stefan.oberholzer@bfe.admin.ch
SFOE programme manager: Stefan Oberholzer
SFOE contract number: SI/501696-01

The author of this report bears the entire responsibility for the content and for the conclusions drawn therefrom.



Summary

In the mid-to-long term, the full efficiency potential of crystalline silicon wafer should be exploited because higher efficiency modules lower installation costs, save area and ultimately reduce electricity costs. The CHESS project aims at developing passivating contacts for silicon solar cells and to define simple processing steps for their integration into mainstream production. Such contacts hold the promise to increase the efficiency. Thus, we focused on passivating contacts for the more common *p*-type wafers, and we study their compliance with diffusion of the *pn*-junction and the firing of the metallization. We developed processes to realize solar cells with passivating contacts on both sides, and we explored interdigitated back contacted (IBC) solar cells as the ultimate solution to reach high conversion efficiencies. Within this project, we could successfully demonstrate the integration of firing compatible passivating contacts on the rear side of *p*-type *c*-Si solar cells with conversion efficiencies up to 22.5%. Additionally, we introduced a novel metallization process for passivating contacts. Our approach is based on a thin transparent conductive oxide capped with a silicon nitride dielectric layer following by annealing at 350°C. The advantages of this approach are: full recovery of sputtering damage, process simplification and reduction of material costs (only 15 nm thick ITO was used). The proposed process was used to demonstrate solar cells with front and rear passivating contacts with conversion efficiencies up to 22.8%. Finally, we explored masking deposition as potential solution to simplify patterning of passivating contacts in IBC architecture. During the whole duration of the project, we conducted advanced characterization techniques to provide novel insights on the working principles of passivating contacts. In particular, we demonstrated the role of hydrogen to the passivation of interfacial defects, and that the crystallinity fraction of the layer is decisive for the activation of its dopants.

Zusammenfassung

Das Projekt «CHESS» widmete sich der Entwicklung von passivierenden Kontakten für Silicium Solarzellen auf der Basis von vereinfachten Prozessschritten, um eine rasche industrielle Umsetzung zu ermöglichen. Daher konzentrierten wir uns auf Kontakte für *p*-dotierte Wafer die mit dem Diffusionsprozess des *pn*-Überganges und mit dem Feuerschritt der Metallisierung kompatibel sind. Wir entwickelten Solarzellen sowohl mit beidseitig passivierenden Kontakte als auch mit passivierenden Kontakten auf der Rückseite, um höhere Wirkungsgrade zu erzielen (sogenannte IBC Zellen für «interdigitated back contacts»). Im Rahmen des Projektes konnten wir so die Integration von feuerbaren Rückkontakten für *p*-dotierte Zellen zeigen, die Wirkungsgraden bis 22.5 % erzielen. Parallel dazu entwickelten wir neue Metallisierungsprozesse für die Vorderseite. Diese beruhen auf einer transparenten leitfähigen Schicht in Kombination mit Silicium Nitrid, gefolgt von einem Tempersschritt bei 350 °C. Die Vorteile liegen in einer deutlichen Materialersparnis, da die ITO Schicht nur 15 nm dick ist, und in einer kompletten Ausheilung der Grenzflächendefekte, die während der Abscheidung entstehen. Entsprechende Solarzellen erzielten Wirkungsgrade bis 22.8 %. Schliesslich untersuchten wir die Abscheidung durch Schattenmasken um die Strukturierung von IBC Kontakten zu vereinfachen. Während des gesamten Projektes wurden die Entwicklungsschritte mit einer Vielzahl von Analysemethoden begleitet, um ein tieferes Verständnis der passivierenden Kontakte zu erlangen. So konnte zum Beispiel gezeigt werden, dass Wasserstoff entscheidend zur Passivierung der Grenzflächendefekte beiträgt, und dass die Kristallinität der Schichten für die Aktivierung von Dotierstoffen entscheidend ist.

Résumé



À moyen et long terme, le potentiel d'efficacité maximum du silicium cristallin devrait être exploité pleinement car des modules à plus haut rendement économisent de l'espace et de l'installation et réduisent finalement les coûts d'électricité.

Le projet CHESSE visait à développer des contacts passivants pour les cellules solaires en silicium cristallin (c-Si) et à identifier des procédés simples pour leur intégration à l'échelle industrielle. Ces contacts offrent justement un potentiel de rendement plus élevé. Nos efforts se sont plus particulièrement concentrés sur le développement de contacts passivants compatibles avec des plaquettes en c-Si de type p (les plus couramment utilisées dans l'industrie), ainsi qu'avec des étapes industrielles à haute température (par exemple : diffusion de la jonction p-n et recuit rapide pour la métallisation). Nous avons développé des procédés permettant la fabrication de cellules solaires passivées des deux côtés, et nous avons exploré la fabrication de cellules solaires avec les deux types de contacts à l'arrière (structure dite « IBC ») comme solution ultime pour atteindre des rendements de conversion élevés. Dans le cadre de ce projet, nous avons démontré avec succès l'intégration de contacts passivants compatibles avec un recuit rapide à l'arrière de cellules solaires c-Si de type p avec des rendements de conversion atteignant 22,5%. De plus, nous avons introduit un nouveau procédé de métallisation des contacts passivants, basé sur l'empilement d'une couche diélectrique de nitrure de silicium sur un oxyde transparent conducteur (OTC) mince suivi d'un recuit à 350°C. Cette approche innovante permet la régénération complète des dommages causés par la pulvérisation de l'OTC, la simplification du procédé et la réduction des coûts liés aux matériaux (OTC réduit à seulement 15 nm d'épaisseur). Ce procédé a permis la démonstration de cellules solaires avec des contacts passivants des deux côtés avec des rendements de conversion jusqu'à 22,8%. Enfin, nous avons exploré le dépôt des couches passivantes à travers des masques comme solution pour simplifier la localisation des contacts passivants dans l'architecture IBC. Pendant toute la durée du projet, nous avons aussi mené des travaux de caractérisation avancés qui ont permis une meilleure compréhension des mécanismes fondamentaux associés aux contacts passivants développés. En particulier, nous avons étayé la compréhension du rôle de l'hydrogène, et que la fraction cristalline des couches passivantes contrôle l'activation de la dopage.



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List of abbreviations

WP	Work-package
BSF	Back surface field
c-Si	crystalline silicon
E_F	Fermi-level
FF	Fill factor
FPC	Fired passivating contact
GW_p	Gigawatt, produced under ideal illumination (peak)
IBC	Interdigitated back contact
ITO	Indium tin oxide; a transparent conductive oxide used for contacting
TMB	Trimethylboron
iV_{oc}	Implied open circuit voltage, projected from a contactless lifetime measurement
j_{sc}	Short circuit current density
p -type	p -doped semiconductor; in silicon: doped with Al or B
n -type	n -doped semiconductor; in silicon: doped with P
PERC	Passivated emitter and rear cell
$POCl_3$	Phosphorous oxychloride; used for diffusion of the pn -junction
poly	Polycrystalline layer (after crystallisation)
PECVD	Plasma enhanced chemical vapor deposition
PSG	Phosphosilicate glass; a layer grown during phosphorous diffusion
SiC _x	Silicon carbide, in this context containing only a few at% of C
SiN _x	Silicon nitride; usually Si-rich and hydrogenated
SiO _x	Silicon oxide; in this context Si-rich
V _{oc}	Open circuit voltage
ECV	Electrochemical capacitance-voltage
SIMS	Secondary Ion Mass Spectrometry



1 Introduction

This project is devoted to the development and the integration of a new generation of passivating contacts for crystalline silicon solar cells. Based on the unique expertise in plasma deposition developed at the PV-Lab in Neuchâtel, we could obtain key insights into the operation principle of passivating contacts and thus contribute to extending the learning curve of standard c-Si solar cell technologies. The project demonstrated various options for lean processing of passivating contacts, contributing to reducing the cost of solar electricity and mitigating the space usage of photovoltaics.

2 Context

2.1 Background / State of the art

A recent article in the journal Science investigated different scenarios towards extending photovoltaic electricity production into the Terawatt scale [1]. According to their more conservative estimates, the annual global manufacturing capacity could reach between 500 GW_p/y and 1 TW_p/y by 2030. Based on the current value of 100 GW_p/y, this corresponds to annual growth rates of 15% and 21%, respectively, and past experience suggests that these figures are not unrealistic. Since crystalline silicon (c-Si) contributes more than 90% to the current global PV production, it is likely that this technology will keep its dominating role throughout this period and beyond. In order to shoulder this growth, the production capacity will need substantial upgrades and also the efficiency of mass-produced cells should be further improved. Considering the tough financial environment of PV, both measures should come with a minimum of investment. Thus, it is crucial to provide to cell manufactures the building blocks that give them the possibility to integrate novel concepts into existing manufacturing processes without radical changes.

2.2 Motivation of the project

The theoretical efficiency limit of silicon solar cells is at 29.4% [2] and various research groups and companies have demonstrated impressive progress towards this limit by the incorporation of passivating contacts. The highest ever demonstrated efficiency of 26.7% relies on low-temperature passivating contacts [3]. Alternatively, passivating contacts that are more compatible with standard processing steps at high temperature achieved efficiencies between 25.7 [4] and 26.1% [5]. However, they are either based on *n*-type wafers which are less common in manufacturing [4], or they employ rather complicated fabrication steps [5]. Therefore, passivating contacts are not yet widely used in industrial production. The CHESS project is devoted to bridging this gap by the development of passivating contacts that are compatible with the standard processing sequence wherever possible. Thus, we aim at providing a lean integration strategy that needs only one or two additional components.

2.3 Goals

The goals of the CHESS project are threefold: First, we will investigate passivating contacts for the upgrading of the rear side of industrial solar cells. For this reason, passivating contacts, which can be integrated into current manufacturing steps such as phosphorous diffusion process for forming the front emitter or firing necessary for cell metallization. Once those recombination losses at rear side are reduced, conversion efficiency may become front side limited. We also explore passivating contacts that are suitable for front side applications. This requires not only excellent surface passivation and charge carrier transport but also high optical transparency. To reduce electrical losses while maximizing light in



coupling in the solar cells, as the third objective we investigate masking depositions for localization of the front passivating contact or by moving both contact types to the rear of the cell. To reach such objectives, we will rely on tunnel oxide optimization, advanced metallization for passivating contacts and advanced characterization.

3 Approach and methodology

Figure 1 illustrates the working principle of different rear contacts in p -type solar cells. The rear contact of such a cell should collect holes that are majority carriers, but it should avoid that minority carriers reach the rear contact. The left panel shows the contact used in many of the current solar cells. It employs a thick region with higher doping at the rear of the wafer, which yields an upwards band bending at the interface between the p -type bulk and the p^+ -type region. Thus, electrons feel a weak field effect passivation, which is called **back surface field** (BSF). Nevertheless, there is a considerable chance that they overcome the weak band bending and reach the interface to the metal, which is characterized by a high density of recombination centers. Currently, industry switches to the improved design of the **passivated emitter and rear cell** (PERC). In this cell type, most of the rear area is covered by an insulating dielectric such as Al_2O_3 . Subsequently, small areas are opened in the insulator with a laser process and contact is established through these openings with the same process as in the BSF design. Thus, electrons are still exposed to the recombination mechanism at the contact to the metal, but the extent is reduced proportionally to the reduced area.

Passivating contacts change on this situation by a variety of measures (fig. 1, middle and right panels); first, the doped region is narrower and its band bending is stronger; second, there is chemical passivation since there are fewer defects at the interface between silicon and the oxide; and third, the loss of minority carriers is further reduced by the tunnelling probability through the interfacial oxide.

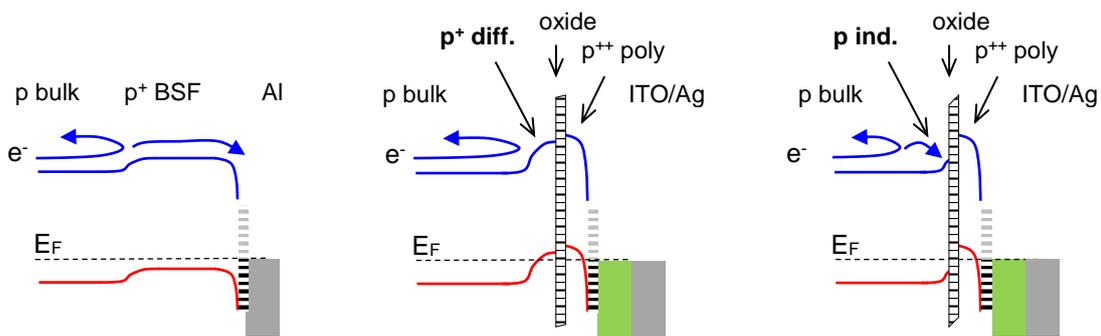


Figure 1: Illustration of the rear contact in standard solar cells (left) and the passivating rear contacts envisioned in this project, either annealed with band bending due to an in-diffused p^+ region (middle) or fired where band bending is induced across the oxide (right).

4 Results and discussion

4.1 $POCl_3$ integration

Passivating contact technologies compatible with the thermal budget of currently manufactured solar cells are optimized. The scope is to demonstrate solar cells with an industrial diffused emitter combined



with one of the full-area passivating contact technologies (integrated within the diffusion or firing processes) on the rear side with an efficiency above 23%.

4.1.1 Integration of diffused passivating contact

Solar cells were prepared by depositing a $\mu\text{c-Si(p)}$ layer via PECVD on top of a chemically grown thin tunnelling SiO_x layer (1.2 nm). Within the same PECVD process, another thick intrinsic $\text{SiO}_x(\text{i})$ layer was also deposited to act as a P-diffusion barrier (as sketched in Figure 2, left). The whole structure is then loaded into a tube furnace and exposed to a POCl_3 diffusion process that occurs on both sides of the wafers, thus motivating the need for a P-diffused barrier on the $\mu\text{c-Si(p)}$ on the rear that allows avoiding unwanted n doping. The doping profiles measured by ECV for the $\mu\text{c-Si(p)}$ with different thicknesses of the SiO_x -diffusion barrier, after removal of the latter, are illustrated in Figure 2, right. A clear drop in B concentration is observed for the sample without the diffusion barrier suggesting P-doping compensation of the $\mu\text{c-Si(p)}$ layer. SiN_x layers were then applied to both surfaces, a fire-through Ag paste was screen printed on the front and the samples were fired at 840°C on a belt furnace. The implied V_{oc} of the cells was monitored during all steps to allow an assessment of the passivation. For the $\mu\text{c-Si(p)}$ we used two thicknesses namely 40 and 80 nm. Figure 3 shows that the rear contact is successfully formed with the thermal budget of the POCl_3 diffusion. Firing improves the iV_{oc} further to around 690 mV, thanks to defect passivation due to hydrogen that is released from the SiN_x . After stripping of the rear SiN_x , the samples were finished with a low-temperature rear metallization of sputtered indium tin oxide (ITO) and silver in order to assess j_{sc} and FF . The cells show j_{sc} up to 40.4 mA/cm^2 and FF up to 75%. Unfortunately, the efficiencies of this batch reached only 20.1% since sputtering damages reduced the V_{oc} to around 660 mV, a massive drop with respect to the iV_{oc} values before sputtering. The obtained efficiency values were lower than expected and therefore we decided to put more effort on the more promising fired passivating contact approach.

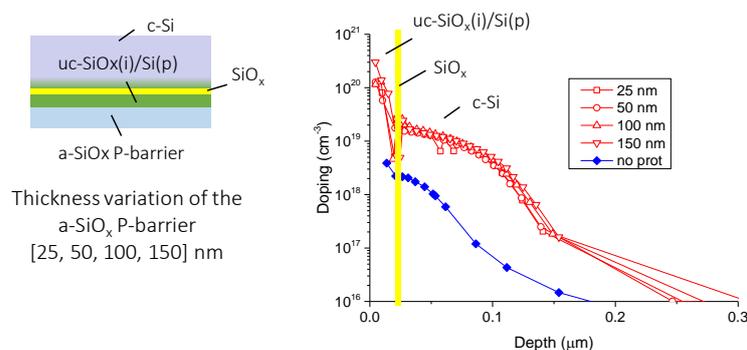


Figure 2: (left) Sketch of the $\mu\text{c-Si(p)}$ layer capped with an a-SiO_x barrier, to prevent P-diffusion, having different thicknesses [25, 50, 100, 150] nm. (right) Measured B diffusion profile with and without the a-SiO_x . All samples were exposed to a POCl_3 diffusion process.

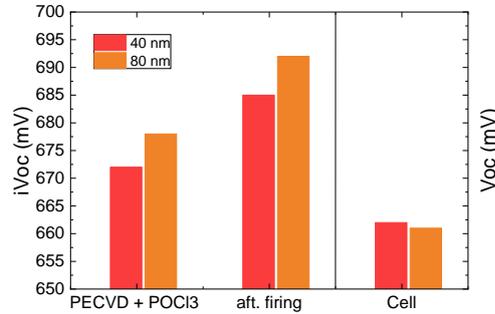
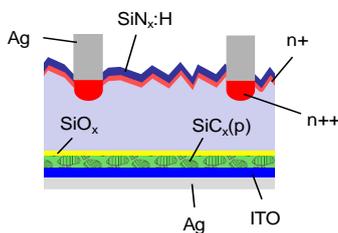


Figure 3: iV_{oc} values measured at different stages of solar cell processing. Two $\mu\text{-Si(p)}$ layers 40 and 80 nm thick were tested.

4.1.2 Integration of fired passivating contact

Towards the second route of integration with the standard cell process, we investigated passivating contacts that are compatible with the firing process used for metallization formation of manufactured c-Si solar cells [6]. We termed this approach fired passivating contact (FPC).

For the integration of the FPC in solar cells, the P-diffusion is first performed. As the diffusion process occurs on both sides of the wafer, the P-doped region is subsequently etched away from the rear side in an alkaline bath. Only then the stack of interfacial oxide and passivating $\text{SiC}_x(\text{p})$ is applied to the rear and SiN_x is deposited on both sides of the wafer. Finally, the front metallization is printed and the whole stack is fired. Since the firing process is characterized by a very fast heating ramp of around $50^\circ\text{C}/\text{sec}$, the formation of molecular hydrogen might build up enough pressure to delaminate the SiC_x film from the wafer. Therefore, we developed a p-type SiC_x layer, in which the addition of carbon provides excellent adhesion to the underlying oxide as well as strong hydrogen bonding within the layers. So far, the described processing sequence is exactly the same as the one used for manufacturing of industrial PERC cell. The rear is then finished with an HF etching to remove the rear SiN_x layer, followed by a low-temperature metallization process based on sputtering of ITO/Ag. Those steps are non-standard in production, and we plan to replace them by means of screen-printing metallization. Figure 4 right shows the solar cell architecture integrating the FPC. The V_{oc} of 682 mV, a current density (J_{sc}) of $41.8 \text{ mA}/\text{cm}^2$ (with a double antireflection coating) and a FF of 79%, result in an efficiency of 22.5%.



Front side coating	Rear FPC	η [%]	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]
SiN_x	HD- $\text{SiC}_x(\text{p})$	21.8	680	40.9	78.5
SiN_x	$\text{Si(i)}/\text{SiC}_x(\text{p})$	22.0	682	41.15	79.0
$\text{SiN}_x/\text{MgF}_2$	$\text{Si(i)}/\text{SiC}_x(\text{p})$	22.5	682	41.8	79.0

Figure 4. Sketch of the solar cell architecture with FPC.

Table I. Summary of the measured JV parameters for the best cell.

4.2 Co-annealed front and rear contacted solar cells

WP2 of this project is devoted to the development of the next generation of front and rear side contacted solar cells employing full-area passivating contacts. We aim at demonstrating co-annealed solar cells with conversion efficiency above 24%.



4.2.1 Development of highly transparent annealed passivating contacts for textured surfaces

We processed c-Si solar cells integrating SiN_x:H/ITO/ μ c-Si(n) front contacts obtained according to the processing sequence described in Figure 7 of section 4.3.1. The final cell architecture is shown in Figure 5 a. The J-V characteristics obtained from the I-V measurements of the best cell are shown in Figure 5 b. We measured V_{oc} of 719 mV and FF of 81.9%. The conversion efficiency is limited by a relatively low J_{sc} of 38.6 mA/cm². Finally, we reached record conversion efficiency of 22.8% (for this type of cell architecture). To understand the losses at the cell level, $SunV_{oc}$ is also displayed on this graph. We attributed the loss of V_{oc} to the rear contact since the iV_{oc} measured previously on symmetrical n-type textured samples was above 728 mV. By comparing the EQE of our best cell with a cell made with a standard process (see reported in [11]), we observe a decrease response in the near IR-region, which we attribute to free carrier absorption in the ITO (Figure 5 c). By optimizing the front TCO to enable $J_{sc} > 40$ mA/cm², our results pave the way for >24% conversion efficiency.

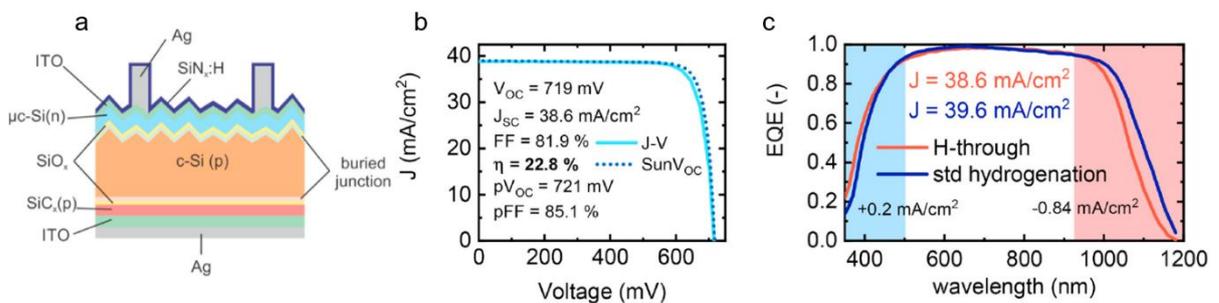


Figure 5: a. Schematic of the solar cell structure with the H-through process applied at the front side b. J-V characteristics and $SunV_{oc}$ measurement of the best cell obtained based on the H-through process c. EQE of the best cell made with the H-through process and of a cell made with the std hydrogenation process.

Towards the integration of passivating contacts into more industrially compatible processes we investigated the possibility to replace the front side low-T metallization process with screen printing and firing-through of Ag paste. Rear emitter solar cells with two-side passivating contacts were fabricated as depicted in Figure 6(a). For such cells we used the same μ c-Si(n) and SiC_x(p) that were developed for the H-through approach. Thus, we deposited on top of a UV-O₃ grown tunnel oxide, the μ c-Si(n), on the front textured side, and SiC_x(p) on the planar rear side. We investigated μ c-Si(n) with thicknesses variation from of 15, 20, 30, 60, 80 and 120 nm deposited over the full wafer front side. An annealing step in a tube furnace at 850°C for a dwell time of 30 s was performed. Then a SiN_x layer was deposited on each side of the wafer followed by screen-printing of an Ag-grid on the front side and firing at peak temperature of 800°C. Afterwards, the cells were finished by etching of the rear SiN_x followed by sputtering of an ITO/Ag stack. As shown in Figure 6 (b)-(c), the FF was found to slightly increase towards thicker layers whereas a strong increase in V_{oc} from 660 mV to 700 mV was measured when increasing the layer thickness from 15 to 120 nm. This effect is explained by the confinement of the Ag-crystallites within the μ c-Si(n) when its thickness is increased: hence, an electrical contact with passivating contact is formed between the passivating contact and the metal paste without damaging the interfacial SiO_x. However, such thick layers are responsible for strong optical losses (see Figure 6(d)) limiting the final conversion efficiency below 20 % (Figure 6 (e)).

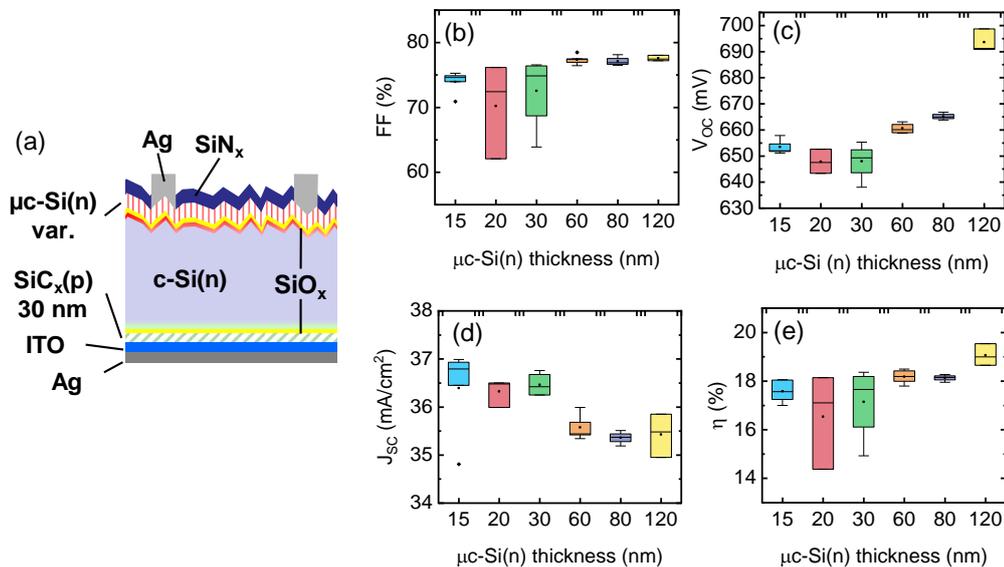


Figure 6: Sketch of n-type c-Si solar cell with full-area two side passivating contacts. The front side $\mu\text{c-Si}(\text{n})$ layer was metallized with conventional screen printing and firing through process. (b) FF, (c) V_{oc} , (d) J_{sc} and (e) η of the fabricated solar cell as a function of the front $\mu\text{c-Si}(\text{n})$ thickness.

4.3 TCO and metallization

The objective of this activity is to identify TCOs suitable for high-temperature passivating contacts. Such films should (i) maintain initial surface passivation quality of the passivating contacts, (ii) enable low resistance to charge carrier extraction, (iii) provide thermal stability at high processing temperature and finally (iv) be cost-effective.

4.3.1 Temperature-stable TCOs for high-temperature passivating contacts

Since application on the front side of a solar cell requires high transparency, parasitic absorption in the poly-Si layer needs to be minimized. To this aim we developed doped micro-crystalline ($\mu\text{c-Si}$) layers. However, when integrated in solar cells containing ITO, such transparent contacts suffer from strong sputtering damage (i.e. strong V_{oc} degradation), which could not be recovered at temperatures as the ones typically used for silicon heterojunction cells. Curing at higher temperature ($> 350^\circ\text{C}$) resulted in a partial recovery of the initial (i.e. before metallization) iV_{oc} . Unfortunately, the opto-electrical properties (i.e. transparency and lateral conductivity) of the ITO degrade at such high temperatures.

In CHESS we developed a novel approach for curing of the sputtering damage. Compared to the standard approach illustrated in Figure 7 a, the newly introduced approach shown in Figure 7 b has the benefits of better recovery of sputtering damage, but also of reduced processing complexity and lower material costs (as only 15 nm of ITO are required). Our solution follows a conventional process sequence for the growth of an interfacial SiO_x , the deposition of an *in situ* phosphorous-doped micro-crystalline silicon ($\mu\text{c-Si}(\text{n})$) layer, and annealing at high temperature (850°C). After that, an ITO layer and the silver metallization are deposited for lateral conductivity, only then followed by the deposition of a hydrogen rich silicon nitride ($\text{SiN}_x\text{:H}$) layer on top, which serves as hydrogen (H) reservoir and anti-reflection coating. We then use one single thermal treatment for 30 min in the range $300\text{--}450^\circ\text{C}$ to sinter the screen-printed paste, recover sputtering damage induced by ITO deposition, and diffuse H from the $\text{SiN}_x\text{:H}$ layer towards the c-Si/ SiO_x interface where it passivates interfacial defects. In Figure 7, it clearly



appears that this novel H-through process is leaner than the standard hydrogenation one, since the etching of the $\text{SiN}_x\text{:H}$ layer is no longer necessary.

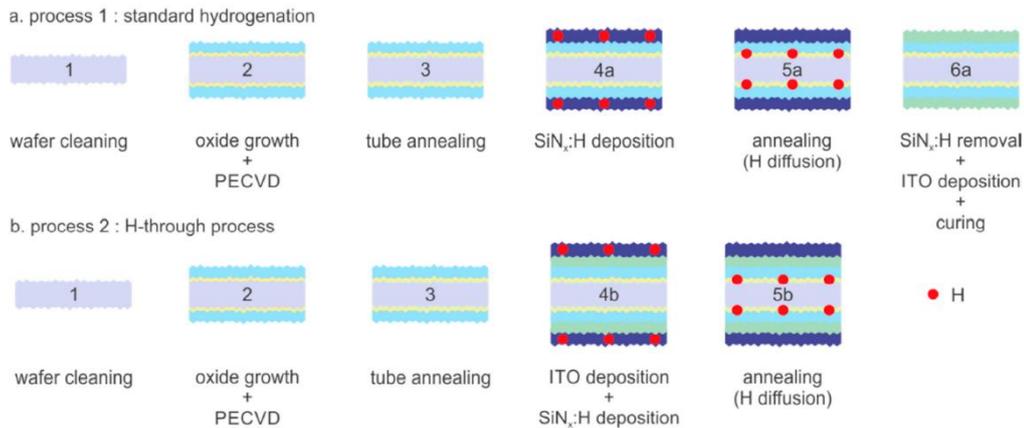


Figure 7: Fabrication sequence of a. the standard hydrogenation process and b. the novel H-through process developed in this project.

To demonstrate the feasibility of the H diffusion through the ITO layer, we prepared symmetrical samples with $\text{SiN}_x\text{:H}/\text{ITO}$ stacks, with variation of the ITO thickness and the annealing temperature. Figure 8 a, b and c show the minority carrier lifetime, iV_{oc} values and recombination current density (J_0) obtained as functions of the ITO thickness at different process steps, respectively. One can observe a loss of passivation (i.e. decrease of lifetime and iV_{oc} and increase of J_0) after ITO deposition, resulting from associated sputtering damage. After annealing at 300°C , the passivation properties were recovered to a similar level than before ITO deposition, indicating an efficient curing of the sputtering damage induced by ITO deposition. From annealing at 350°C , a significant increase of the passivation properties is observed, which likely results from the diffusion of H from the $\text{SiN}_x\text{:H}$ layer toward the $\text{SiO}_x/\text{c-Si}$ interface. One can observe that thinner ITO layers yield higher lifetimes and iV_{oc} values, as they possibly facilitate H diffusion. The highest lifetime of >4.5 ms and iV_{oc} up to 732 mV were reached with a 15 nm-thick ITO film. For the standard hydrogenation sequence, we observe that the J_0 values start increasing between 350 and 400°C (not shown here), which could indicate an easier loss of hydrogen as the samples are no longer capped with $\text{SiN}_x\text{:H}$, thus counteracting the curing of the sputtering damage. We conclude that the H-through process can enable higher passivation either by still ensuring diffusion of H and/or avoiding its effusion out during annealing.

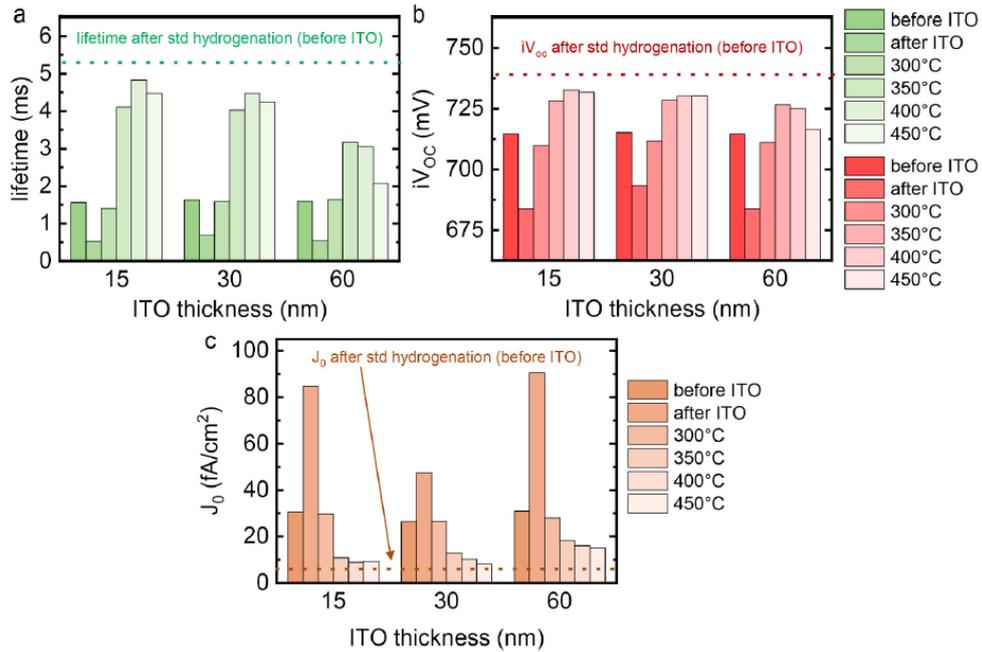


Figure 8: a. Minority carrier lifetime (ms) at injection level of 10^{15} cm^{-3} as a function of the ITO thickness (nm) for H-through process, b. iV_{oc} (mV) deduced from the lifetime as a function of the ITO thickness (nm) for H-through process, c. J_0 (A/cm^2) as a function of the ITO thickness (nm) for H-through process. Samples in a, b and c were annealed in ambient air.

4.4 Tunnelling layer optimization

The tunneling SiO_x is an essential component of all passivating contact technologies developed in this project. In WP4 we investigated several tunneling layers and processes aiming at improving the surface passivation quality without strongly degrading charge carrier transport (material type, density of the material and thickness).

4.4.1 Optimization of SiO_x tunnelling layer grown by ozone oxidation

Here we compare the performance of tunnel oxide fabricated by wet chemical oxidation in HNO_3 or grown by UV-exposure. We report the performed for the FPC approach, but the tests were also performed on other passivating contacts such as the $\mu\text{-Si}(\text{n})$ discussed in WP2. As shown by the iV_{oc} and the photoluminescence (PL) images in Figure 9, the FPC employing the UV- O_3 grown oxide exhibits higher PL signal and iV_{oc} compared to the one with HNO_3 . We measured best ρ_c of 7 and $12 \text{ m}\Omega \cdot \text{cm}^2$ for the HNO_3 and UV- O_3 samples, respectively. Similar results, meaning higher passivation quality and a slight increase in contact resistance were also obtained for other passivating contacts.

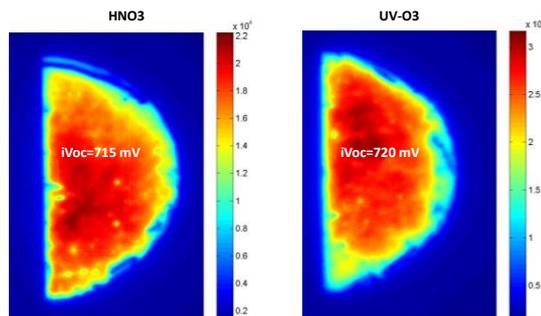


Figure 9: Photoluminescence images of FPC with HNO_3 grown SiO_x (left), and UV- O_3 grown SiO_x (right). The warm colors denote regions of high lifetime. Measured iV_{oc} are also reported.



4.5 Advanced patterned solar cells

Hard mechanical masking was employed to simplify the fabrication process of patterned solar cells. This approach will be used to thicken the passivating contact underneath the metal finger of two-sided contacted cells or to fabricate IBC.

4.5.1 Exploring deposition through mask for simplified patterning process

Masking deposition method is simpler and less costly than structuring with photolithography, but the presence of the mask can modify the plasma during the deposition process. In the first experiments of this activity, we simply deposited n-type SiC_x through a shadow mask and annealed the samples in a tube furnace at 800°C . After annealing at 800°C , the PL image (Figure 9) shows no apparent structure. Whereas, after annealing at 900°C , the passivation of the region covered with SiC_x is worse than in the surrounding area. We explain this finding by the break-up of the interfacial oxide. Overall, the results are consistent with fully covered samples (reported in our previous work [11]). For the sample annealed at 800°C we obtained an iV_{oc} above 710 mV.

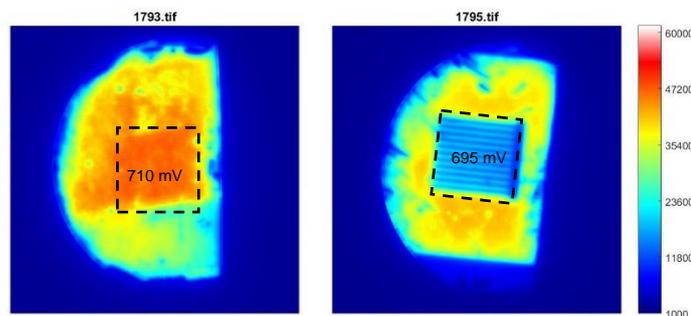


Figure 10: Photoluminescence images of n-type passivating contacts deposited through a shadow mask and annealed for 8 min at 800°C (left), and 900°C (right). The dashed square illustrates the area of the mask, warm colors denote regions of high lifetime.

4.5.2 Hard-masking deposition for two-sides contacted c-Si solar cells with passivating contacts.

In this section, we demonstrate the feasibility of deposition of the $\mu\text{c-Si}(\text{n})$ layer through hard mask. As discussed in WP2, the solar cell efficiency of devices metallized by means of screen printing and firing trough was limited by the strong parasitic absorption in the front side poly-Si. To overcome such limitation, we investigated hard masking deposition to localize the passivating contact under the metallized area. We first investigated different mask opening widths. As shown in Figure 11a, we demonstrated that the deposition rate is directly correlated with the mask opening width i.e. smaller widths require a longer deposition time. The profile shown in Figure 11b shows also a low finger tapering (10-15 nm) which is beneficial to minimize parasitic absorption. Finally, we demonstrated on symmetrical wafer (i.e. thin $\mu\text{c-Si}$ on both sides of the wafer and thick localised $\mu\text{c-Si}(\text{n})$ layer at the front) after hydrogenation by firing of a SiN_x , a promising iV_{oc} of 720 mV. The PL image shown in in Figure 11c exhibits only minor differences between regions featuring thin and thick $\mu\text{c-Si}(\text{n})$ layers, demonstrating the efficiency of the hydrogenation process in both regions.

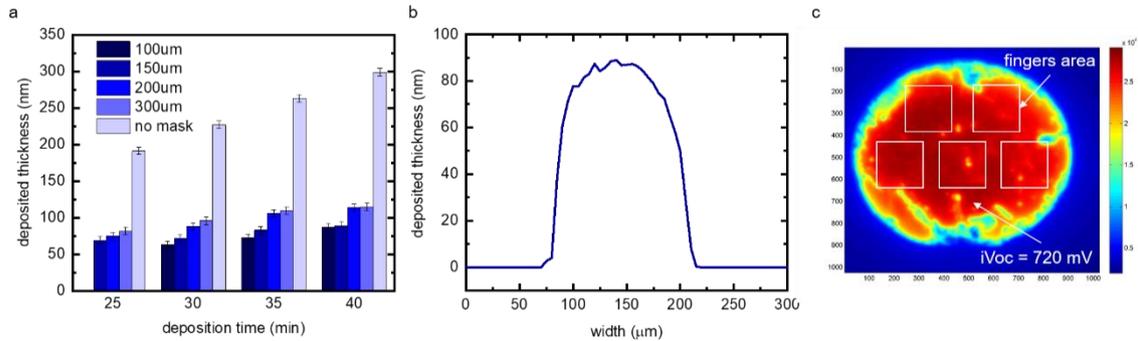


Figure 11: a. deposited thickness of the $\mu\text{-Si(n)}$ layer through different mask opening width b. Raman profilometry of a thick localised $\mu\text{-Si(n)}$ layer deposited through a mask opening width of $100\mu\text{m}$ for 40 min c. PL image of a symmetrical wafer with 5 area of $100\mu\text{m}$ PECVD fingers deposited on one side of the wafer.

Solar cells with passivating contacts were fabricated similarly to the processing sequence described in 4.2.1 for the screen-printed and firing through metallization approach. The only difference was the addition of the hard masking deposition of a thick $\mu\text{-Si(n)}$, resulting in the device sketched in Figure 12. The cell results are shown in the table in Figure 12. A conversion efficiency of $\sim 21\%$ could be achieved with a promising V_{oc} of $\sim 707\text{ mV}$. However, the J_{sc} is still limited to 38.8 mA/cm^2 . We attribute such relatively low value to residual parasitic absorption in the front poly/Si. For this batch of cells a FF of 76.05% was obtained, that was possibly limited due to a small misalignment between the metal print and the $\mu\text{-Si(n)}$ fingers and/or a non-fully optimized firing through process. Further optimization towards reduction of front side parasitic losses and firing through process (e.g. firing temperature, Ag paste) will enable a conversion efficiency above 22%.

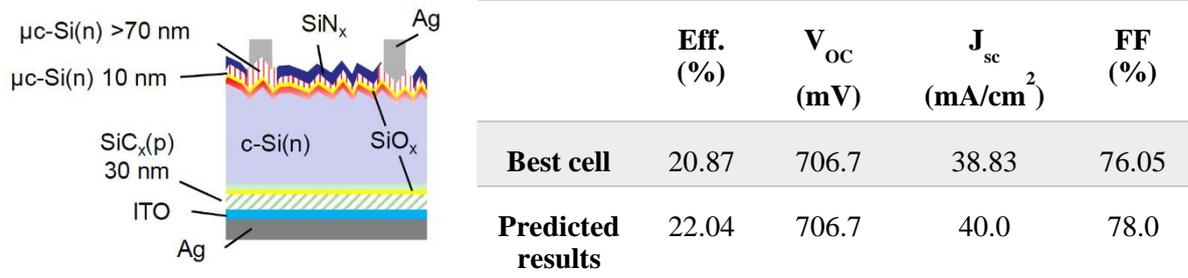


Figure 12. Sketch of the fabricated solar cells with front side localized passivating contacts. The table summarizes the IV parameter of the best device.

4.6 Characterization and understanding

In this section we aim at identifying efficiency losses in solar cells with high-temperature passivating contacts. In addition to that, novel insights on the working principles of high-temperature passivating contacts by using advanced characterization techniques will be provided.

4.6.1 Advanced characterization

Test structures based on symmetrical samples and transfer length method (TLM) were used to determine relevant junction parameters (J_0 value, contact resistivity, sheet resistance, transversal conductivity). Examples of such measurements are reported in Figure 3, Figure 8, Figure 10. ECV and



Secondary Ion Mass Spectrometry (SIMS) measurements were employed to measure the doping profiles of the deposited layers at different processing stages, as shown in Figure 2, Figure 13. SIMS measurements were also performed to assess H evolution during the various fabrication steps of the FPC (Figure 4, left). The obtained results introduce new insights about H-evolution in passivating contacts and its implication on the surface passivation.

In its as-deposited state, the $\text{SiC}_x(\text{p})$ layer shows a large H concentration but a poor passivation quality ($iV_{oc} < 600$ mV). This result is most likely explained by the highly defective nature of the tunnel oxide (before hydrogenation), resulting in Fermi level pinning. Upon firing all hydrogen effuses out of the $\text{SiC}_x(\text{p})$ and surface passivation slightly improves ($iV_{oc} < 675$ mV). After hydrogenation, H accumulates at $\text{SiO}_x/\text{c-Si}$ interface and is also reintroduced in the $\text{SiC}_x(\text{p})$. This event corresponds to a massive increase in iV_{oc} to values above 710 mV.

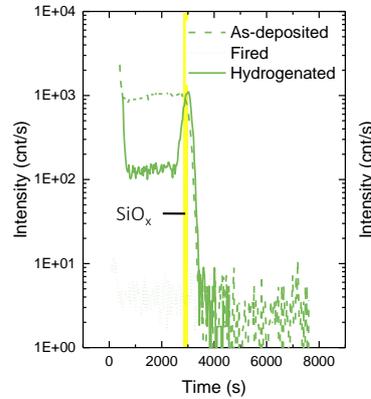


Figure 13: SIMS measurements of the H signal for the FPC in the as-deposited, fired and hydrogenated states.

4.6.2 Understanding of working principles of solar cells with passivating contacts

The prevailing transport mechanism of tunnel-oxide Poly-Si passivating contacts is still under debate; experimental evidence suggests that it could be either due to tunneling through a continuous oxide layer for samples annealed with low thermal budget [12], or to transport through pinholes formed in the oxide for samples annealed at high temperatures [13]. To identify the dominant transport mechanism for the different layer configurations and firing temperatures, we measured $\rho_c(T)$ by means of temperature-dependent TLM. Such technique was already employed to unveil dominant transport mechanism in silicon heterojunction or TOPCon [12]. In this task, we focused on understanding the passivation and transport mechanisms at play in fired passivating contacts (FPC) used as rear p+ passivating contacts in p-type solar cells (presented in part 4.1.2 of this report). The FPC contact was fabricated similarly as described in part 4.1.2, except that we investigated three different configurations of the silicon based layer forming the FPC namely: a- $\text{SiC}_x(\text{p})\text{:H}$, a- $\text{Si}(\text{i})\text{:H}/\text{SiC}_x(\text{p})\text{:H}$ and a highly-doped a- $\text{SiC}_x(\text{p})\text{:H}$ (HD- $\text{SiC}_x(\text{p})$). The firing temperature (T_{firing}) was also varied in the range 770-830°C. Subsequently to this first firing performed to activate the FPC, all samples were coated with an $\text{SiN}_x\text{:H}$ layer and fired on a belt furnace at nominal peak temperature of 830°C to promote interface hydrogenation. Firstly, the iV_{oc} and ρ_c relative to the three different FPC configurations were investigated, results are illustrated in Figure 14. Figure 14 a shows a clear increase in iV_{oc} when T_{firing} is raised from 770°C to 800°C and a slight decrease for $T_{firing} = 830^\circ\text{C}$ for all three configurations. The highest iV_{oc} of 722 mV was reached for the $\text{Si}(\text{i})/\text{SiC}_x(\text{p})$ stack fired at 800°C, corresponding to J_0 of ~ 7 fA/cm². As shown in Figure 14 b, for all FPC configurations a massive drop in ρ_c , from >1000 m $\Omega\cdot\text{cm}^2$ to <80 m $\Omega\cdot\text{cm}^2$, was observed when increasing T_{firing} from 770°C to 800°C. A further increase in T_{firing} to 830°C leaves ρ_c almost unchanged. We note that for all FPC configurations, $T_{firing} \geq 800^\circ\text{C}$ enables ρ_c below 80 m $\Omega\cdot\text{cm}^2$, which is not FF limiting for



full area contacts. The observed iV_{OC} and ρ_c behaviors as functions of T_{firing} are possibly explained by three mechanisms: oxide reconstruction, doping activation and oxide degradation due to diffusion of impurities (e.g. B or C) occurring towards higher T_{firing} . Indeed, the increase in iV_{OC} and the decrease in ρ_c when increasing T_{firing} from 770 to 800°C is possibly explained by reconstruction of O atoms forming Si–O bonds leading to a more stoichiometric SiO_x [6], [8] and doping activation in the $SiC_x(p)$ promoting accumulation of holes underneath the SiO_x [9]. At firing temperatures of 830°C, those beneficial effects may be counterbalanced by diffusion of B or C from the $SiC_x(p)$ into the SiO_x , that are responsible for creating additional interfacial defects [10], resulting in a drop of the iV_{OC} (see Figure 15 (a)).

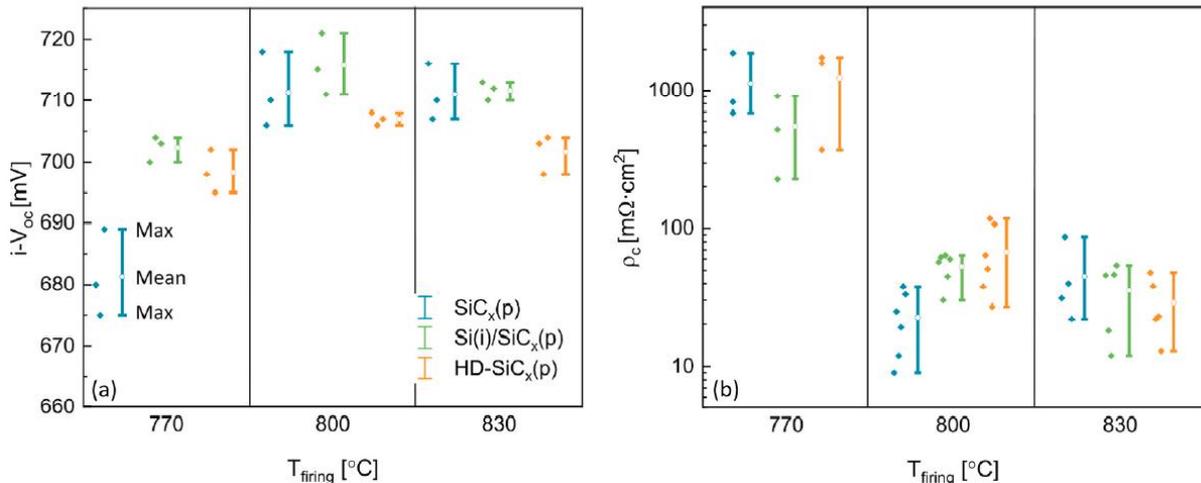


Figure 14: (a) iV_{OC} and (b) ρ_c as functions of T_{firing} and for three FPC configurations ($SiC_x(p)$, $Si(i)/SiC_x(p)$ and HD- $SiC_x(p)$). The maximum and minimum values are shown at the end of the whiskers. The open circles represent the mean values. The diamonds represent the data points.

Raman measurements were performed to evaluate the impact of the layer crystallinity on the FPC junction quality (i.e. surface passivation and charge carrier extraction). The results illustrated in Figure 15 (a)-(c) indicate a sharp increase in crystallinity, especially for the $SiC_x(p)$ and $Si(i)/SiC_x(p)$ configurations, when T_{firing} is raised from 770 to 800°C. This firing was performed in a cold-wall RTP system which measures the wafer temperature during the firing process. All samples were measured after hydrogenation obtained by SiN_x deposition and firing on a belt furnace at 830°C. Therefore, the hydrogenation firing occurs at $T \sim 770$ °C, thus leaving unaffected the micro-structural layer properties which were set by the first firing. To be noted that this is the air temperature which is typically 50°C higher than the wafer temperature. For the $SiC_x(p)$ and a- $Si(i)/SiC_x(p)$ a further increase of the firing temperature to 830°C affects the crystallinity only marginally. Interestingly, the HD- $SiC_x(p)$ shows a much weaker tendency towards crystallization, even for $T_{firing} = 830$ °C. The explanation for this behavior is twofold: first, dopant incorporation causes high levels of disorder in the small host crystallites reducing their ability to crystallize at a given temperature; second, the trimethylboron (TMB) is a C-containing gas and C incorporation within the Si-network is known to retard crystallization [11].

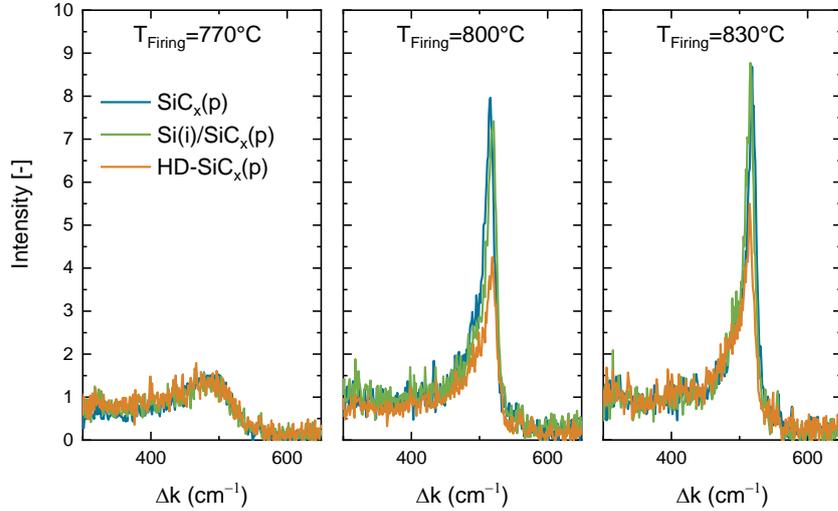


Figure 15: Raman signal of the three FPC configurations namely $\text{SiC}_x(\text{p})$, $\text{Si}(\text{i})/\text{SiC}_x(\text{p})$ and $\text{HD-SiC}_x(\text{p})$ fired at temperatures of 770, 800 or 830°C.

For the samples fired at 770°C, regardless of the FPC configuration, a strong decrease of the contact resistance was observed towards higher temperatures of the cell (Figure 16 (a)). On the contrary, Figure 16 (b) shows a T -independent $\rho_c(T)$ for the $\text{SiC}_x(\text{p})$ and $\text{Si}(\text{i})/\text{SiC}_x(\text{p})$ whereas the one of the $\text{HD-SiC}_x(\text{p})$ shows a slight decrease towards higher temperatures. All three configurations exhibit a T -constant behavior of $\rho_c(T)$ when fired at 830°C, Figure 16 (c). These results suggest T -independent tunneling is the dominant transport mechanism in $\text{SiC}_x(\text{p})$ and $\text{Si}(\text{i})/\text{SiC}_x(\text{p})$ stacks, for $T_{\text{firing}} \geq 800^\circ\text{C}$. On the contrary, charge carrier transport is a combination between direct tunneling and thermionic emission through a barrier for all samples fired at 770°C and for the $\text{HD-SiC}_x(\text{p})$ fired at 800°C. Such barrier can be present either at $\text{c-Si}(\text{p})/\text{SiO}_x/\text{SiC}_x(\text{p})$ or $\text{SiC}_x(\text{p})/\text{ITO}$ interface. Indeed, the tunneling probability of holes through a thin SiO_x (<1.5 nm) strongly relies on the alignment of the valence band edges between the $\text{SiC}_x(\text{p})$ and the $\text{c-Si}(\text{p})$ [14]. As the samples fired at 770°C and $\text{HD-SiC}_x(\text{p})$ fired at 800°C are expected to have a lower concentration of electrically active B (being more amorphous, see Figure 15), and consequently the effective barrier height/depth becomes larger thus reducing the hole tunneling probability through the SiO_x . The barrier at $\text{SiC}_x(\text{p})/\text{TCO}$ is the result of a downward band-bending that is caused by Fermi level pinning or by the work function of the ITO. Assuming Fermi level pinning between the $\text{SiC}_x(\text{p})$ and the ITO, as this is typical for metal/semiconductor interfaces, the barrier height does not depend much on the doping concentration within the semiconductor but rather on the interface defect type and density. On the contrary, its barrier width (i.e. depletion width) is doping dependent [15]. In particular, the higher the doping concentration in the Si-doped layer the narrower the barrier width becomes. Our observations indicate that increasing layer crystallinity and thus the amount of electrically active dopants, makes tunneling at both SiO_x and the $\text{SiC}_x(\text{p})/\text{ITO}$ interface to be the dominant transport mechanism in FPC.

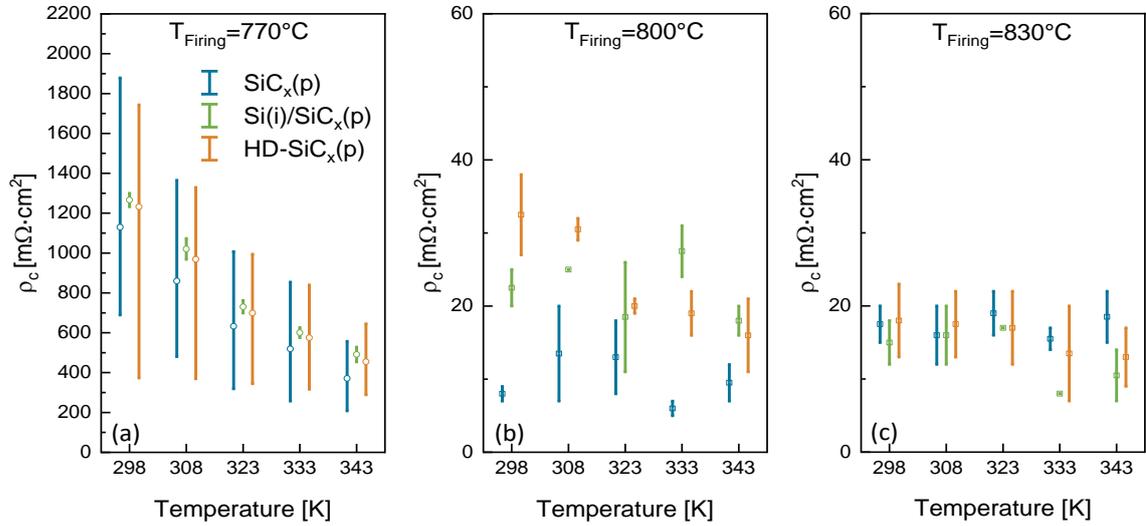


Figure 16: Measured contact resistance as a function of the substrate temperature. The different three FPCs are fired at (a) 770°C, (b) 800°C and (c) 830°C. The maximum and minimum values are shown at the end of the whiskers. The open squared symbols represent the mean values.

Finally, temperature dependent J-V measurements, between -100°C and $+80^\circ\text{C}$, were performed in order to unveil possible differences in the transport mechanisms for the different FPC configurations in finished solar cells. The Si(i)/SiC_x(p) and the HD-SiC_x(p) were chosen for this study. Strikingly, despite the similar FF values measured at STC, the temperature dependence of their respective FF is remarkably different. As shown in Figure 17 (a), $FF(T)$ of the device with the Si(i)/SiC_x(p) linearly increases with decreasing T_{meas} reaching a value of 87% at -100°C . On the contrary, the FF of the cell with the HD-SiC_x(p) shows a saturation and a roll-off for T_{meas} below -50°C . This further proves that for the HD-SiC_x(p) charge carrier extraction is a combination between thermionic field emission (TFE) and pure field emission (FE). The latter is completely suppressed for the Si(i)/SiC_x(p) solar cell thanks to the larger number of active dopants. By fitting of the FF trends according to the equations in Ref. [12], we were able to extract the height of the energy barrier. A small activation energy (E_a) of ~ 30 meV was obtained for the solar cell with the Si(i)/SiC_x(p) whereas the one employing the HD-SiC_x(p) had an E_a of ~ 90 meV. Both cells showed an increase of $V_{oc}(T)$ towards lower temperature, which is explained by the direct T -dependence of the intrinsic carrier concentration, as shown in Figure 17 (b). In summary, the impressive performance of our solar cells with partially crystalline FPC layers confirms that it is possible to suppress possible transport barriers at both c-Si and TCO interfaces, as sketched in Figure 17 (c). This can be achieved by tuning the dopant flow and firing temperature of the FPC in order to obtain highly-crystalline layers. In conclusion our advanced set of characterization and modelling provides guidelines on the design and transport mechanisms associated to FPC contacts.

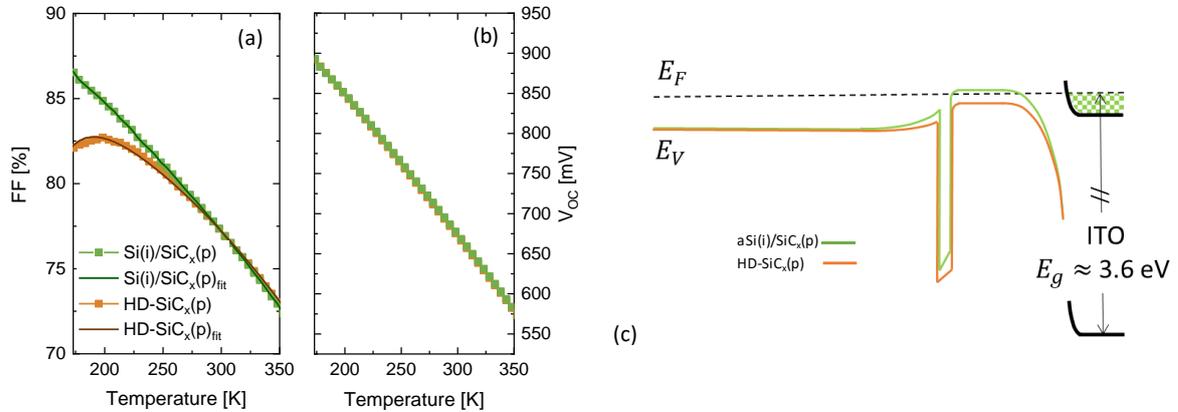


Figure 17: a) FF and (b) V_{oc} plotted over temperature. The solar cells featured the Si(i)/SiC_x(p) or the HD-SiC_x(p) as rear side passivating contact fired at 800°C. The dashed lines were calculated using a temperature-independent series resistance. The solid lines were calculated according to the equations reported in Ref. 12. (c) Electronic band structure of the c-Si/SiC(p)/ITO stack with the energy levels corresponding to the valence band (E_V) and the Fermi level (E_F). The sketch is for illustrative purposes.

Other powerful tools that we used to conduct material science with CHESSE, are scanning electron microscope (SEM) and transmission electron microscopy (TEM). Both techniques were used along the whole project duration. Here we report few examples. SEM were used mainly to characterize layer thickness and coverage factor. Figure 18 shows the SEM for a $\mu\text{c-Si(n)}$ layer when deposited, for the same time, (a) without masking and (b) with hard masking (as in Section 4.5.3). From the figures we estimated a scaling factor of ~ 3 time in layer thickness when hard masking is employed with respect to full-area deposition.

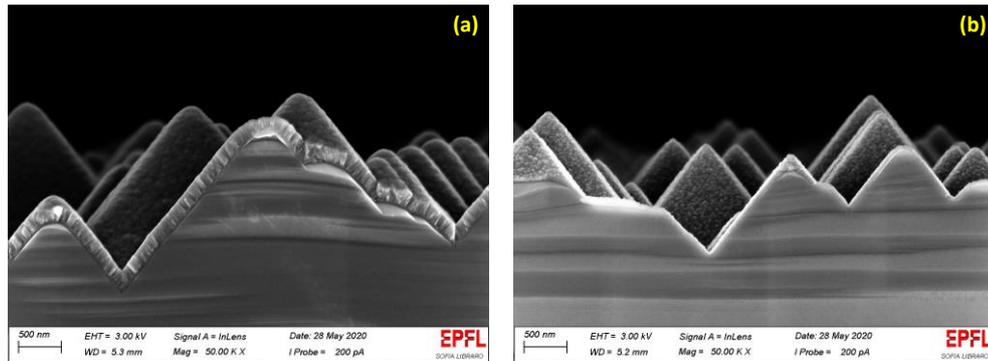


Figure 18: (a) $\mu\text{c-Si(n)}$ layer deposited over full-area. (b) $\mu\text{c-Si(n)}$ layer deposited through-hard mask. For both cases we used the same deposition time.

5 Conclusions and outlook

In conclusion, within CHESSE we could successfully demonstrate and introduce several breakthrough technologies to the field of photovoltaics and specifically passivating contacts. Despite the COVID-19 pandemic that delayed some of our activities we could reach most of the targeted objectives. We could successfully demonstrate the integration of passivating contacts as PERC upgrade. We obtained conversion efficiencies up to 22.5%, which was 0.5% below our final target. An alternative metallization



process and its integration in co-annealed high-efficiency c-Si solar cells with front and rear side passivating contacts was demonstrated. We also introduced a novel approach for eliminating sputtering damage, simplify process integration and reduce material costs, consisting in hydrogenation through a TCO layer. With this we demonstrated record conversion efficiency, for p-type c-Si solar cells with two sides passivating contacts, up to 22.8%. This was evaluated amongst the best 10 abstracts at the SiliconPV 2020 conference. Despite the good result, we still have work to reach our target 24%. The small number of processed samples and the lab closure during COVID explains the gap in large part. We also fabricated co-annealed solar cells with passivating contacts metallized by screen printing and firing through. We showed that 120 nm thick layers are required to reach cell V_{OC} above 700 mV. We demonstrated the use of alternative processes for the formation of the tunnel oxide. In particular, UV- O_3 grown oxide allows better passivation compared to the standard wet chemically grown oxide (HNO_3) without hindering charge carrier extraction. The validity of hard-masking deposition to form localized passivating contacts for two-sides contacted and IBC solar cells was explored. For two-sides contacted c-Si solar cells with localized passivating contacts were able to reach conversion efficiency of ~20.9% and indicated a clear path towards samples with efficiency over 23%. The achievement of this efficiency target with the proposed approach, would enable a broader adoption of polysilicon based passivating contacts in the solar cell industry. From a more scientific point of view, in WP6, advanced characterization techniques (SIMS, Raman, ECV, SEM, TEM...) were employed during the project duration to better understand the working principles of passivating contacts. In particular, we showed, by SIMS that the hydrogenation process introduces H within the passivating contacts and more specifically at the SiO_x/c -Si interface. Moreover, we demonstrated that the layer crystallinity fraction plays an important role on the junction quality and determines the dominant charge carrier transport mechanism. This work was also evaluated amongst the best 10 abstracts at the SiliconPV 2020 conference. The results generated within CHESS in terms of process integration, junction quality (i.e. surface passivation and contact resistance), and understanding pave the way for >24% conversion devices that are compatible with current industrial process. This would enable a broader adoption of this technology at industrial scale that will contribute to make PV more affordable by further reducing costs per area.

6 Publications

6.1 Oral presentations

- Nogay_2018ipvc Fluorinated Boron Doped Passivating Contact for Silicon Solar Cells
G. Nogay, E. Rucavado, Q. Jeangros, S. Eswara, J. Stuckelberger, P. Wyss, M. Morales, A. Ingenito, F.-J. Haug, P. Löper, C. Ballif
Extended Oral Presentation at the 45th IEEE PVSC, Hawaii
Student Award Winner
- Ingenito_2018ipvc Strategies for integration of passivating contacts in existing production lines
A. Ingenito, P. Wyss, G. Nogay, J. Stüchelberger, C. Allebé, J. Horzel, M. Despeisse, F.-J. Haug, P. Löper, C. Ballif
Oral Presentation at the 45th IEEE PVSC, Hawaii
- Haug_2018epvsec SiCx- and SiOx-based passivating contacts for high-efficiency silicon solar cells,
F.-J. Haug, J. Stuckelberger, G. Nogay, P. Wyss, M. Lehmann, L. Gnocchi, C. Allebé, J. Horzel, M. Despeisse, A. Ingenito, C. Ballif
Oral Presentation at the 35th EU-PVSEC, Brussels



- Stückelberger_2018epvsec Transparent passivating contacts for front side application
J. Stückelberger, G. Nogay, P. Wyss, L. Gnocchi, M. Lehmann, J. Diaz Leon, L. Ding, J. Horzel, C. Allebé, M. Despeisse, F.-J. Haug, A. Ingenito, C. Ballif
Oral Presentation at the 35th EU-PVSEC, Brussels
- Ingenito_2018mrs Integration strategies of high temperature passivating contacts
A. Ingenito, G. Nogay, C. Allebé, J. Stückelberger, P. Wyss, J. Horzel, F. Sahli, J. Werner, L. Ding, J. Diaz Leon, F. Meyer, M. Lehmann, A. Savoy, S. Eswara, T. Wirtz, S. Nicolay, Q. Jeangros, M. Despeisse, F.-J. Haug, C. Ballif
Invited Oral Presentation at the MRS Fall, Boston
- Ingenito_2019 Implementation and Characterization of Tunnel-Oxide Passivating Contacts for Single Junction c-Si and Perovskite/c-Si Tandem Solar Cells A. Ingenito, F. Mayer, P. Wyss, C. Allebé, J. Diaz Leon, A. Savoy, F. Sahli, M. Lehmann, Q. Jeangros, M. Despeisse, S. Nicolay, F.-J. Haug, C. Ballif, 36th EUPVSEC, 2019
- Haug_2019 SiCx- and SiOx-based passivating contact for silicon solar cells. F.-J. Haug, M. Lehmann, F. Meyer, P. Wyss, C. Allebé, M. Despeisse, A. Ingenito, C. Ballif, 9th SiPV, 2019.
- Ingenito_2019 Passivating contacts activities at pvlab and csem in Neuchâtel A. Ingenito, F. Mayer, P. Wyss, A. Savoy, C. Allebé, L. Senaud, P.-S. Bertrand, G. Nogay, J. Stückelberger, F. Sahli, J. Werner, J. Diaz Leon, M. Lehmann, S. Nicolay, Q. Jeangros, M. Despeisse, F.-J. Haug, C. Ballif. 17e Congrès photovoltaïque national (2019).
- Meyer_2020 Optimization of front SiNx/ITO stacks for high-efficiency two-side contacted c-Si solar cells with co-annealed front and rear passivating contacts Meyer F., Savoy A., Diaz J., Persoz M., Niquille X., Allebé C., Nicolay S., Haug F.-J., Ingenito A., Ballif C. 10th SiPV 2020, **best 10 abstracts**.
- Libraro_2020 Formation of p-type passivating contacts by short annealing S. Libraro, F.-J. Haug, J. Díaz León, C. Allebé, S. Nicolay, A. Ingenito, C. Ballif. 37th EUPVSEC (2020)
- P.Wyss_2020 Firing-through metallisation of PERT-like cells using uc-Si(n) as rear side full area passivating contact P. Wyss, A. Ingenito, Q. Jeangros, J. J. Diaz, C. Allebé, S. Nicolay, F.-J. Haug, C. Ballif. 37th EUPVSEC (2020)

6.2 Peer-reviewed articles

- Ingenito_2018ne A passivating contact for silicon solar cells formed during a single firing thermal annealing
A. Ingenito, G. Nogay, Q. Jeangros, E. Rucavado, C. Allebé, S. Eswara, N. Valle, T. Wirtz, J. Horzel, T. Koida, M. Morales-Masis, M. Despeisse, F.-J. Haug, P. Löper, C. Ballif
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