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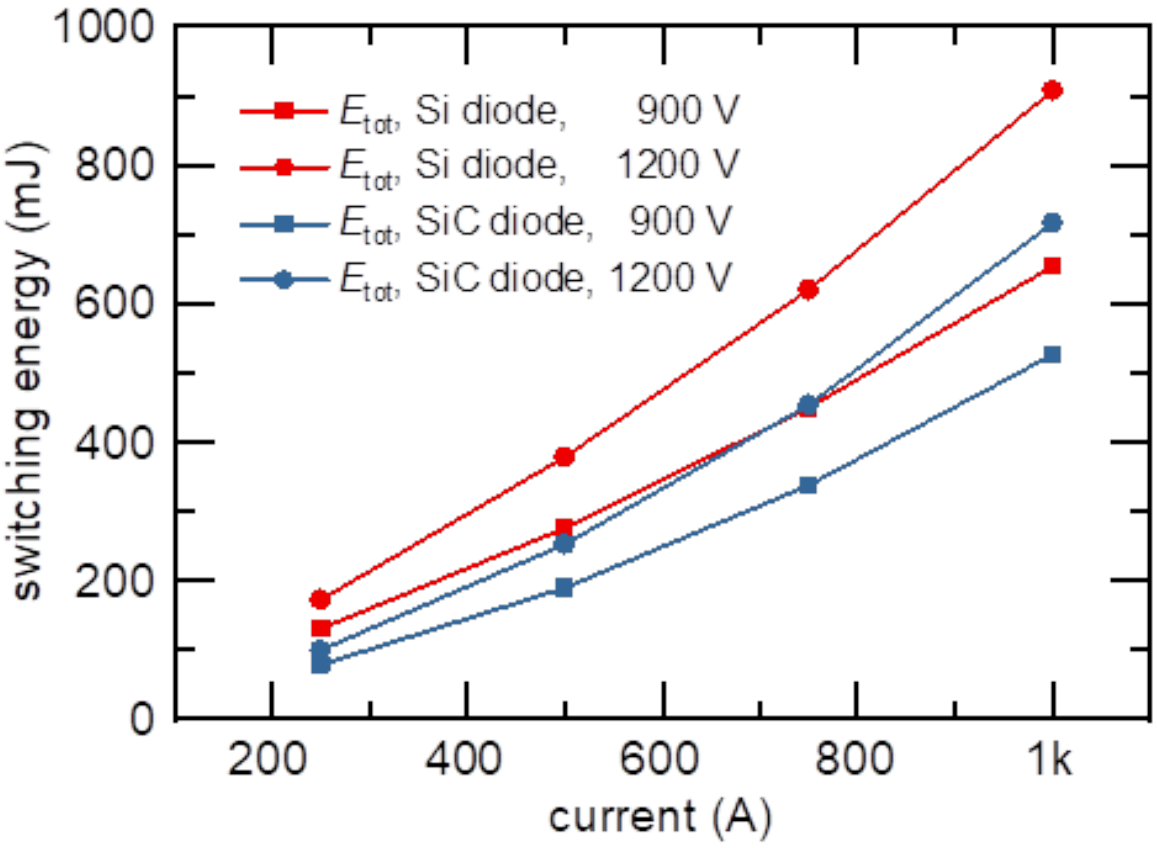
Swiss Federal Office of Energy SFOE
Energy Research and Cleantech

Final report

1500-SIC

Development of a new photovoltaic inverter with silicon carbide (SiC) technology for full power operation at 1500V



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Publisher:
Swiss Federal Office of Energy SFOE
CH-3003 Bern
www.bfe.admin.ch
energieforschung@bfe.admin.ch

Agent:
ETH Zurich
Advanced Power Semiconductor Laboratory
Physikstrasse 3
CH-8092 Zurich
www.aps.ee.ethz.ch

Author:
Ulrike Grossner, APS, ulrike.grossner@ethz.ch

SFOE P+D: Karin Söderström, karin.soederstroem@bfe.admin.ch.
SFOE PV research: Stefan Oberholzer, stefan.oberholzer@bfe.admin.ch.

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Summary

Photovoltaic (PV) energy is experiencing significant cost reduction over the last years. Lately, the bias voltage of photovoltaic panels has risen from 1000V to 1500V, leading to a significant reduction of the Balance of Plant cost. To improve the Levelized Cost of Energy, manufacturers are increasing the installed DC power of PV panels for a given nominal AC power of the inverter (so-called capacity factor) from 1.2–1.3 to higher values. This results in a larger voltage at the maximum power point of the PV panel. Consequently, conventional power electronics solutions rated at 1700V maximum voltage are not suitable as they are typically designed for a nominal power below approximately 1300V. Increasing the capacity factor leads to higher maximum power point voltage. Therefore, new solutions are required to deliver rated power near 1500V. The project «1500-SIC» delivered a solution incorporating a new 1700V-rated silicon carbide (SiC) diode, tested for operation at full power of a 1500V inverter. This document is a final report, focusing primarily on the newly established competencies within Switzerland.

Zusammenfassung

Energie aus Photovoltaik erfährt derzeit eine signifikante Kostenreduktion. Um mit dem Preisverfall der Solarmodule und auch deren technischer Weiterentwicklung Schritt zu halten, wird der Spannungsstrang auf immer höhere Spannungen gesetzt: eine Steigerung von 1000V auf 1500V führt zu einer wesentlichen Verringerung der Anlagenkosten. Um die Levelized Cost of Energy zu verbessern, werden immer höhere Gleichstromleistungen der Solarmodule an die Wechselstrominverter angeschlossen und damit der sogenannte capacity factor der Anlage von 1.2–1.3 auf höhere Werte gebracht. Daraus resultiert eine höhere Spannung am Punkt der höchsten Leistung des Solarmoduls. In Konsequenz können keine herkömmlichen 1700V-Leistungselektronik-Systeme verwendet werden, da diese für eine Spannung von 1300V ausgelegt sind. Aus diesem Grund müssen neue Lösungen für eine Benutzung bei 1500V Spannung entwickelt werden. Das Projekt “1500V-SIC” liefert solch eine neue Lösung durch die Verwendung einer neuartigen 1700V Siliziumkarbiddiode und einer Anpassung des Gesamtsystems auf diese neue Bauelementtechnologie. Die neue Inverter-Anlage wurde für eine volle Auslastung bei 1500V getestet. Dieses Dokument stellt den Schlussbericht des Projekts dar und fokussiert mehrheitlich auf die in der Schweiz neu etablierten Test- und Simulationsmethoden und die dazu erstellten Anlagen.

Résumée

L'énergie photovoltaïque connaît actuellement une réduction de coût importante. Afin de suivre la baisse du prix des modules solaires et aussi leur développement technique, la chaîne de tension est réglée sur des tensions toujours plus élevées : une augmentation de 1000V à 1500V entraîne une réduction significative des coûts du système. Afin d'améliorer le coût de l'énergie, des puissances de courant continu de plus en plus élevées des modules solaires sont connectées aux onduleurs à courant alternatif et ainsi le facteur de capacité du système passe de 1,2-1,3 à des valeurs plus élevées. Il en résulte une tension plus élevée au point de la puissance la plus élevée du module solaire. Par conséquent, les systèmes électroniques de puissance conventionnels de 1700V ne peuvent pas être utilisés, car ils sont conçus pour une tension de 1300V. C'est pourquoi de nouvelles solutions doivent être développées pour une utilisation à une tension de 1500V. Le projet "1500V-SIC" apporte une telle solution en utilisant une nouvelle diode au carbure de silicium de 1700V et en adaptant l'ensemble du système à cette nouvelle technologie. Le nouveau système d'onduleur a été testé pour une pleine charge à 1500V. Ce document est le rapport final du projet et se concentre principalement sur les nouvelles méthodes de test et de simulation établies en Suisse et sur les équipements créés à cet effet.

Main findings

- Silicon carbide (SiC) diodes replacing silicon (Si) diodes in high power modules lead to a reduction of switching losses of 21 to 42%, depending on the current.
- SiC diodes may reach failure in time (FIT) rates comparable to that of Si diodes.
- Increasing the power density of the inverter by 8 % with a 10 %-reduction in costs per kW ratio is possible.

Contents

Abbreviations

SFOE	Swiss Federal Office of Energy
AC	Alternating Current
APS	Advanced Power Semiconductor Laboratory, ETH Zurich
BRNC	Binning-Rohrer Nanotechnology Center (shared cleanroom between ETH Zurich and IBM Research)
ChipIr	Neutron Testing Facility at ISIS, UK
DAQ	Data Acquisition (system)
DC	Direct Current
DLTS	Deep Level Transient Spectroscopy
DPT	Dual-Source Double Pulse Tester
EM	electromagnetic
Empa	Swiss Federal Laboratories for Materials Science and Technology
FEA	Finite Element Analysis
FIT	Failure in Time
HF	high frequency
IEA 4E TCP	IEA Technology Collaboration Program of Energy Efficient End-Use Equipment
IGBT	Integrated Gate Bipolar Transistor
KPI	Key Performance Indicator
LCOE	Levelized Cost of Energy
LF	low frequency
MOSFET	Metal oxide semiconductor field effect transistor
PCB	Printed Circuit Board
PECTA	Power Electronic Conversion Technology Annex
PIF	Proton Irradiation Facility
PSI	Paul Scherrer Institut
PSU	Power Supply Unit
PV	Photovoltaic
SEB	Single-Event Burnout
SELC	Single Event Leakage Current
SiC	Silicon carbide
TAS	Thermal Admittance Spectroscopy
WBG	wide band gap

1 Introduction

1.1 Background information and current situation

The project «1500-SIC» was executed in the framework of a European call SOLAR-ERA.NET Cofund action that brings together national European organisations owning and/or managing major solar power research and innovation programmes throughout Europe, funding projects typically involving academic and industrial partners active in photovoltaic technology (PV). The «1500-SIC» project consortium consists of the company Gamesa Electric from Spain, a worldwide supplier of PV inverters; Infineon Technologies Austria, a worldwide supplier of semiconductors for power electronics and the Swiss, purely academic partner, the Advanced Power Semiconductor Laboratory (APS) at ETH Zurich. To optimally use the cofund action, the contract between SFOE and APS goes beyond the actual technical goals of the 1500-SIC project by targeting the establishment of APS as a national competence centre for power semiconductors in Switzerland.

1.2 Purpose of the project

Photovoltaics is a technology of vital importance for current and future electric grid solutions. Whereas there is a lot of knowledge and expertise already available on photovoltaic cells and modules, the actual connection of such technology to the grid requires the use of power electronic devices in inverter systems.

The levelized cost of energy (LCOE) of PV are largely driven by the system costs. Therefore, the established standard for direct current (DC) voltages in utility-scale systems is nowadays at 1500 V. Such a high operation voltage requires the same low failure rates and high efficiency for the power electronics as lower-voltage systems. However, as the voltage increases, and the systems are being operated at elevations of 3'000 m, the semiconductor devices need to be tested for their ruggedness against cosmic radiation.In the recent years, it has been shown that the incorporation of silicon carbide (SiC) is highly beneficial for reduction of losses incurred during operation of a solar inverter. The material exhibits a higher critical electric field, allowing a unipolar operation with fast charge carriers also at comparably high system voltages. The overall prospect of SiC (and other wide band gap (WBG) semiconductors) for application has been extensively outlined in the first phase of the Power Electronic Conversion Technology Annex (PECTA) within the IEA 4E TCP (Technology Collaboration Program of Energy Efficient End-Use Equipment)[1].APS is a laboratory still in the start-up phase, and its major scientific topics of power semiconductor materials and devices, their characterization and ruggedness and reliability testing is of high importance to ensure a reliable design and dimensioning of power semiconductor devices to be used in PV-enabling power electronics systems. The SFOE project is strengthening the start-up phase of APS with the clear goal to enable future projects with Swiss industrial partners.Objectives

For APS, the following SCIENTIFIC AND TECHNOLOGICAL OBJECTIVES can be deducted from the consortium agreement (see also Transnational Project Progress Report as attached to this document):

- **Increase PV conversion efficiency** by the usage of a new SiC diode technology for application in the inverter described in objective (1) of the overall consortium project. The key performance indicator (KPI) is an improvement of inverter energy efficiency:

  APS contributed through characterization of both diodes as well as power modules with the SiC diodes.

- **Cosmic ray performance**. Assuring a low Failure in Time (FIT) value for this operation voltage is a key objective for the project. The KPI is an understanding of the influence of cosmic ray failures

[1] "Wide Band Gap Technology: Efficiency Potential and Application Readiness Map", https://pecta.iea-4e.org/files/other-files/0000/0186/PECTA_Report_Total-V10final-May-2020.pdf

on the FIT rates of the inverter, including root-cause analysis. Typically, the failure due to cosmic ray can be described by a charge accumulation leading to catastrophic failure.

APS contributed by establishing the FIT value for the new diode technology and the understanding of the failure mode under radiation.

- **Full power test bench:** To validate the improvements described above, a full power test bench with capabilities of testing central inverters up to 3MW with DC voltages up to 1500V will be developed. The KPI is the availability of the test bench before the test campaign starts.

  APS contributed through switching performance measurements on the power module level in order to enabling the dimensioning of the overall system.

Specifically, APS was building up a variety of testing setups as well as routines, for the testing and characterization of individual semiconductor devices as well as of entire power modules. There is also emphasis on establishing correct modelling procedures to enable virtual prototyping 80 power modules in the future (beyond the scope of this project).

2 Description of facility

As further discussed below, there is a variety of testing possibilities to investigate failure modes of power devices and the base semiconductor material due to irradiation (cosmic radiation). Testing for these two different types of semiconductor dies (the simple diode-type test structure for the base material and the fully processed power diode) differs in the mounting and electrical connection during the test. While power semiconductor devices are often tested in an active mode (applied voltage with a recording of a leakage current or a resistance), simple test structures and the semiconductor material itself are typically tested “passively”, i.e. without any applied voltage. Consequently, also the subsequent characterization of the irradiated samples differs. Power devices are characterized using parameter analyzers and custom-made test setups for static and dynamic performance values. Semiconductors, on the other hand, are tested for electrical properties, such as carrier concentration and electrically active defects.

The following testing capabilities are established and are made available for testing of irradiated samples in a dedicated test facility through this project:

- A probe station equipped with a thermal chuck with a diameter of 75 mm, connected to a Keithley Parametric Curve Tracer 2600-PCT-4B in combination with other measurement equipment for characterization of semiconductor test structures and fully processed power semiconductor dies.
- A test box comprising of a fixture and the required cabling to be connected to the curve tracer for characterization of packaged semiconductor devices. At the moment, type TO247-3L and TO247-4L compatible fixtures are available.
- A modular custom-made test stand with the following capabilities:
  - A dual-source double pulse tester (DPT) able to automatically measure losses for any current power semiconductor device, with a wide range of current and voltage. Due to the dual source topology, the system energy is minimized and voltage and current can be selected freely in any combination up to 2000 V and 2000 A. This tester has been successfully implemented for both discrete devices (type TO247-3L and TO247-4L) and larger power modules.
  - A Short circuit and an avalanche tester; ruggedness under extreme conditions such as short circuit and avalanche breakdown is important for many applications of power semiconductors.

- A measurement system capable of Deep Level Transient Spectroscopy (DLTS), the HERA-DLTS system, which can also be used to perform Thermal Admittance Spectroscopy (TAS) measurements, allows temperature scans in the range from 20 K to 800 K. The minimum pulse width is limited to 1 µs at ± 100 V and 20 ns at ± 10 V pulse voltage. In addition, a photo diode allows optical stimulation. The specimen is limited to 20 x 20 mm^2 with contacts of radii larger than 280 µm.

In order to further expand the simulation and modeling capabilities, the following activities were perfomed:

- The analysis of the existing modelling tools and methods for modeling of power semiconductor devices and their packages increasing the understanding of the state-of-the-art limits with respect to modeling accuracy and computational complexity is targeted.
- The APS Lab has been developing own modelling tools taking advantage of specialized numerical methods, which allow a simultaneous control of accuracy and computational cost. Most of the effort is directed towards efficient automated system design procedures for finding optimal design solutions at minimal costs by considering dominant multi-physics design aspects. An ETH thermal modeling tool for analyzing thermal aspects of power semiconductor packages has been further developed, tuning its capabilities for modeling WBG power semiconductor packages operating at higher temperatures.

3 Procedures and methodology

3.1 Radiation Hardness

SiC device technology has become a viable alternative to silicon based power devices for high-efficiency and high-power density applications in extreme environments, including space, avionic and particle accelerator industries. However, like their silicon counterparts, SiC devices are known to be susceptible to destructive Single Event Burnout (SEB). Examples of possible causes include high-energy neutrons produced from the interaction between cosmic rays and the terrestrial atmosphere, protons in high energy accelerators and heavy-ion environment encountered in space.

Additionally, in the case of heavy-ions, a unique signature is observed in SiC Metal oxide semiconductor field effect transistors (MOSFETs) and it is referred to as Single Event Leakage Current (SELC). Single ions can cause permanent degradation that leads to a gradually increased leakage in both drain and gate current with increasing heavy-ion fluence. This damage is not catastrophic, but the device operation may be altered, which complicates the assessment of radiation tolerance in these parts.

For the SiC diodes considered within this project, radiation experiments were performed at different European facilities (i.e., ChipIr for terrestrial neutrons, PSI for 200 MeV protons).

Testing was performed as an active test, monitoring the breakdown voltage. Printed Circuit Boards (PCBs) for up to 30 diodes, thereof 5 boards á 20 diodes for neutrons and 4 boards á 10 diodes for protons have been used. The diodes were soldered and wire-bonded, a conformal coating was applied. A board as used for neutron testing is shown in Fig. 1.

The electrical connection was monitored using a 32-channel data acquisition system (DAQ), allowing individual current and voltage measurement for each diode. A 2 kV power supply unit (PSU) supplies all samples in parallel, fuses to interrupt and isolate after breakdown of a single diode sample are integrated in the PCB. The equivalent circuit and control unit are shown in Fig. 2.

Additionally, accelerated high-energy neutrons and protons experiments were performed for different commercial SiC MOSFET technologies with planar and trench gate design. Failure in Time (FIT) and SEB cross-sections were calculated as function of the drain-source bias voltage during the irradiation. Different latent damage was observed for the devices that did not fail. These results could provide important information on the SEB physical mechanism, which is still not completely understood among the scientific community.

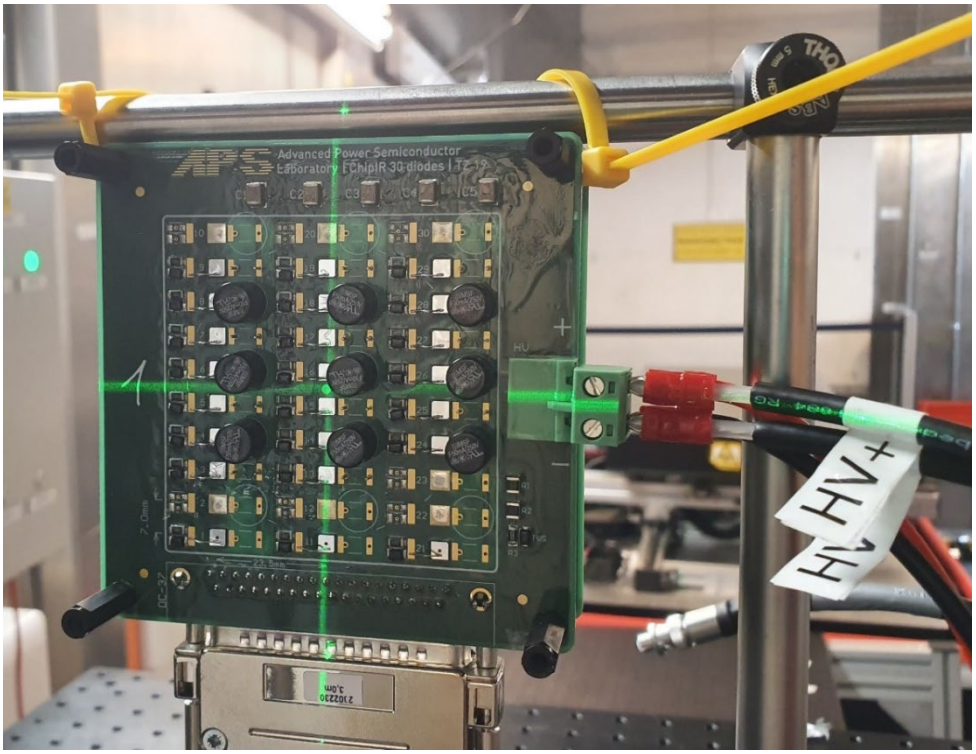

Fig. 1. PCB with SiC mounted for radiation hardness testing at ChipIR.

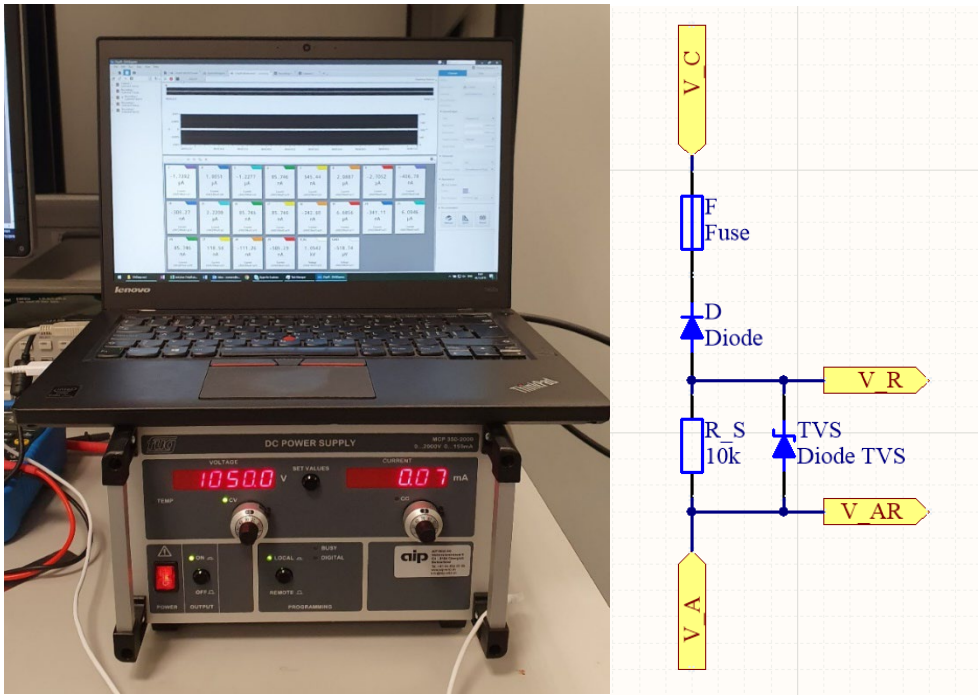

Fig. 2. Power supply and control for radiation hardness testing (left panel), equivalent circuit (right panel).

3.2 Switching Losses of Power Modules

The switching losses of the power module are characterized using the aforementioned dual-source double pulse tester. Double pulse testing is a common method used to measure the switching losses of power semiconductor devices, such as Integrated Gate Bipolar Transistors (IGBTs), MOSFETs and diodes. The test emulates hard-switched conditions with a highly inductive load, which is a very common usage scenario. This usage also results in the highest possible losses, since the device is exposed to both full load current and full DC link voltage at the same time during the switching process. The APS switching tester uses a modified topology with two sources, two capacitor banks and several auxiliary switches and diodes. The current in the inductor is delivered by low voltage capacitors, the high voltage capacitors only supply the test voltage and little to no current. This topology allows current and voltage to be controlled independently instead of being closely coupled through the inductor.

Whereas more tests where envisioned in the proposal phase of the project, the consortium partners have agreed to limit the tests of the power modules to the switching loss tests.

3.3 Simulation of Switching Losses and Improvement of Simulation Tools

With the increase of the computational power of todays' personal computers, the extensive multi-physics modelling of power semiconductor packages and devices becomes feasible. In the last decades, modelling as an engine for virtual prototyping has gained in importance and several powerful software tools have become commercially available allowing two or more design aspects (electrical-thermal-electromagnetic-mechanical) to be simultaneously modelled and investigated. The software tools have been selected for the dedicated modelling tasks based on the available built-in numerical methods.

The APS Laboratory has access to the following software packages:

- Multiphysics simulation at package level: Dassault (CST Studio Suite), KEYSIGHT (Momentum, EMPro), ANSYS (Q3D, HFSS, Icepak, Mechanical), COMSOL
- Electronic device characterization: Dassault IdEM
- Circuit simulation environments: SIMetrix Pro, LTSpice, KEYSIGHT ADS

The numerical engines based on the Finite Element Analysis (FEA) of COMSOL and ANSYS are employed for the thermo-mechanical coupled simulations.

Commercially available electromagnetic (EM) modelling tools offer numerical solvers specialized either for the low frequency (LF) or high frequency (HF) domain. Q3D Extractor, a specialized quasi-static EM tool for the extraction of parasitics, generates an EM model of a 3D geometry structure based on separate calculations of capacitive and inductive effects in a form of an equivalent electrical circuit (RLGC circuit). The needs to resort to radio frequency modelling techniques for predicting rather fast switching transients of power devices have been recognized and HF EM tools such as e.g. ANSYS HFSS and KEYSIGHT Momentum have been used. Consequently, APS obtained the licenses for CST Studio Suite and IdEM. CST Studio Suite offers LF and HF EM simulation engines with the functionality similar to ANSYS and COMSOL tools.

The IdEM tool is used for the generation of time domain models (circuit netlists) of frequency-dependent layout and package models. The frequency-dependent EM models are represented as multiport networks described by network S/Z/Y-parameters generated by electromagnetic modelling tools such as ANSYS HFSS, ANSYS Q3D, KEYSIGHT Momentum, etc.

For modelling the switching transients, device models are simulated in time-domain circuit simulators (SIMetrix Pro, LTSpice, KEYSIGHT ADS) together with circuit netlists of layout and package EM models. In comparison to other circuit simulators, Keysight ADS allows the circuit simulations directly with S-parameters, based on advanced algorithms for the S-parameter-to-impulse response conversion and convolution.

4 Results and discussion

The overall results of the entire project are summarized in Table 1. Table 2 lists the project goals, their status at the end of the project and some related comments.

Issue / Indicator	Initial value at start of project	Expected value at the end of project	Reached value	Further information
TRL progress	2 for Inverter 3 for Diode	2 for Inverter 5 for Diode	TRL 6 for Inverter TRL 5 for diode	A handful of inverter prototypes have been validated and certifications is ongoing. Diode technology was successfully developed into a test sample status being usable by system engineers in real applications.
Power density		10% improvement over baseline	8%	Initial and final values not given because the improvement is assessed in relative terms with respect to the baseline. The new inverter is outdoor (the baseline was indoor), which has a negative impact in power density.
Maximum voltage	Inverter deliver nominal power below 1300V	Deliver nominal power at 1500V	1350V	1500V will be achieved in 2021, in the framework of a new project already in progress.
Cost of product		Cost / kW compared to baseline solution	10%	Initial and final values not given because the improvement is assessed in relative terms with respect to the baseline. The new inverter achieves a 10% reduction in cost / kW.
Efficiency when providing reactive power for grid supporting		Efficiency improved with respect to baseline	+0.5% absolute efficiency	CEC efficiency has already been certified: 99.3%.
Cosmic Ray performance analysis	Limited understanding of influence of cosmic ray on FIT rates of inverter	Understanding and root cause analysis of cosmic ray performed	FIT established	FIT comparable to Si devices; root-cause of failure is anode-cathode short.
Efficiency of power module		30% efficiency improvement of power module over baseline	21% at 1kA, 42% at 200°.	Total switching losses are reduced by 21 – 42 % of previous Si-based technology (depending on current).
Tolerance of power module to cosmic radiation		Reduction of FIT due to cosmic radiation compared to baseline		Comparable FIT rate based on similar FIT-rate at device level expected, but not tested directly.
Testing at full scale		Inverter tested at full scale validating the achieved improvements.	Yes.	

Table 1. Results, targets and achievements – technological, economic, environmental and other indicators.

For the Swiss part of the consortium, the following specific technical results have been obtained:

#	TITLE	STATUS	COMMENTS
1	PV inverter capable of operating at full power up to 1500V	Achieved 1350V.	A new power block (with a more competitive technology than the one originally planned) is being manufactured to achieve 1500V. This new development is out of the scope of this project.
2	PV inverter with increased power density (kW/m3)	Achieved.	8% higher power density, despite the fact that the new inverter is outdoor.
3	Increase PV conversion efficiency by the usage of a new SiC diode technology	Achieved.	CEC efficiency has increased from 98.8% to 99.3% (values tested by an independent certification company).
4	Cosmic ray performance	Achieved.	Assessed by ETH Zurich.
5	Enhanced grid integration	Achieved.	Efficiency has increased for every power factor value, including 0 (reactive mode).
6	Full power test bench	Achieved.	Up to 3 MW was the commitment in the project proposal. 5 MW is the final value.

Table 2. Project goals, their status at the end of the project, comments.

4.1 Radiation Hardness

Testing of the semiconductor diode test structures using DLTS has revealed an increase in electrically active defects, leading to higher leakage currents in the samples and lower forward voltage current. This is expected and a well-established result.

The obtained FIT data of the tested fully processed diodes as acquired from proton and neutron testing is similar, with a slightly higher values for the protons. The tests have been conducted at the ChipIR facility[2] of the ISIS Neutron and Myon Source (neutron testing) and the Proton Irradiation Facility (PIF) at the Paul Scherrer Institut (PSI)[3]. As shown in Fig. 1 and 2, the power diodes are mounted on PCBs, and biased and controlled via a DAQ. The irradiation is continued until a statistically significant amount of devices failed at the respective bias voltage; the voltage is then changed for the next set of samples and the irradiation and data acquisition procedure restarted.

At 1500 V, a FIT per die of 200 has been found. Comparing the results to the ones in literature, the newly developed SiC diodes show a higher FIT per active area than Si devices[4] and SiC MOSFETs[5] for voltages lower than 1300V, but outperform the Si devices for voltages above that threshold (see Fig.3).

This is a result which shows the successful design and manufacturing of reliable SiC diodes for operation at high system voltages, as they deliver a similar cosmic ray hardness as a specifically hardened device, hence expensive technology (CAL4 diode) and a better FIT than the Si diodes to be replaced (reference diode). As the system voltage is set to 1500V, the performance at this voltage, not below, is relevant for the comparison. The MOSFETs used for comparison of SiC device performance have shown to be designed with a larger derating in voltage capablility; when taking into account the breakdown voltage

[2] https://www.isis.stfc.ac.uk/Pages/ChipIR.aspx

[3] http://pif.web.psi.ch/

[4] Scheuermann, Schilling: “Impact of device technology on cosmic ray failures in power modules.” IET Power Electronics, 2016, Vol. 9, Iss. 10, pp. 2027–2035

[5] Lichtenwalner et al. “Reliability of SiC Power Devices against Cosmic Ray Neutron Single-Event Burnout.” Materials Science Forum, vol. 924, June 2018, pp. 559–562.

of the devices, the SiC diodes of this project show a superior design with respect to the termination region (result achieved by the consortium partner Infineon; see Transnational Project Report attached).

An analysis of the failure mode of the tested devices revealed an anode-cathode short (not shown here), further corroborating the superior device design od the SiC diodes of this project.

4.2 Switching Performance

With the newly designed DPT, switching performance of the power modules has been tested for samples containing Si IGBTs and Si diodes as well as samples containing Si IGBTs and SiC diodes. The following parameters have been used:

- gate voltages of +15 V / -10 V,
- gate resistances of 1.2 Ω / 3.4 Ω,
- case temperature of 25 °C,
- collector current between 250 A and 1000 A (4 datapoints), using an applied collector-emitter voltage between 900 V and 1200 V, respectively.

For turn-on, using SiC diodes has resulted in a 26–60% improvement compared to the solution using Si-diodes; the total switching energy was 21–42% lower compared to the Si solution, depending on the current level. A direct comparison of the two sets of samples is presented in Fig. 4.

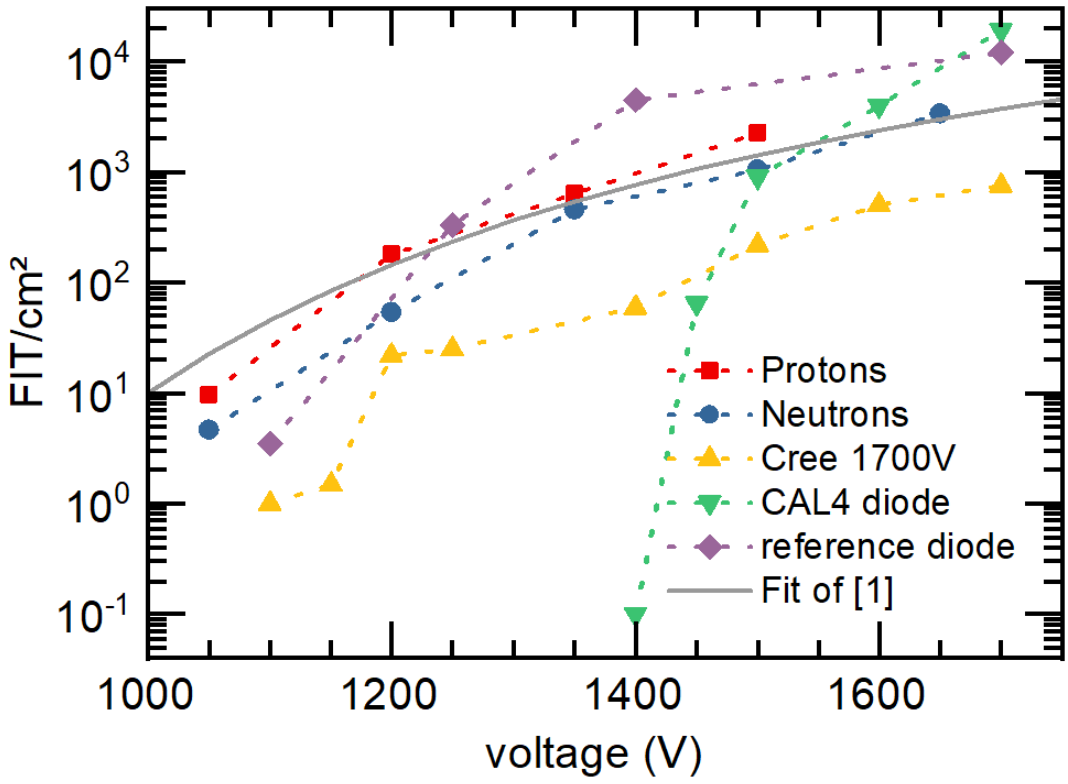

Fig. 3. Radiation hardness as measured in FIT/cm² for the newly developed SiC diodes using protons (red squares) and neutrons (blue dots). For comparison, data for SiC MOSFET technology (denoted “CREE 1700V”, yellow triangles) and Si diodes (CAL4 diode, green triangles and reference diode, purple diamonds) are shown.

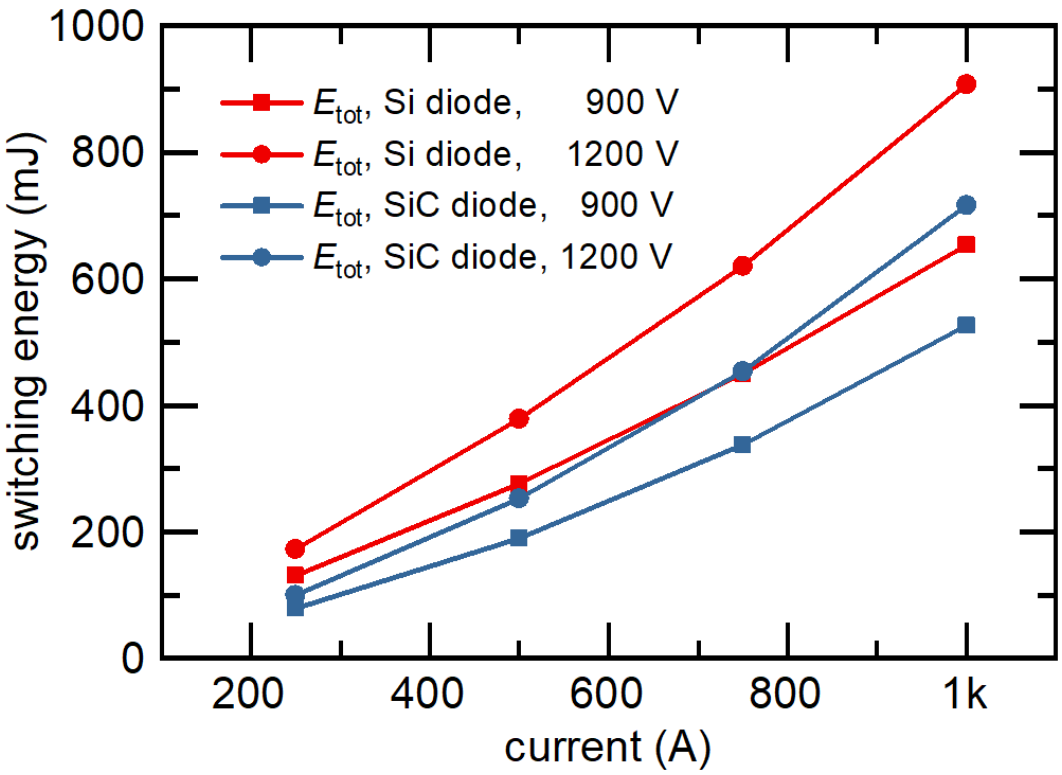

Fig. 4. Total switching energy for two sets of IGBT modules. Containing Si diodes: red data points, containing SiC diodes: blue data points.

4.3 Power Module Optimization Using Virtual Prototyping

Extensive analysis of the available commercial tools for simulation of power device switching performance has been performed. The switching tester utilized within the project has been fully characterized for parasitic circuit elements and the parameters have been used for cross-calibration of experimental with the different simulation results. In consequence, it has been found that the many aspects such as circuit and package layout parasitic effects as well as thermal couplings cannot be neglected in the design optimization process for advanced power modules. These multi-physics design tasks can be approached by using different modeling tools for assessing the behavior of advanced power module prototypes before the actual package fabrication. The trade-off between accuracy and computational time has been an important challenge preventing virtual prototyping based on multi-physics modeling to further reduce the needs for extensive hardware prototyping.

The APS research team has been working on the analysis of the existing modelling tools and methods for multiphysics modeling of power semiconductor devices and their packages increasing the understanding of the state-of-the-art limits with respect to modeling accuracy and computational complexity. The main research has been focused on the circuit-thermal-electromagnetic coupled simulations establishing a comparative analysis of different numerical methods and coupling approaches. In parallel, own modelling tools taking advantage of specialized numerical methods are being developed, which allow a simultaneous control of accuracy and computational cost. Most of the effort is directed towards efficient automated system design procedures for finding optimal design solutions at minimal costs by considering dominant multi-physics design aspects. An ETH thermal modeling tool for analyzing thermal aspects

of power semiconductor packages has been further developed[6], tuning its capabilities for modeling WBG power semiconductor packages operating at higher temperatures. Furthermore, a collaboration with the EMC Lab research group led by Prof. Dr. Giulio Antonini at the University of L'Aquila has been further strengthened in the framework of this project; first joint publications include the assessment and further development of a full physics-based circuit simulation technique[7].

Based on the assessments made during the power module testing and of the simulation tools, a new concept for an advanced power module utilizing SiC devices was developed. Beyond the scope of this project, but targeting a similar application, the design study results in lower loss, higher switching frequency, and higher power density (not shown here).

4.4 Dissemination and Communication of Results

The consortium is currently working towards a joint peer-reviewed publication of the results. Furthermore, the project has resulted in 1 white paper, one Disclosure of Invention, 3 partially related PhD theses and a Science Brunch Austria presentation (see also the final Transnational Progress Report attached). Currently, the dissemination activities are severely impacted by the Covid-19 situation.

5 Conclusions

The project enabled a variety of growth opportunities for APS and a new product line for each of the two collaborators. APS was able to establish a research infrastructure entire new to the ETH domain and within Switzerland.

SiC has proven to be a rugged and energy-efficient technology, enabling utilization in demanding applications such as high-power utility-scale power conversion.

6 Outlook and next steps

The project team has put together a dissemination plan including specific conferences such as PCIM where the consortium will target to submit a joint publication outlining the outcomes of the program now that experimental results are available. Besides, the 1500-SiC project will be presented in the course of the Science Brunch, an event initiated by the climate and energy funds in Austria, where also a booklet will be published. This event was initially planned to take place in May 2020 but was finally shifted to October 2020 due to the worldwide COVID-19 pandemic. Solar exhibitions such as Intersolar will be targeted once Gamesa Electric is in position to commercialize the results. Most targeted events are facing difficulties and cancellations due to COVID-19. Therefore, the dissemination will take place after the end of the project, most likely in 2021.

The testing and analysis tools developed for this project are establishing both the power module testing as well as the cosmic radiation testing capabilities at APS and will continued to be used in future projects.

[6] Race et al. "Electrothermal Modeling Including Temperature-dependent Material Properties for Silicon Carbide Power Electronics Applications", to be published.

[7] Romano et al., "Circuit synthesis techniques of rational models of electromagnetic systems: A tutorial paper", International Journal of Numerical Modelling-Electronic Networks Devices and Fields, vol. 32: no. 5, pp. e2612, Chichester: Wiley, 2019.; "Rigorous dc Solution of Partial Element Equivalent Circuit Models Including Conductive, Dielectric, and Magnetic Materials", IEEE Transactions on Electromagnetic Compatibility, vol. 62: no. 3, pp. 870-879, New York, NY: IEEE, 2020.

The accumulated know-how is planned to be published in a post-project phase, comparing the different approaches and impact of different particle beams.

7 National and international cooperation

Throughout the project, communication and interaction with both consortium partners was performed. The results of switching tests both at power module as well as for the full-scale converter were discussed in the consortium meetings. Discussions on radiation hardness of SiC diodes were of high technical excellence. Overall, the cooperation was informative, targeted and is enabling future collaborations.