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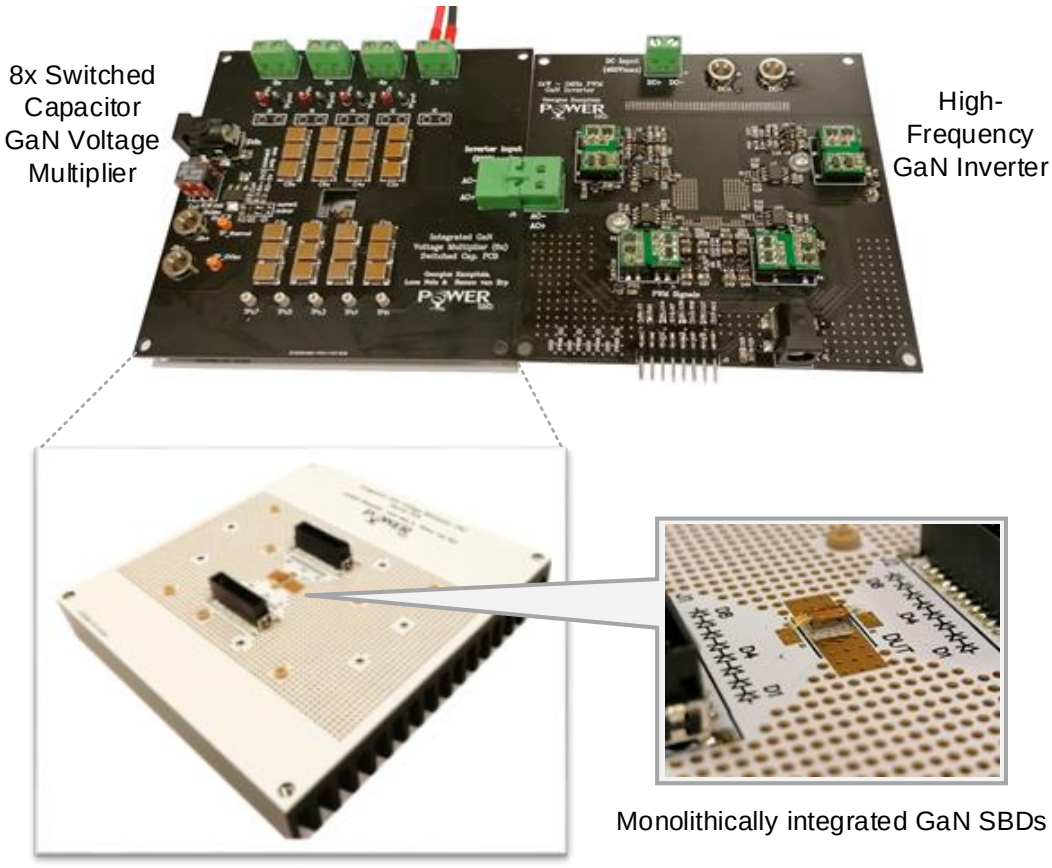
High-efficiency power converters for potentially-large energy-savings applications



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Zusammenfassung

Ziel dieses Projekts ist es, Stromrichterschaltungen mit großem Energieeinsparpotenzial für anspruchsvolle Anwendungen wie PV-Mikrowechselrichter und LED-basierte Straßenbeleuchtung zu entwerfen und zu demonstrieren. Diese Arbeit zeigt nicht nur das volle Potenzial der bei Powerlab-EPFL entwickelten Technologien, sondern ermöglicht auch eine enge Beziehung zu den Branchen. Dieses Projekt ermöglicht in Kombination mit der einzigartigen Struktur unseres Labors eine Optimierung sowohl auf der Geräte- als auch auf der Schaltkreisseite, da die Informationen aus den Schaltkreisen als Feedback zur Optimierung der Geräte und umgekehrt verwendet werden können. Dieser Ansatz eröffnet eine neue Ära für Leistungselektronikanwendungen und das aktuelle Projekt hat dazu beigetragen, unsere Arbeit zu beschleunigen, zu demonstrieren und zu kommunizieren. Der erste Teil dieses Projekts war der Identifizierung der Wandlertopologie gewidmet, die die vorteilhaften Eigenschaften der lateralen GaN-HEMTs am besten ausnutzt. Wir haben einen modularen 2,5-kW-Switched-Capacitor-Multilevel-Wandler ohne magnetische Komponenten entworfen und entwickelt, der nur 0,2 l Volumen einnimmt. Dieses System wurde später auf eine neue PV-Architektur angewendet, die auf der Parallelschaltung mehrerer PV-Module auf der Hochspannungsseite dieser Wandler basiert. Unser Ansatz hilft dabei, den Energieverlust im Zusammenhang mit teilweiser Verschattung anzugehen. Um die Leistungsdichte des Prototyps des magnetfreien Wandlers zu maximieren, haben wir ein neuartiges mikrofluidisches Kühlsystem entwickelt, das auf reinraumgefertigten Si-Kühlplatten basiert und für maximale Leistungszahlen optimiert ist. Auf Bauteilebene haben wir eine hochskalierte Tri-Anode-GaN-Schottky-Barrier-Diode hergestellt und den ersten monolithisch integrierten Vollbrückengleichrichter und passiven Spannungsvervielfacher in einer Cockcroft-Walton-Konfiguration demonstriert. Letztendlich hat unsere Arbeit in diesem Projekt die Grenzen der Konvertertechnologie erweitert, indem alle vorteilhaften Eigenschaften von Materialien mit großer Bandlücke ausgenutzt wurden.

Résumé

Le but de ce projet est de concevoir et de démontrer des circuits de conversion d'énergie offrant un potentiel important d'économie d'énergie dans des applications exigeantes, telles que les micro-onduleurs photovoltaïques et l'éclairage public à LED. Ces travaux illustrent non seulement le potentiel des technologies créées au Powerlab-EPFL, mais facilitent également les relations étroites avec les industries. Ce projet, associé à la structure unique de notre laboratoire, permet une optimisation à la fois du côté dispositif et du côté circuit. Les informations provenant des circuits peuvent notamment être utilisées comme rétroaction pour optimiser les dispositifs et inversement. Cette approche ouvre une nouvelle ère pour les applications en électronique de puissance et le projet en cours a permis d'accélérer, de démontrer et de communiquer notre travail. La première partie de ce projet visait à identifier la topologie de convertisseur qui exploite au mieux les caractéristiques avantageuses des GaN HEMT latéraux. Nous avons conçu et mis au point un convertisseur multiniveau modulaire à condensateur commuté de 2.5 kW sans composant magnétique qui occupe seulement 0.2 L de volume. Ce système a ensuite été appliqué à une nouvelle architecture PV basée sur la connexion en parallèle de plusieurs modules PV du côté haute tension de ces convertisseurs. Notre approche permet de réduire la perte d'énergie liée à l'ombrage partiel. Afin de maximiser la densité de puissance du prototype de convertisseur sans magnétique, nous avons développé un nouveau système de refroidissement microfluidique, basé sur des plaques froides en Si fabriquées en salle blanche et optimisé pour un coefficient de performance maximal. Au niveau des appareils, nous avons fabriqué une diode à barrière Schottky à trois anodes GaN mise à l'échelle et avons présenté le premier redresseur en pont complet et multiplicateur de tension passifs intégrés monolithiquement dans une configuration Cockcroft-Walton. Finalement, notre travail dans le cadre de ce projet a repoussé les limites de la technologie du convertisseur en exploitant toutes les propriétés avantageuses des matériaux à large bande interdite.

Summary

The purpose of this project is to design and demonstrate power converter circuits with large energy saving potential in demanding applications, such as PV microinverters and LED-based street lighting. Not only does this work showcases the full potential of the technologies created at Powerlab-EPFL, but also facilitates a close relationship with industries. This project, in combination with the unique structure of our Lab, enables optimization in both the device and circuit sides, as the information from circuits can be used as feedback to optimize the devices and vice-versa. This approach opens a new era for power electronics applications and the current project helped fast-track, demonstrate and communicate our work. The first part of this project was dedicated to identify the converter topology that best exploits the advantageous characteristics of the lateral GaN HEMTs. We designed and developed a 2.5kW switched capacitor modular multilevel converter with no magnetic components that occupies only 0.2L of volume. This system was later applied to a new PV architecture based on the parallel connection of multiple PV modules at the high-voltage side of these converters. Our approach helps address the energy loss related to partial shading. To maximize the power density of the magnetic-free converter prototype, we developed a novel microfluidic cooling system, based on clean-room fabricated Si cold plates and optimized for maximum coefficient of performance. In a device level, we fabricated a scaled up Tri-anode GaN Schottky Barrier Diode and demonstrated the first monolithically integrated full bridge rectifier and passive voltage multiplier in a Cockcroft-Walton configuration. Ultimately, our work within this project pushed the limits of the converter technology by exploiting all advantageous properties of wide band-gap materials.

Main findings

- Development of a new ultra-compact and efficient magnetic-less DC/DC converter with high step-up conversion ratio and low cooling requirements. The developed system has huge potential of entering the market related to renewable energy generation, electric vehicles and data centre applications.
- Utilization of the developed magnetic-free converter in a module-level PV architecture in parallel-configuration for maximum power extraction under partial shading conditions. The new PV configuration is capable or increasing up to 20% the annual energy yield of residential PV systems in urban areas with low installation height.
- Development of a compact and energy-efficient cooling system based on multiple miniaturized microfluidic cold-plates compact through a 3D-printed flow distribution manifold. This novel approach offers a new way of co-engineering the cooling and the electronics together to achieve more compact and efficient power converters.
- Demonstration of the first monolithically integrated GaN full bridge rectifier and an 8-time GaN voltage multiplier in a Cockcroft-Walton configuration, utilizing the Tri-Anode GaN Schottky Barrier Diodes (SBDs), developed in our Lab.

Contents

Abbreviations

2DEG	Two-dimensional electron gas	**MSB**	Most significant bit
AGM	Absorbed glass mat	**NOCT**	Nominal operation cell temperature
BMS	Battery management systems	**P&O**	Perturb and Observe
CAD	Computer-aided design	**PCB**	Printed circuit board
CNC	Computer numerical controlled	**PI**	Proportional Integral
COP	Coefficient of Performance	**PLL**	Phase locked loop
DER	Distributed energy resources	**PR**	Proportional-resonant
DI	Deionized	**PS**	Partial shading
DOD	Depth of discharge	**PV**	Photovoltaic
DPT	Double pulse tester	**PVPO**	PV power optimizers
FBR	Full Bridge Rectifier	**PWM**	Pulse width modulation
FOB	Focused ion beam	**SBD**	Schottky Barrier Diode
FRB	Fast-recovery diode	**SEM**	Scanning electron microscope
HEMT	High Electron Mobility Transistor	**SLA**	Stereolithography
IC	Integrated circuit	**SoC**	State of charge
ICP	Inductively coupled plasma	**SOGI**	Second-order generalized integrator
IR	Infrared	**SP**	Series-Parallel
LED	Light emitting diode	**SS**	Subthreshold swing
LPF	Low-pass filter	**TCT**	Total cross-tied
LSB	List significant bit	**TCTR**	TCT rearranged
MCU	Microcontroller unit	**TIM**	Thermal interface material
MLPE	Module-level power electronics	**VMPV**	Voltage multiplied Photovoltaic
MMC	Manifold microchannel	**VRLA**	Valve regulated lead-acid
MMCC	Modular multilevel capacitor clamp	**ZCS**	Zero current switching
MPPT	Maximum power point tracking		

1 Introduction

1.1 Background information

In this project all of the defined goals were met and the milestones summarized in Table 1 have been surpassed. A short description of the different aspects of the project is given in this section and a detailed explanation is presented later in this report.

Milestones	Sept 2017	2018	2019	March 2020
M1: Design and Efficiency comparison of soft- and hard-switching topologies				
M2: Demonstration of initial circuits for LED-street lighting				
M3: Design and demonstration of initial circuits for PV micro-inverters				
M4: Integration of full prototype				
M5: Feedback to our devices and circuit re-design				
M6: Final prototype design and demonstration				
M7: Technology transfer to companies involved				
M8: Final report				

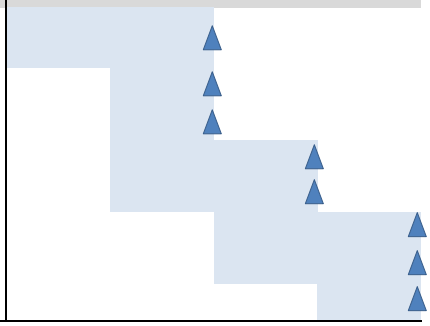


Table 1. Milestones

For the 1st Milestone, *Design and Efficiency comparison of soft- and hard-switching topologies*, we investigated new switching capacitor topologies, both with transistors and diodes, for high power density applications. First, we examined a modular multilevel capacitor clamped (MMCC) DC/DC converter with a 10-times voltage boost capability and soft switching operation, achieved by tuning the switching frequency to match the internal resonant frequency. We then proceeded with the investigation of a diode-based switching capacitor topology that utilizes the state-of-the-art monolithically integrated diodes developed in POWERLab. For efficient implementation of this part of the project, there was a close collaboration between the circuit design and the device fabrication teams, in accordance with the Milestone 5, *Feedback to our devices and circuit re-design*.

We also fulfilled the 6th Milestone, *Final prototype design and demonstrati*on, regarding the PV micro-inverters. We utilized the developed MMCC converter to boost the output voltage of a PV panel by 10 times, an approach that enables the parallel connection of all the PV modules at the common high-voltage DC-Bus. We demonstrated that our new PV architecture can have better conversion efficiency (>96%) and significantly higher power extraction efficiency (>99.7%) compared to state-of-the-art topologies, while the parallel connection addresses all issues related to partial shading.

We also moved forward with the 4th Milestone, *Integration with full prototype*, by optimizing the new microchannel liquid cooling heatsinks, dedicated to the micro-inverter prototypes. A thorough mathematical analysis was performed to find the optimum microchannel width that result to the best coefficient of performance at minimum flow rate and pressure drop. We developed an aluminum milled and a 3D printed heatsink that incorporate the clean-room fabricated microchannel cold-plates to assess the performance of our novel cooling system. The results show by co-designing the electronics with an efficient cooling system we can reduce the thermal resistance of the heatsink by one order of magnitude.

We have also completed the *Final prototype design and demonstration* of the *circuit for LED-street lighting* (Milestones 4th and 2nd and 3rd). We completely redesigned the entire system to achieve a long lifetime, reliability and low cost. We revisited both the energy storage system and the PV module. We also developed an online human interface environment for storing and managing useful data, such as produced and consumed power, battery temperature, local environmental conditions and more.

Finally, this report is the realization of the last Milestone, *Final report*, which includes noteworthy outcomes of our research, reveals our approach to disseminate our results in high-impact factor journals and international conferences and proposes ideas for a successful continuation of our work.

1.2 Purpose of the project

The main purpose of this project is to design and demonstrate power converter circuits that will be part of a full demonstrator for two main applications: PV microinverters and LED-based street lighting. This project is complementary to the SFOE-funded project: “GaN-based Power Electronics for Energy Efficiency Applications”, however the present project aims to focus on the conclusions obtained in this first SFOE project to develop real-size demonstrators. This not only showcases the full potential of the technologies created at Powerlab-EPFL, but facilitates a close relationship with industries. The final goal of this project was to develop and transfer these technologies to the industry, which in our view is the only way for our technologies to reach their full societal impact.

This project is strongly related to our current activities, since in our long-term our goal is to deploy the designed and fabricated devices in our laboratory. This gives an extra degree of freedom for optimization in both the device and circuit sides, as the information from circuits can be used as feedback to optimize the devices and vice-versa. In addition, other circuit components have also been re-designed (as the high frequency of GaN devices allows the reduction of parasitic inductive and capacitive components, and their high temperature operation reduces the need for cooling systems). This is in particular relevant for magnetic components, which can be much reduced in size under high frequency with a judicious design. This allowed the demonstration of more efficient systems with much reduced footprint.

1.3 Objectives

The main objective of this project was to demonstrate optimum converter topologies with co-designed cooling systems that fully exploit the potential of GaN technology. To reach this goal, we addressed several scientific and practical challenges. More specifically, the layout of the magnetic-free converter had to be carefully designed to overcome all electromagnetic interference (EMI) issues, related to the Miller effect and driver-to-transistor physical distance. At the same time, maximizing the power density of the converter increases the heat fluxes, which in turn makes the heat extraction a challenging task. To this end, we needed to come up with an efficient liquid cooling system with high coefficient of performance, low pressure drop and low flow rate requirements. Additionally, equal distribution of the coolant to all GaN devices needed to be ensured for a reliable operation. Another goal of the project was to apply the magnetic free converters in a PV application with large energy saving potential. In this field, we addressed the issues related to the parallel connection of multiple nX converters on the same high voltage DC bus and, more specifically, the reverse current flow formed by the switched capacitors current loops. Also, to maximize power extraction capability of the PV generator, even in-non uniform insolation conditions, we had to transfer all control functionalities in a secondary conversion stage (inverter / regulated dc/dc converter), while retaining low control complexity. Finally, to achieve system miniaturization we addressed the challenges of monolithic integration of several power devices on the same substrate. The first objective was to scale up (in current) our SBDs and, then, solve the problems related to the common-buffer leakage. Ultimately, our work resulted in novel approaches for combining electronics, cooling and device fabrication.

2 Procedures and methodology

This project has been the enabling factor for the development of methods of power conversion with large energy saving potential. Our main goal was to push the limits of power density of the state-of-the-art converter by exploiting one of the most interesting characteristics of the GaN technology: i.e. the lateral structure of the GaN HEMTs that offers the possibility to monolithically integrate several devises in a single power integrated circuit (IC). This feature opens a new era for power electronics applications and the current project helped fast-track, demonstrate and communicate our work.

The work started with the introduction of a new ultra-compact and efficient magnetic-less DC/DC converter, shown in Figure 1(a), suitable for photovoltaic (PV) systems (but also for electric vehicles, data centers and DC microgrids) that eliminates all magnetic components, which commonly dominate the size and weight of power systems. The transistor technology also helped migrate from bulky and unreliable electrolytic capacitors to efficient, compact and long-lifetime multilayer ceramic capacitors. We optimized the circuit by developing a detailed model of a single cell (2x conversion ratio) and running simulations in Matlab/Simulink.

We took full advantage of the exceptional performance of the magnetic free converter by introducing a module-level PV architecture in parallel-configuration for maximum power extraction, under partial shading (PS) conditions (**Section 3.1**). The nX converter is intended to boost the PV voltage by a fixed ratio, while the maximum power point tracking MPPT is shifted to the grid-side inverter. Although simple, this approach has not been tested before. We connected the voltage-multiplied PV modules (VMPV) in parallel to a common DC-bus, which offers expandability to the system and eliminates the PS issues of a typical string architecture. Our approach relieves the PV-side converter from bulky capacitors, filters, controllers and voltage/current sensors, allowing for a compact and efficient conversion stage. We initially simulated the new configuration in a 5 kW residential PV system and compared against conventional PV arrangements. For the experimental validation, we tested the VMPV architecture on a 2-module 500 WP prototype, exhibiting an excellent power extraction efficiency of over 99.7% under PS conditions and minimal DC-bus voltage variation of 3%, leading to a higher total system efficiency compared to most state-of-the-art configurations.

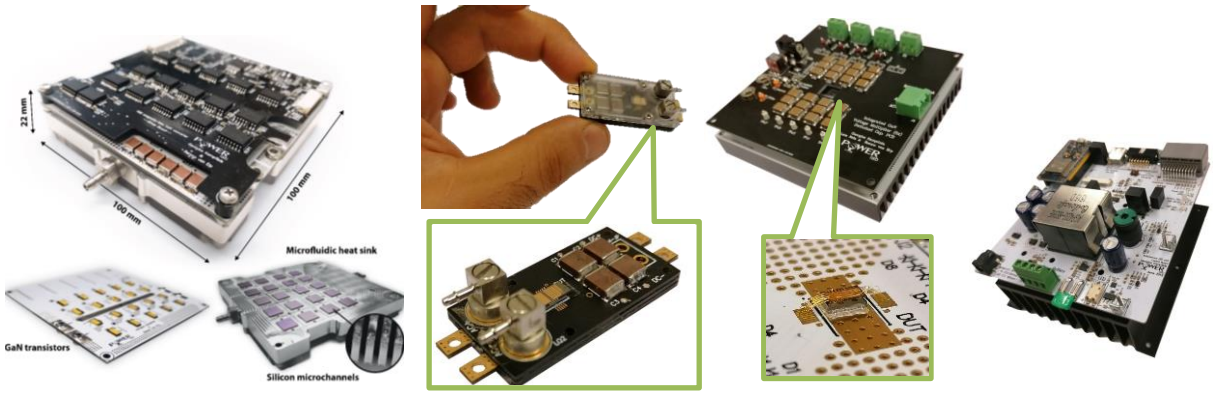


Figure 1: (a) High power density GaN-based magnetic-free converter with co-designed micro-fluidic cooling system. (b) Monolithically integrated full-bridge rectifier of 120W with embedded microchannels and liquid distribution system (c) 8x voltage multiplier with monolithically integrated SBDs (d) New MPP tracker for the autonomous street lighting system. It features WiFi and Bluetooth connectivity for collective valuable information on a server.

To optimize the heat extraction capability of our new converter, we developed a new approach for compact and energy-efficient cooling, where multiple miniaturized microfluidic cold-plates are attached to the transistors, as depicted in Figure 1(a). We minimized the high pressure drop associated with microchannels by connecting these cold-plates in parallel using a compact 3D-printed flow distribution manifold. In **Section 3.2** we present the modeling, design, fabrication and experimental evaluation of this microfluidic cooling system and provide a design strategy for achieving energy-efficient cooling with minimized pumping power. A thermal resistance of 0.2 K/W was measured at a flow rate of 1.2 ml/s and a pressure drop of 600 mbar, enabling the cooling of a total of 300 W of losses in the converter using only 75 mW of pumping power, which can be realized with small micropumps. Experimental results show a 10-fold increase in power density compared to conventional cooling, potentially up to 30 kW/l. Our cooling approach offers a new way of co-engineering the cooling and the electronics together to achieve more compact and efficient power converters.

Having demonstrated a fully functional magnetic-free converter and its cooling system, we moved forward miniaturizing the system by integrating several devices on the same chip. This step was revolutionary, both for our lab and the research community, since it requires the expertise for several different disciplines (material science, electrical engineering, mechanical engineering). As a first demonstrator we developed a full bridge rectifier, shown in Figure 1(b), utilizing the Tri-Anode GaN Schottky Barrier Diodes (SBDs), developed in our Lab. As explained in **section 3**, our SBDs show excellent DC performance with low turn-on voltage and large breakdown thanks to their 3D contact structure around the two-dimensional electron gas (2DEG) channel. More importantly, though, they exhibit remarkable dynamic performance, proven by the substantial decrease in the recovery charge and an improvement in frequency response. In the same context of integrating several GaN SBDs on the same chip, we demonstrated the first GaN voltage multiplier in a Cockcroft-Walton configuration, illustrated in Figure 1(c), where 8 scaled-up diodes constitute the core of a 70W 8-time voltage boost converter.

We also expanded our knowledge on the microfluidic cooling systems and developed a new direct-cooling system for GaN-on-Si power integrated circuits (ICs), in which the silicon substrate functions as a microfluidic heat sink, turning Si into a cost-effective, high thermal performance substrate. Flowing coolant through microchannels etched in the backside of the substrate enables a much denser integration of GaN power devices in a single chip. A novel hybrid printed circuit board (PCB) was also developed (see Figure 1(b)) that provides fluidic and electric connection to the liquid-cooled power IC. We believe that the high cooling efficiency, large heat extraction capabilities and low-cost fabrication process of embedded microchannels on GaN-on-Si, in combination with new PCB based coolant delivery, can be an enabling technology for the next generation of ultra-high power-density ICs.

We also revisited the autonomous LED street lighting system to finalize its design and add features for enhancing the system-to-human interface. We collaborated with a team of architects that designed a custom PV panel that is aesthetically appealing and has the electrical requirements specified by this application. Gel lead-acid batteries replaced the old LiFePo4, given that weight is not a restriction to the system and they can perform way more reliable in low temperature conditions. A completely new MPP tracker, shown in Figure 1(d), was designed and developed that incorporates both the battery charger and the LED driver in a single PCB. The system also features WiFi connectivity that helps upload important statistical data, such as environmental conditions, produced energy, consumed energy, etc., on an online server. Final a graphical user interface was developed to present the stored data in a representative form.

3 Results and discussion

Throughout this project, we have achieved the following, summarizing results:

1. **Demonstration of a new PV architecture based on the magnetic-free micro-converters**: We have revisited the topologies used in conventional energy conversion systems for PV applications and have proposed a completely new PV arrangement. We utilize a high power density magnetic-free nX converter with each PV panel to form a high voltage module and then connect them in parallel, effectively addressing the partial shading issues. The flat efficiency curve of the nX converter, combined with the outstanding power extraction efficiency of the parallel architecture is estimated to increase the energy yield up to 20% in residential PV systems.

2. **Optimization of the new near-junction microfluidic heatsinks:** We developed customized clean room fabricated Si-based microchannels and liquid spreading manifolds that can effectively cool down the local hotspots of modern GaN-based power converters. These heatsinks were used to cool down the developed converters utilizing both commercial transistors but also our Lab's GaN devices. We designed and developed two liquid distribution manifolds, one aluminum milled and a 3D printed, that equally distribute the coolant to all hotspots. We optimized the cooling system by performing a detailed mathematical analysis, supported by 3D finite element simulations.

3. **Demonstration of state-of-the-art devices fabricated in our laboratory**: We have developed extremely fast GaN Schottky barrier diodes with high breakdown voltages (>600V), ultra-low leakage current and negligible reverse recovery charge. Our devices performance well surpasses all other commercial diodes of any technology (Si or SiC). To fully exploit the advantageous features of our devices we demonstrated scaled-up diodes with a current capability >2A.

4. **Monolithic integration of our devices to form power ICs**: We integrate several of our novel SBDs in a single chip to form high power ICs. We first developed a full bridge rectifier and tested it up to 120W. The system was cooled-down through our established microchannel cooling system and a liquid distribution integrated in the PCB. Our latest achievement concerns the fabrication of an 8x integrated voltage multiplier in Cockcroft-Walton configuration, tested up to 70W. This prototype is one step closer to the magnetic-free converter concept and showed promising potential for the future power ICs.

5. **A complete redesign of the autonomous street lighting system**: We updated the entire system (including the energy storage system, the PV module, the MPPT tracker), while considering reliability and cost as the main criteria for this practical applications. We collaborated with a team of architects that designed a practical and, at the same time, aesthetically appealing PV generator, the construction of which was performed in EPFL, Microcity Lab. We also developed a database for storing useful information of the autonomous LED light (produced and consumed power environmental conditions and more), through WiFi communication protocol. We finally built a graphical user interface to present the data in a concise and representative manner.

6. **Established new collaborations and obtained extra funding to help the execution of the project**: In addition to the grants that we have for the complementary projects including the SNSF projects, ERC Starting Grant, SNSF *Assistant Professor Energy Grant***,** *European Space Agency (ESA)*, which focus on new technologies to scale up our devices for the applications related to this project. This project was a major enabler for us to establish collaboration with large European companies and laboratories, through an European Union H2020 ECSEL projet (UltimateGAN), which awarded 48M Euros for 26 partners in Europe. This project is enabling a close collaboration of our laboratory with the semiconductor company Infineon. In addition, we are currently establishing collaboration projects with other large semiconductor and power companies such as ABB and Eaton. We have also established collaborations with a Swiss company (Aebischer & Bovigny) to design and fabricate automated lighting systems. We have also established collaborations with a Swiss company Montena to design high-power pulse generator systems.

These achievements are described more in details below:

3.1 GaN-Based Micro-Converters for Maximum Energy Extraction from PV Generators

3.1.1 Voltage Multiplied PV Architecture

Photovoltaics (PV) are increasingly gaining grounds over other power generation technologies, conventional or renewables, and are expected to dominate in future distributed energy resources (DER) and smart grid applications [1]. This trend is supported by the latest statistics, according to which the PV capacity installation in 2017 surpassed all other technologies, for the first time in history [2]. However, maximum energy extraction from the PV generator is commonly hindered due to partial shading (PS) conditions. This is particularly sever in urban environments, with low installations height. According to [7]–[9], PS is responsible for a reduction of the annual energy yield by 10-20% in building integrated PVs.

To increase the PV energy production under PS conditions, various software and hardware solutions have been proposed over the last decades. Although economical and easily applicable, software solutions, such as enhanced maximum power point tracking (MPPT) algorithms[3] [4], can only have a limited impact, since the shaded modules will still be bypassed or will operate at sub-optimum power point. On the contrary, hardware solutions can offer a significant improvement in PV generation during PS. More specifically module-level power electronics (MLPE) is the most effective hardware solution for PS loss mitigation. This approach aims to maximize the power yield of each individual panel through dedicated MPPTs.

In this field, micro-inverter topologies have proven commercially successful, since they offer the flexibility to connect any number of PV modules directly to the AC grid [5], but they exhibit low power density, due to the large component count and strict filter requirements [6]. Other popular MLPE alternatives include the PV power optimizers (PVPO) [7], distributed power processors [8] and voltage equalizers [9], which are buck-boost DC-DC converters, integrated with the solar panels of a typical string arrangement. According to [10], these systems have lower long-term efficiency compared to micro-inverters and reduced expandability, due to the minimum required string length [11]. The state-of-the-art approach promotes *micro-converters* that allow parallel connection of the PV modules in a single DC-bus, through high step-up DC-DC converters [26]. This solution aims to exploit the clear advantages of parallel-configuration for addressing PS effects [27]. Several converter topologies with large voltage boost ratio have lately been proposed, including cascade boost [26], coupled inductors [28], switching capacitors [29], and combinations of the above. However, these topologies are known to require complicated control algorithms and, most importantly, employ electrolytic capacitors and magnetic components that limit the power density and the lifetime of the system. They also exhibit significant efficiency drop in low loading conditions, which is a drawback, given that a PV generator operates within 30%-80% of its nominal power for 80% of the time [34].

Our goal is to successfully address the PS issues and overcome the limitations of the conventional converters and, by utilizing the highly efficient and compact nX converter, already developed within this project in PowerLab. The foundation of the new approach relies on the combinations of a non-regulated high-step-up micro-converter with each PV panel, to form a high-voltage/low-current building block. All the Voltage Multiplied PV (VMPV) modules are connected in parallel at the input of the grid-side inverter, which simultaneously regulates the operating point of all PV panels with a central MPPT. Each module contributes additively to the total system output by injecting the power that corresponds to the common DC-voltage, i.e. $P_{PV\text{-}j}(V_{PV\text{-}j} = V_{DC}/n)$, where $P_{PV\text{-}j}$ and $V_{PV\text{-}j}$ are the output power and voltage, respectively, of the j panel. A simplified schematic of the proposed VMPV architecture is presented in Figure 2 (a, topology *iv*).

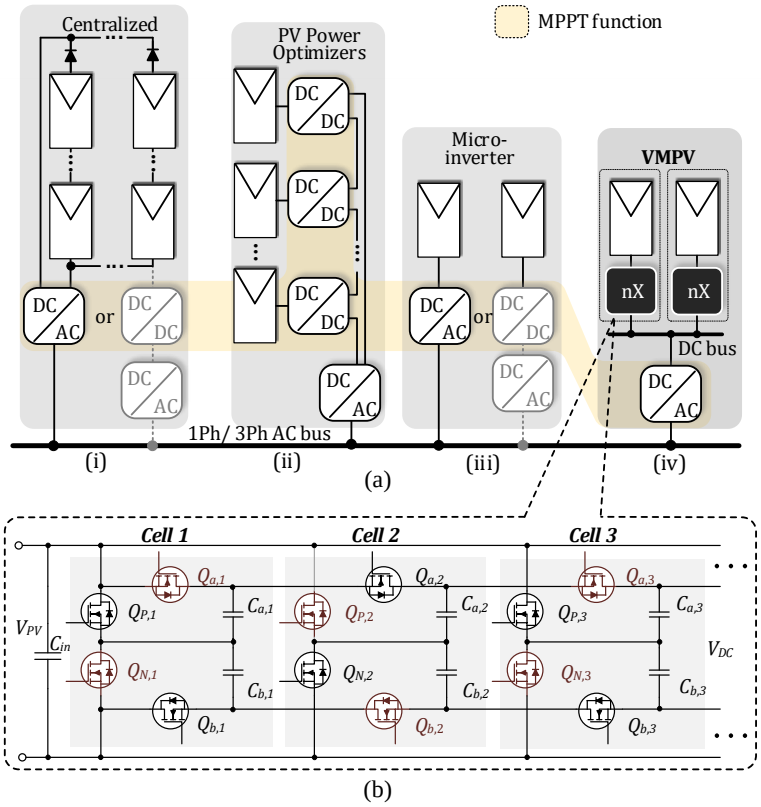


Figure 2: (a) PV architectures: *i)* central inverter, *ii)* PVPOs *iii)* micro-inverters and *iv)* the Voltage Multiplied architecture. The highlighted area indicates the converters responsible for the MPPT. (b) Schematic diagram of the magnetic-free SC voltage amplifier.

The effect of the PV module voltage amplification can be viewed as “stretching” the output I-V characteristic to higher voltages and lower currents, while keeping the produced power constant, as shown in Figure 3. The multiplication factor, *n*, should be higher than the V_{DC}/V_{MP} ratio, where V_{DC} is the required DC-link voltage for grid integration (e.g. 400 V) and V_{MP} is the nominal PV panel voltage at MPP (e.g. 40 V).

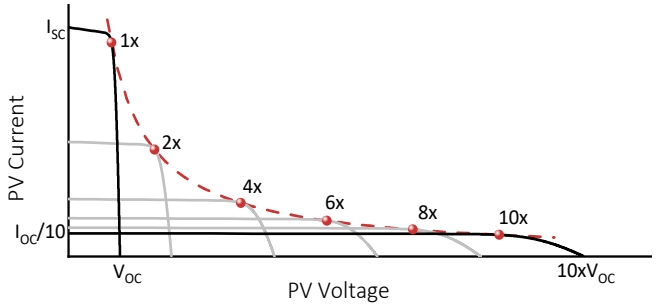


Figure 3: Modified *I-V* characteristic of the voltage multiplied PV module.

PV-Side Converter

As demonstrated in the 2018 annual report "*High-efficiency power converters for potentially-large energy-savings applications*", the nX converter combines high power density with high conversion efficiency and a fixed voltage ratio. The fixed boost ratio is not a limitation for this application, given that the maximum power point (MPP) voltage of a PV panel varies insignificantly with the environmental conditions. It should be mentioned here that the increased efficiency and power density of the nX converter come at a cost of a high transistor count. However, the latest advancements on GaN technology reveal the unique potential for monolithic integration of multiple devices on a single power chip [12], rendering this topology an ideal platform for future VMPV modules.

Our approach offers control simplicity, since all power devices are switching in a complementary pattern with a fixed 50 % duty cycle. There is no need for feed-back control loop thus, no requirements for voltage/current sensors, costly microcontrollers and communication links. A simple pulse width modulation (PWM) integrated circuit (IC) is adequate for the operation of this converter.

The power devices are subjected to low voltage and current stress, due to the modular structure of the topology. Further, the converter can operate in zero current switching (ZCS) mode, if the switching frequency is tuned to match the circuit resonance frequency, determined by the capacitors and the circuit parasitic inductances [13].

The utilization of state-of-the-art wide bandgap GaN transistors offer the option to replace the electrolytic capacitors of the circuit, which is the most common point of failure [5], [6], [14], with robust and efficient ceramic capacitors, by increasing the switching frequency of operation. This technology migration helps to achieve a long lifetime for the converter, to match that of the solar panels (above 25 years), which is an important requirement for modern PV systems. The small footprint and low driving requirements of HEMTs further contribute to the miniaturization of the micro-converter.

Gris-Side Inverter

Regulation of the operating point of a PV module, string or system is traditionally performed by the front-end converter, as indicated by the highlighted area in Figure 2(a – topologies *i-iii*). In this study, the fixed voltage ratio at the PV-side requires that the MPPT function is performed by the grid-side inverter, much like a single-stage system. Therefore, although our topology is fundamentally a two-stage system, it operates like a single-stage centralized system in terms of MPPT function, but with higher MPP tracking efficiency. Specifically, the merits of this new architecture are:

- The entire PV system has always a single MPP, even under mismatched irradiance and temperature conditions, due to the parallel connection of the VMPVs. As a result, no PV module is bypassed and the MPP is always successfully tracked, as opposed to the multi-peak P-V curves in centralized architectures, leading to almost 100% power extraction efficiency under any partial shading conditions.
- The DC-link voltage variation is limited due to the inherently small deviation of VMP with the environmental conditions. This makes it easy for the inverter to extract the maximum power while meeting the input voltage requirements, in contrast to single-stage systems under PS.
- Having a single grid-side inverter permits implementation of sophisticated control functions, such as ancillary services to the grid (e.g., fault ride through, reactive power injection, frequency regulation), as opposed to the micro-inverters that cannot afford such complexity.

3.1.2 Modelling and Simulations

Here we aim to assess the power extraction efficiency of the new PV architecture under PS conditions, against conventional PV configurations, through simulations in Matlab/Simulink. We define

the total system efficiency, η_{sys}, as the product of conversion efficiency, η_c, and extraction efficiency, η_{ext}:

$$\eta_{sys} = \eta_c \cdot \eta_{ext} \quad (1)$$

η_{ext} is given as the ratio of the average output power of the PV system to the total available power from all individual modules. Reduction of η_{ext} is usually attributed to 3 factors: (a) the shaded modules operate at a sub-optimal operating point or are completely bypassed, (b) the MPPT is trapped on a local MPP and (c) the MPPT causes oscillations around the normal operating point. For a fair comparison of the VMPV with other conventional architectures, the first factor will be considered, assuming that the MPPT algorithm can always find the global maximum, even in the case multiple power peaks at PS.

Shading Patterns

We consider two realistic shading patterns, depicted in Figure 4. Solid lines show the SP configuration and dashed lines represent the TCT interconnection scheme.

1) Shading Pattern A: Long-Narrow

In this case the shadow covers the majority of one string of a rooftop PV structure, giving rise to three irradiance intensity levels, G_1 = 900 W/m2, G_2 = 600 W/m2 and G_3 = 300 W/m2 as shown in Figure 4 (a). Ambient temperature of 20 ^{o}C and wind speed of 1 m/s are considered, according to the international standard IEC-61215. The nominal operation cell temperature (NOCT) is also included in Figure 4, considering both the photoelectrical and photothermal conversion effect.

1) Shading Pattern B: Short-Wide

This scenario concerns a façade PV system, partially shaded by the pattern illustrated in Figure 4(b). In contrast to an open rack rooftop structure, the building integrated PVs are characterized by a higher temperature, since only one side of the panel is in contact with the air.

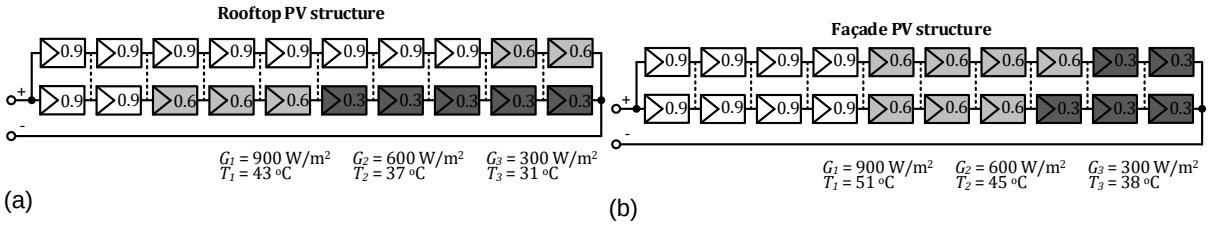
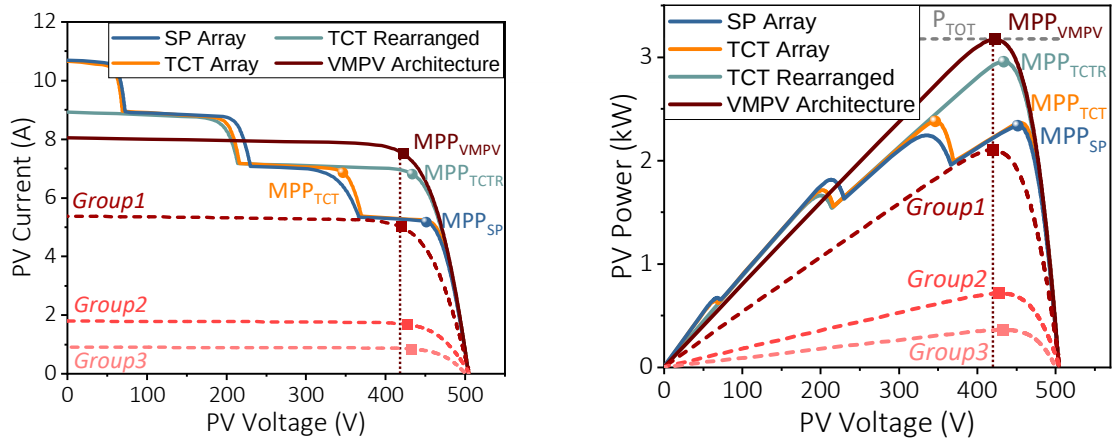


Figure 4: Indicative PS scenarios. (a) Long-narrow *shading pattern A* and (b) Short-wide *shading pattern B*.

Static Characteristics

The simulation results for the case-study A are presented in Figure 5. The grey dashed line corresponds to the maximum available power, P_{TOT}, extracted from an ideal PV architecture and is used as a benchmark in the comparison (η_{ext} = 100%). It is evident that both SP and TCT configurations exhibit poor extraction efficiencies of 73.59% and 74.94%, respectively, due to the bypassing of the shaded modules. On the other hand, the dynamic rearrangement of the panels significantly improves the efficiency to 93.12% and reduces the number of local maxima to 2. However, it is our VMPV architecture that achieves the best extraction efficiency of 99.86% with just a single global MPP.

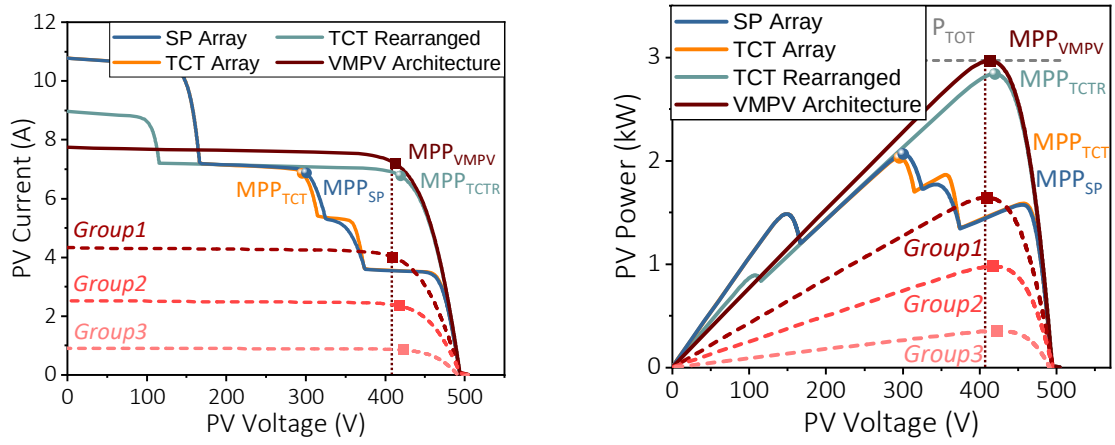
To further investigate these numbers, the *I-V* and *P-V* curves of the individual modules are show in Figure 5, classified into three groups (Group 1-3) according to the three different operating conditions. In contrast to SP and TCT (static or rearranged), the high-voltage parallel connection ensures that all PV groups operate at a common voltage (vertical dotted line) that is very close to the individual MPPs (square markers). It is worth noting that even for the highly shaded Group 3, more than 99.5% of the available power is extracted.



(a) (b)

Figure 5: (a) *I-V* and (b) *P-V* curves of the examined PV architectures under the *shading pattern A*: *Long-Narrow*. The figure also includes the output characteristics of the 3 PV groups of the proposed parallel connected VMPV system that correspond to the different irradiance levels.

The output I-V and P-V characteristics for the *shading pattern B* are presented in Figure 6. Even under these highly non-uniform irradiance and temperature conditions the VMPV architecture still exhibits a near-perfect efficiency of 99.8%. As a comparison, the SP and TCT interconnection schemes have η_{ext}(SP) = 69.4% and η_{ext}(TCT) = 68.3%, respectively, while the electrically rearranged TCT array has η_{ext}(TCTR) = 95.5%.

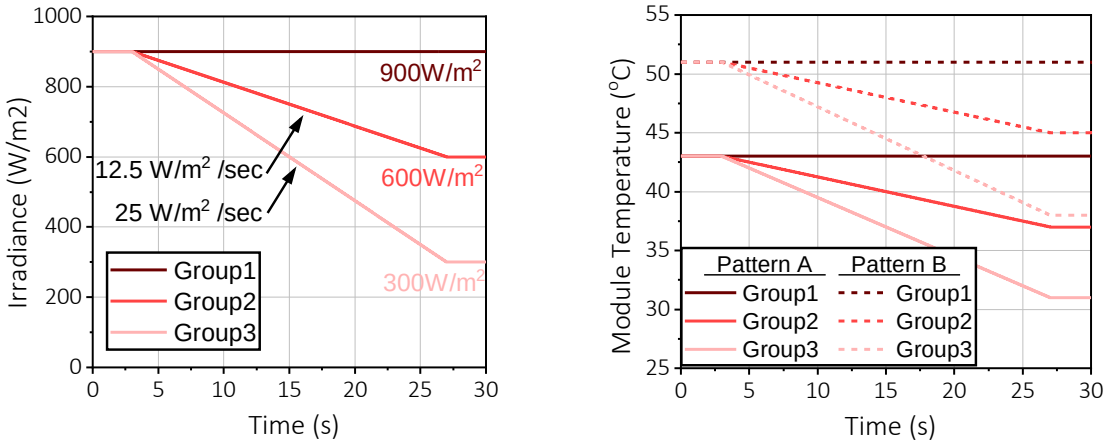


(a) (b)

Figure 6: (a) *I-V* and (b) *P-V* curves of the examined PV architectures under the *shading pattern B*: *Short-Wide*. The figure also includes the output characteristics of the 3 PV groups of the proposed parallel connected VMPV system that correspond to the different irradiance levels.

Real-time maximum power point tracking

To evaluate the time-response of the whole system under variation of the atmospheric conditions, the proposed PV architecture is connected to a single-phase grid-side inverter. The scenario where a façade PV structure is initially uniformly insolated (G_1 = 900 W/m^2) and gradually shaded to match *shading pattern B* is simulated. A linear drop of the irradiance is considered (see Figure 7), at a rate of 25 W/m^2 per second, which is a representative value for rapidly changing environmental conditions. The temperature variation of the individual PV groups is shown in Figure 7 (b), for the investigated *patterns B*.



(a) (b)

Figure 7: (a) Irradiance and (b) temperature variation with time for the 3 PV groups of the VMPV architecture. Continuous line represent the *shading pattern A* and dashed line is used for the *shading pattern B*.

The inverter control is structured in three nested control loops, as in [15]. The outer control loop is a Perturb and Observe (P&O) MPPT that is applied at the common high-voltage DC-bus and produces the reference DC-voltage, V_{DC}*. In the middle control loop, a proportional-integral (PI) controller regulates the active and reactive power reference to be injected to the grid, *P** and *Q**, respectively. A proportional-resonant (PR) current controller is implemented in the inner control loop, while the grid frequency is extracted by a second-order generalized integrator phase locked loop (SOGI - PLL).
Figure 8 shows the power and voltage variation of the proposed VMPV and standard SP architectures when the shading evolves towards *shading pattern B*. The new VMPV architecture, follows closely the benchmark curve, even when all the shaded panels have reached their steady state conditions (Time > 27 s). This scenario highlights the merits of a single MPP in the proposed parallel connection against the multiple peak formation in conventional SP configurations and the challenges in identifying the global one. Even if a sophisticated MPPT algorithm is employed that always converges to the global MPP (yellow dashed curves), the respective DC-link voltage (300V in Figure 8(b)) may be outside the inverter limits, thus not allowing operation at the MPP, leading to even lower extraction efficiency.

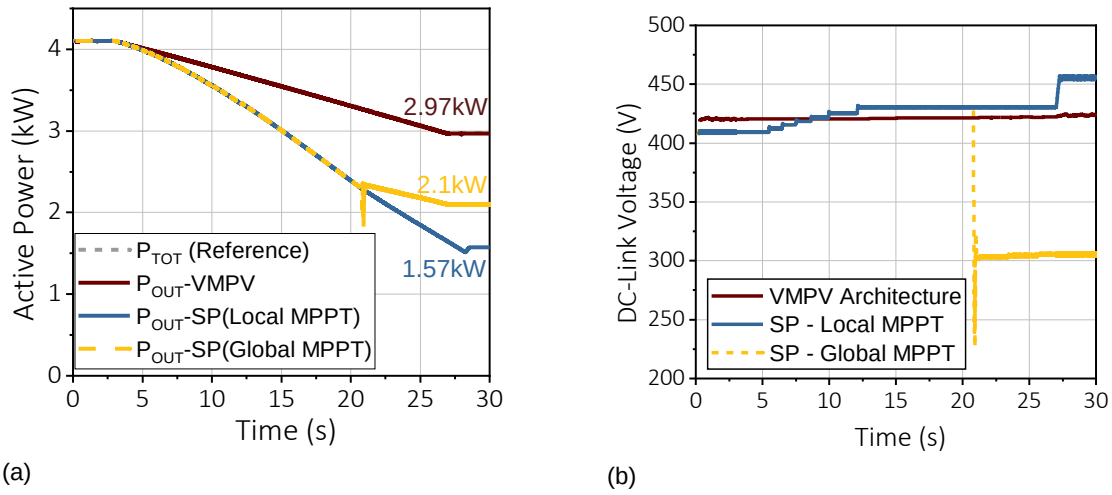


Figure 8: (a) Active power fed to the grid and (b) DC-bus voltage variation with time for the proposed VMPV under *shading pattern B*.

The simulation results show that the proposed VMPV architecture combines the best of MLPE and centralized topologies: it yields near-optimal power extraction (like MLPE, in contrast to the centralized) while allowing for sophisticated control functions in the inverter (like centralized, as opposed to micro-inverters).

3.1.3 Experimental Evaluation

Setup and shading scenarios

In order to experimentally assess our new PV architecture, two 245 WP PV modules of the same type VBHN245SJ25 are used as inputs to two nX converters that are connected in parallel at the high-voltage side, as depicted in Figure 9. Throughout the experiment, both PV panels are placed close to each other on a structure of fixed inclination with respect to the horizon. A semi-transparent fabric is used to cover one PV module completely and uniformly to emulate PS conditions.
A DC-DC converter that performs all control functions, including scanning of the PV curves and MPPT, feeding a resistive load was used as a simple substitute of the grid-tied inverter. This setup allows safe and repetitive testing of the new architecture, while the results are also valid for the grid-connected system. The switching frequency of the buck converter was set to 20 kHz and the MPPT period to 250 ms. All voltage and current measurements were continuously monitored with a sampling rate of 4 kSamples/s and then filtered via a digital low-pass filter (LPF) with a cutoff frequency of 100 Hz to reject the switching noise. The key components and parameters of the experimental setup are summarized in TABLE II.

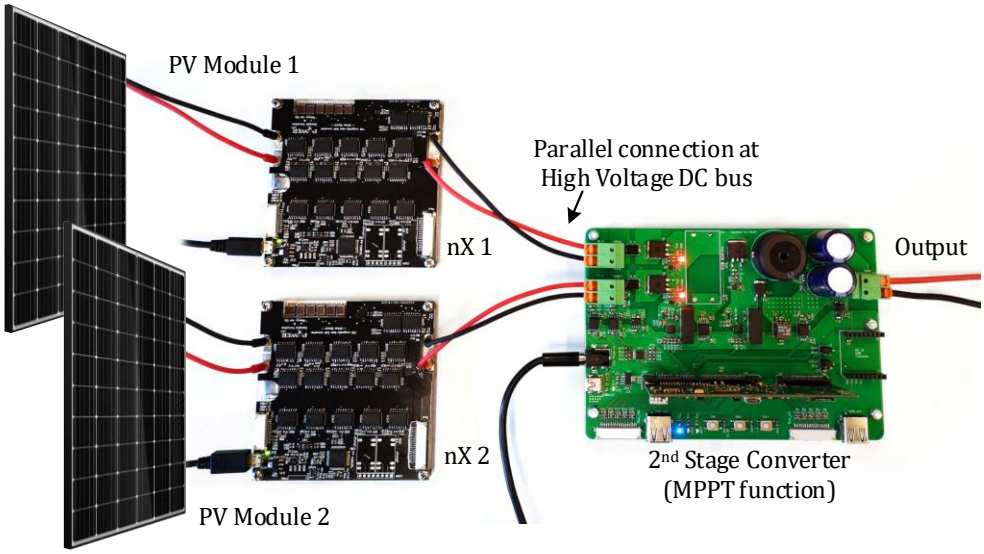


Figure 9: Experimental setup consisting of two identical PV modules along with their 10X voltage multipliers, a secondary-stage converter performing the MPPT function feeding a resistive load.

TABLE II

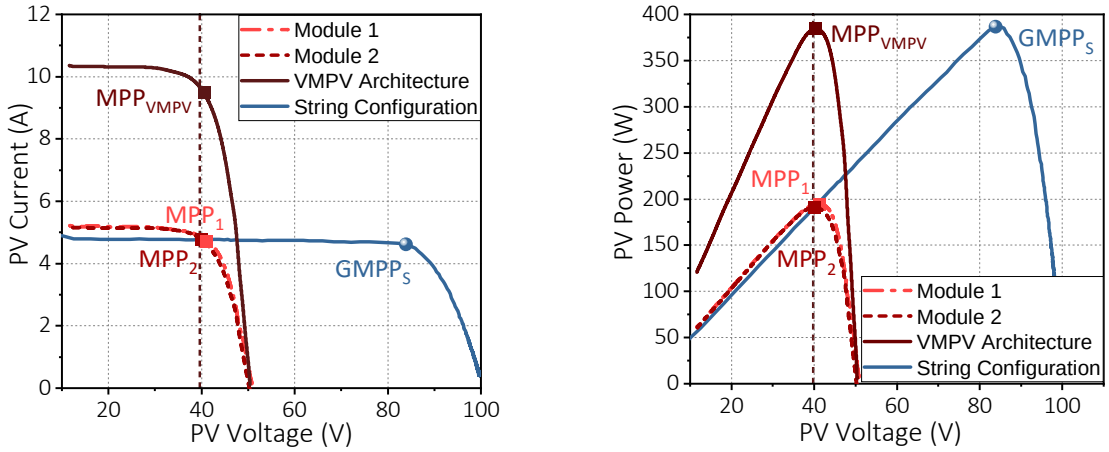
List of Components of the Experimental Setup

Component	**Parameter**	**Value**
PV Modules	Part Type	VBHN245SJ25
	V_{MP}	44.3V
	I_{MP}	5.53A
	V_{OC}	53V
	I_{SC}	5.86A
Module -level nX converter	Transistors in $Q_{P/N}$ position	GS61008T
	Transistors in $Q_{a/b}$ position	GS66508T
	Switching Capacitors	4x2.2uF, X6S
	Gate Driver	LM5114
	Digital/Power Isolator	ISOW7842F
2nd-stage DC-DC converter	Series Diodes	S10KC
	$L_{DC\text{-}DC}$	1.5 mH
	$C_{DC\text{-}DC}$	50 µF
	Transistor	IPB65R190CFD
	Switching Diode	C3D08065E
	Microcontroller	TMS320F28379D
	Switching Frequency ($F_{SW\text{-}B}$)	20 kHz
	MPPT period (T_{MPPT})	250 ms
	Voltage/Current sampling rate	4 ksamples/s
	LPF cutoff frequency (F_0)	100 Hz
Output Resistor	R_{out}	0-240 Ω

Static Characteristics

The *I-V* and *P-V* characteristics of the proposed PV system were recorded in two shading patterns: A) uniform irradiance and temperature conditions and B) partial shading, where one panel is uniformly shaded while the other one remains unshaded. The curves are captured by slowly changing the operating point within 5 sec (scanning).

Figure 10 shows the characteristic curves of the two individual PV modules (dashed and dash-dotted lines) and the combined curve of the proposed VMPV architecture (solid red line), under uniform irradiance and temperature conditions. The two modules are not identical and their MPPs (MPP1 and MPP2) differ by 3.4 W and are spaced by 1.17 V. However, the power loss of the VMPV approach is just 0.4 W, resulting in an excellent extraction efficiency of 99.9%. In fact, both modules operate at 99.9% of their respective MPPs.



(a) (b)

Figure 10: Experimentally extracted (a) *I-V* and (b) *P-V* characteristics of the PV modules under the *shading pattern A*: uniform irradiance and temperature conditions. Values were measured at the PV side for both VMPV and string architectures.

Figure 11 shows the experimentally extracted *I-V* and *P-V* traces under the *Shading Pattern B*: Module 1 is entirely shaded, while Module 2 remains unshaded. Although P_{PV}(MPP1) = 48.7 W is more than 3.5 times smaller than P_{PV}(MPP2) = 174.9 W, their respective voltage difference is just 1.45 V. That leads to an extraction efficiency of 99.74% for the VMPV system. On the other hand, the global MPP of the series connection is P_{PV}(GMPPS) = 174 W, equal to MPP2 minus the power dissipated at the bypass diode of Module 1, resulting in a extraction efficiency of just 77.8%. Still, it is highly possible that a simple MPPT algorithm would converge at a local MPP (LMPP), in which case half of the PV power would be lost (η_{ext}(LMPPS) = 50.5%).

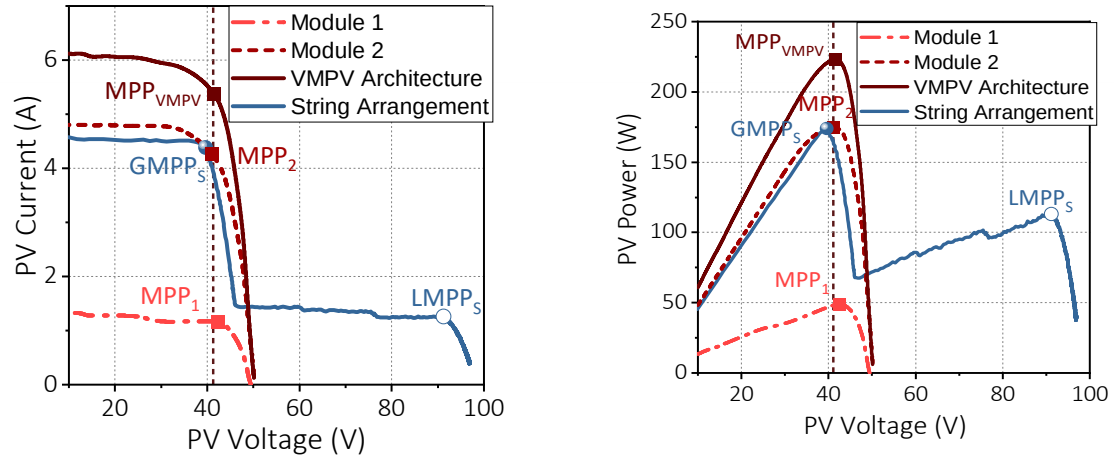


Figure 11: Experimentally extracted (a) *I-V* and (b) *P-V* characteristics of the PV modules under the *shading pattern B*: PS conditions. Values were measured at the PV side for both VMPV and string architectures.

3.1.4. Real-time maximum power point tracking

For this experiment, a P&O algorithm was executed by the second-stage converter, with a period of 250 ms and an MPPT duty cycle step of 1%. The two PV modules were subjected to the two shading patterns of the previous subsection (uniform and PS conditions). Figure 12 shows the output power and DC-bus voltage variation under real time tracking of the MPP. The MPPT algorithm always converges to the single MPP, guaranteeing near-perfect extraction efficiency at any conditions and effectively addressing the tracking challenges of SP configurations. In addition, the DC-link voltage is insignificantly affected by PS (only 3% deviation), which allows for a narrow predetermined input voltage range for the grid-side inverter, in contrast to the single-stage PV systems.

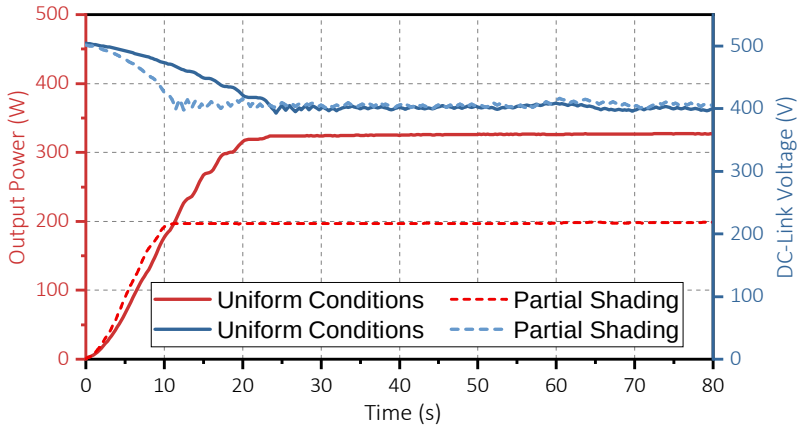


Figure 12: Response of the new VMPV architecture during real time MPPT, under uniform and PS conditions. Output power (in red) and DC-bus voltage (in blue) variation with time.

3.1.4 Discussion and Future Work

Our goal was to demonstrate a highly efficient architecture for residential grid-connected PV systems to increase the energy yield from DEGs. Through the parallel connection at the output of a fixed-ratio high step-up nX converters we managed to eliminate the partial shading challenges of typical series connections and delivering almost 100% extraction efficiency. At the same time, the nX converter features a high flat conversion efficiency of more than 96.3% irrespective of the power level, leading to better total system efficiency at partial shading than most centralized and distributed PV architectures.

The use of GaN HEMTs in the developed magnetic-less nX converters allow for longer-lifetime ceramic capacitors in place of the conventional bulky electrolytic capacitors. This along with the omissions of all magnetic components and the low cooling requirements lead to a very compact solution that can be integrated to the backside of the PV panel, forming a new voltage-multiplied PV module.

All control functions, including MPPT, are transferred to the inverter, simplifying the DC-DC micro-converter requirements for microcontrollers and voltage/current sensors. The high-voltage parallel connection results in small variation of the DC-link voltage with the environmental conditions, which in turn simplifies the requirements for the grid-side inverter, as in two-stage string inverters.

Our proof of concept has been validated through simulations and experimental testing. However, the converter prototype is not yet optimized, in terms of power transfer capability and efficiency. In fact, the current version of the converter is oversized to handle 2.5 kW and occupies 0.1 litters of volume. The system can further be improved by using low-voltage rating HEMTs, with lower on-resistance and smaller footprint, that would improve the conversion efficiency and increase the power density. Additionally a soft-star-up circuit needs to be integrated to ensure reliable operation during power-up and shut-down.

Meeting these future goals will bring us one step closer to commercialization of the developed system. Our new approach offers a promising alternative to an already huge PV market.

3.2 Thermal management

As shown previously, the key enabling factor for high power density converters is the utilization of state-of-the-art GaN devices, which exhibit low specific on-resistance and high breakdown electric field [16], [17]. However, the increased switching frequencies and reduced die sizes cause high heat fluxes, surpassing 1 kW/cm^2 [18], [19], which is far beyond the capabilities of conventional cooling methods [20]. Inadequate cooling of these devices causes high junction temperature which degrades their performance and reliability [21], [22].
The thermal challenges become more pronounced in converter topologies with a large number of active components, such as modular [23], [24] and composite topologies [25]. Uneven temperature rise over multiple devices causes hotspots that limit the system performance. Several modular air-based cooling topologies have been presented to cool down converters with a large number of components in a small form factor [26], [27], but the low heat transfer coefficient of air ultimately limits heat fluxes to roughly 300 W/cm2 [20]. To achieve higher power density in topologies with a large number of components, high-performance cooling techniques, such as liquid cooling, are required to surpass this limit.
Several high-efficiency liquid cooling strategies have been proposed for cooling of individual power devices, such as impinging coolant on the device [28], [29], as well as flowing coolant through microchannels [30]. The latter can result in state-of-the-art heat fluxes, due its large surface area and high heat transfer coefficient [31]. However, microchannels typically suffer from high pressure drop. Approaches to reduce the pressure drop over microchannel heat sinks have received considerable attention [32]. A promising approach is the use of a manifold structure to distribute the flow over the microchannels [33]. This manifold microchannel (MMC) structure reduces the pressure drop, increases the temperature uniformity as well as a higher heat transfer [34], [35]. However, although these MMC heat sinks demonstrated in the literature have outstanding capabilities for high heat flux management [36]–[38], the complicated fabrication procedure, consisting of multiple bonding steps, has prevented large-scale adoption of this technology.
Consequently, there is currently no standard thermal management solution that can be mounted on a converter, like conventional heat sinks, while providing the high cooling performance of microchannels simultaneously to all active devices.

Within this project **we propose a novel compact and energy-efficient microfluidic cooling system for power converters with multiple power devices by mounting microchannel cold-plates on each device.** The high pressure drop usually associated with microchannels was minimized using a customized compact flow distribution manifold that connects these microfluidic heat-sinks in parallel to a common inlet and outlet. A model was developed to determine the optimal microchannel and manifold geometry that maximizes cooling capability and minimizes the required pumping power. Cold-plates were fabricated on silicon using standard clean-room processes, but could easily be replaced by high-throughput fabrication methods such as micro-deformation processes. We demonstrate flow distribution manifolds realized using 3D-printing as well as conventional fabrication methods to demonstrate the possibility of their mass-production in a cost-effective way. The thermal and hydraulic performance of the heat sink is experimentally evaluated and the cooling module, consisting of 20 silicon microchannel cold-plates, is demonstrated on the 2.5 kW switched capacitor converter, to demonstrate the potential of this new cooling system and its impact on power density. This proposed - method provides high performance microchannel cooling in a very compact form-factor with low pressure drop, making it a promising technology for future power converters.

3.2.1 Modelling, Design and Fabrication

Here we derive the analytical expressions that describe the hydraulic and thermal performance of the heat sink, which are used to optimize the heat sink geometry for energy-efficient cooling. First, the cooling performance of an individual cold-plate is evaluated to obtain an optimum design, followed by the design and fabrication of the distribution manifold

Micro-channel Cold Plates

A schematic overview of the proposed cooling method is shown in Figure 13. A packaged device is mounted on a printed circuit board and cooled by a microchannel cold-plate attached on top of the device, separated by a thermal interface material (TIM). We investigate the situation where all dissipated power travels upwards to the microchannel cold-plate, which is the case if the device has a relatively low junction-to-case thermal resistance to the top of the device, and a high junction-to-board thermal resistance.

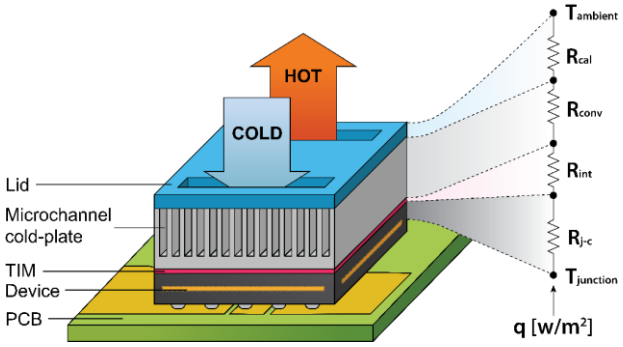


Figure 13: Schematic cross section of a transistor, cooled by a microchannel cold-plate, and an equivalent thermal resistance model.

The cooling efficiency is described by the Coefficient of Performance (*COP*), given in (1), defined as the ratio of dissipated power in the in the system, $Q_{max,}$ to the pumping power required, P, to keep the junction at a given maximum junction temperature, ΔT_{max}. The pumping power, defined in (2), is the product of the flow rate, f, and the pressure drop Δp. R_{tot} is the total thermal resistance between the junction of the device and the inlet temperature of the coolant, which relates the heat losses to temperature rise according to (3). It is clear that to increase COP, the pressure drop, flow rate and thermal resistance have to be reduced. However, these values are interdependent, so to determine the optimal microchannel geometry, relations between pressure drop, thermal resistance and flow rate are required.

$$COP = \frac{Q_{max}}{P} \tag{1}$$

$$P = f\Delta p \tag{2}$$

$$\Delta T_{max} = Q_{max} R_{tot} \tag{3}$$

The total thermal resistance, R_{tot}, is the sum of the 4 components shown in the one-dimensional thermal resistance network in Figure 13.

- The *caloric thermal resistance* of the coolant, R_{cal}, given in (4), describes the temperature rise of the coolant between the inlet (T_{in}) and the outlet (T_{out}) and depends on the flow rate, f, the fluid density, ρ, and heat capacity, C_p.
- The *junction-to-case thermal resistance* of the device, $R_{j\text{-}c}$, is given by the device manufacturer and
- the *thermal interface resistance*, R_{int}, depends on the type of TIM used.
- the thermal resistance of the cold-plate is modeled as only a *convective thermal resistance*, R_{conv}, as expressed in (5), since the conduction component is negligibly small (<0.01 K/W) due to the high thermal conductivity of silicon. h is the heat transfer coefficient and A is the total surface area of the microchannels.

Using the fin model, previously described in [31], [39]–[41], an expression was derived for the convective thermal resistance, as shown in (5). The geometry of a microchannel is described by the channel width and fin width. We define w as both the channel and fin width, which simplifies the analytical expressions. z is the channel depth and Nu is the Nusselt number. ϵ is the fin efficiency,

calculated using (6), where k_s is the thermal conductivity of the heat sink material and k_f the thermal conductivity of the fluid.

$$R_{cal} = \frac{T_{out} - T_{in}}{Q_{max}} = \frac{1}{\rho C_p f} \tag{4}$$

$$R_{conv} = \frac{1}{hA}\epsilon^{-1} = \left(1 + \frac{z}{w}\right)^{-1} \frac{w}{LWk_f Nu}\epsilon^{-1} \tag{5}$$

$$\epsilon = \tanh\left(z\sqrt{\frac{2h}{k_s w}}\right)\left(z\sqrt{\frac{2h}{k_s w}}\right)^{-1} \tag{6}$$

The required flow rate to keep the junction temperature rise at ΔT_{max} can be calculated using (7). The relationship between pressure drop and flow rate in the microchannel cold plate can be expressed in terms of a hydraulic resistance, r_h. Considering a cold-plate with N parallel channels, the pressure drop can be calculated using (8) [42]. Combining equation (1)-(8) results in (9), an expression to calculate COP given a certain geometry and heat load. Eq. (9) shows that the coolant requires a high ratio of $\rho^2 C_p{}^2/\mu$, which makes water a good candidate.

$$f = \left(\rho C_p\left(\frac{\Delta T_{max}}{Q_{max}} - R_{conv} - R_{int} - R_{j-c}\right)\right)^{-1} \tag{7}$$

$$\Delta p = r_h f = \frac{12\mu L}{N(1 - 0.63w/z)w^3 z} f \tag{8}$$

$$COP = \frac{\rho^2 C_p^2 Q_{max}}{r_h}\left(\frac{\Delta T_{max}}{Q_{max}} - R_{conv} - R_{int} - R_{j-c}\right)^2 \tag{9}$$

Using the aforementioned model, we studied the effect of channel size on the cooling performance of silicon microchannel cold-plates with channel depth z fixed at 400 µm and channel width w varying between 10 µm and w = 300 µm. Water was chosen as coolant and a typical value of 0.5 K/W was chosen for both R_{int} and $R_{j\text{-}c}$ [43]. Figure 14 shows the calculated COP versus maximum dissipated power for microchannel cold plates. All curves show the same trend: COP decreases with increasing power due to the higher flow speed required to keep the temperature rise between the junction and the inlet temperature equal to ΔT_{max} = 60 ºC. After a certain power, a sharp cutoff in COP is observed due to the excessively high flow rates. Reducing the microchannel width results in an increase in Q_{max} at which this cutoff occurs, because of the reduced R_{conv}, however, at the cost of a lower COP at lower heat loads. For example, 25 µm channels can extract approximately a 5-time higher heat load than 200 µm channels but have a 10 times lower COP at low heat loads. For the nX converter described here, Q_{max} was estimated at 35 W, making 50 µm channels the favorable design.

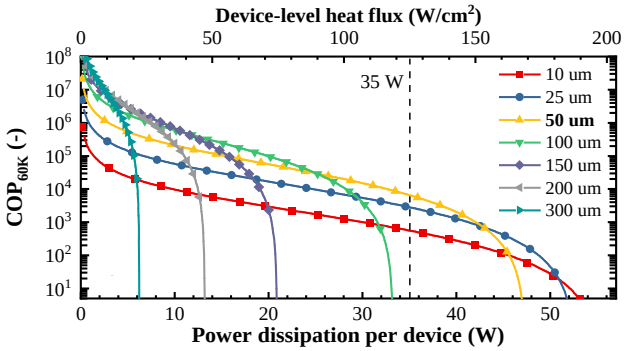


Figure 14: Calculated COP versus maximum power dissipation per transistor (Q_{max}) cooled using the proposed microchannel cold-plate for channel widths varying between 10 µm and 300 µm, considering a maximum temperature rise ΔT_{max} of 60 ºC.

Microchannel cold-plates were fabricated on a 4-inch silicon wafer in the EPFL CMi cleanroom facilities, as illustrated in Figure 15(a). A 2 µm-thick layer of SiO_2 was deposited using plasma-enhanced chemical vapor deposition, which functions as a hard mask for dry-etching. Channels with widths between 25 µm and 100 µm were defined using photolithography followed by a dry-etch of the SiO_2 using C_4F_8 chemistry. Finally, 400 µm-deep vertical channels were etched in silicon using the Bosch deep reactive-ion etching process. Inlet and outlet ducts were 1 mm by 7 mm rectangular openings. Figure 15 (b) shows a scanning electron microscope (SEM) image of the microchannels after etching. As a final step, the wafer was diced into individual 9 mm by 9 mm cold-plates, shown in Figure 15 (c).

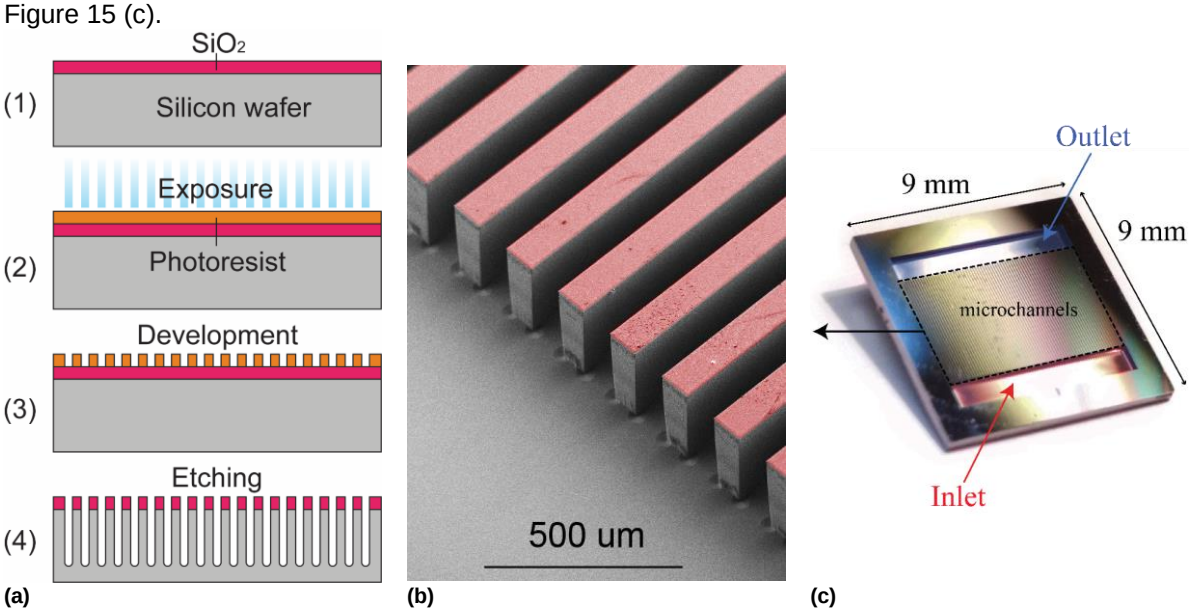


Figure 15: (a) Fabrication process of the silicon microchannel cold-plates. (b) SEM image of the microchannels after etching, where false coloring indicates the presence of SiO_2 (c) Picture of the cold-plate after dicing.

Manifold

contact with the transistors on the PCB. Individual cold-plates can either be connected in series or in parallel. A series connection guarantees a consistent flow rate over all cold-plates, but suffers from a significantly higher pressure drop, as well as a higher temperature rise of the water at an identical flow rate. For this reason, it is favorable to parallelize the cold plates, as illustrated in Figure 16 (a). A careful manifold design is required to ensure an equal fluid distribution over all cold-plates and avoid local overheating [44], [45].

The cold-plate manifold was modeled as a network of resistors, illustrated in Figure 16 (b), where each resistor represents the hydraulic resistance of a specific part of the flow path. The hydraulic resistance of each cold-plate, r_{CP}, can be determined using (8), while the hydraulic resistance of the manifold inlet and outlet sections, $r_{M,}$ calculated using (10). This equation gives the pressure drop of a square manifold channel section with cross-section w_M and length L_M [42]. The currents $I_{CP,i}$ flowing through the resistors represent the flow rate in the cold-plates. Good flow uniformity can be guaranteed if r_{CP} is significantly larger than the sum of the hydraulic resistances over the manifold section. The percentage of variation of current from the mean, E_i, represents the flow non-uniformity, defined according to (11), which is used to assess the quality of the manifold design. A good design should have a low value of $E_{i,}$ such that the liquid is equally distributed over all cold-plates.

$$r_M = \frac{12\eta L_M}{0.42\, w_M^4} \tag{10}$$

$$E_i = \left| \frac{20 \cdot I_{CP,i}}{\sum_{j=1}^{20} I_{CP,j}} \right| - 1 \tag{11}$$

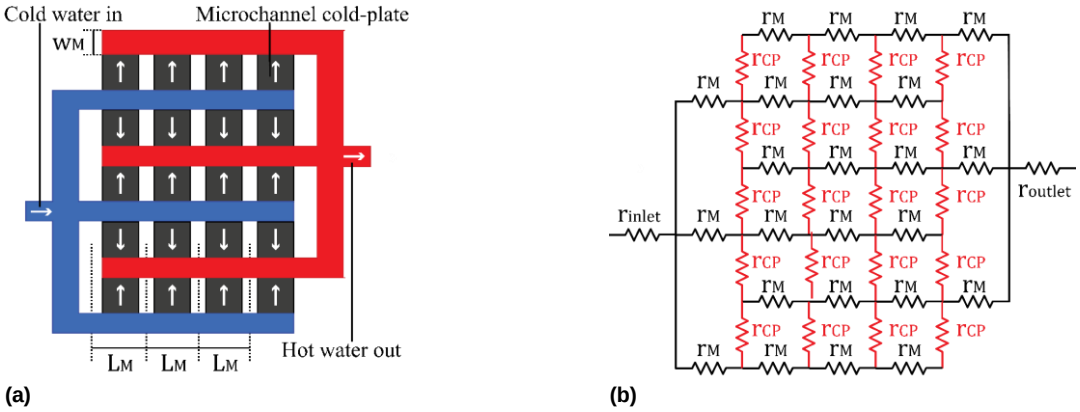


Figure 16: (a) Illustration of the liquid flow through the manifold. (b) An equivalent hydraulic resistance network of the manifold and the microchannel cold plates.

We investigated the flow uniformity of a manifold delivering coolant to a 4 x 5 grid of transistors, using microchannel cold-plates with the following characteristics: N = 80, w = 50 µm and z = 300 µm, L = 6 mm. The manifold had equal section length L_M of 2 cm and their cross-section w_M was varied from 0.5 mm to 3 mm to study its impact on the flow uniformity. *LTspice* was used to calculate the currents in the resistor network, which corresponds to the flow distribution through all 20 cold-plates. Figure 17 shows the percentage of flow non-uniformity, which strongly depends on the manifold channel size. For w_M = 0.5 mm, the flow rate non-uniformity is above 100%, whereas for w_M = 2 mm the non-uniformity is limited to approximately 1%. This result clearly shows the importance of properly sizing the manifold for obtaining a uniform distribution of coolants to the cold plates.

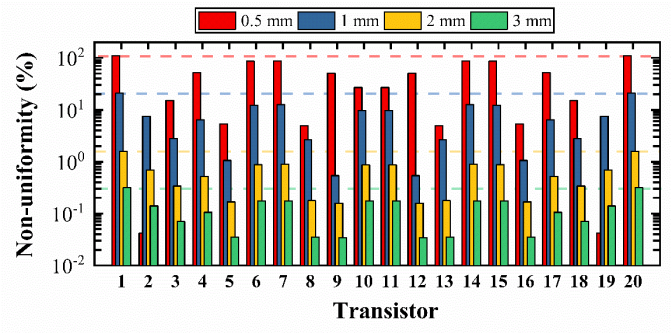
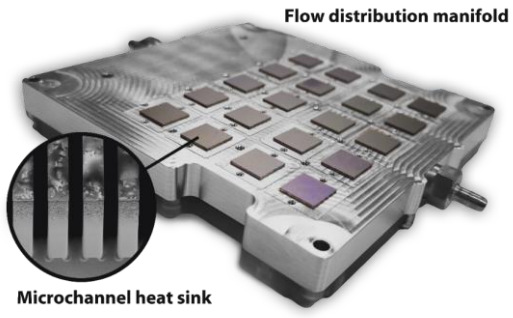


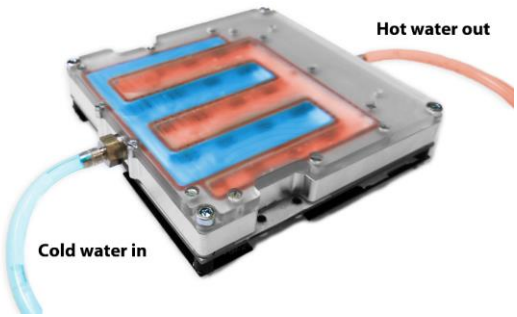
Figure 17: Flow rate non-uniformity for manifold cross-section width w_M varying from 0.5 mm to 3 mm, defined as the percentage of absolute deviation of flow rate from the mean for all 20 cold-plates.

Two flow distribution manifolds were fabricated based on the design rules from the previous simulation. The first manifold, shown in Figure 18 (a), was realized using Computer Numerical Controlled (CNC) machining and consists of three pieces: an aluminum body, a polycarbonate lid and a silicone gasket to provide leak-tight seal. This simple design can be easily fabricated by injection molding for low-cost mass manufacturing. The bottom side of the manifold contains 40 slits connected to the inlet and outlet of 20 silicon microchannel cold plates. The cold-plates were connected to the manifold using a water-resistant double-sided adhesive, which was laser-cut to size. Figure 18 (b) shows the top side of the manifold where the red and blue colors indicate the hot and cold water, respectively.

A more compact manifold was fabricated using stereolithography (SLA) 3D printing. The possibility to 3D print the manifold is very interesting for rapid prototyping together with the electronic design. This way, the geometry of the cold-plate defines the cooling performance whereas the manifold defines the distribution of the coolant. Additionally, by removing the constraints of conventional fabrication methods, more compact designs can be realized. A network of overlapping inlet and outlet channels was designed, shown in the computer-aided design (CAD) model of Figure 18 (c), where the blue and red colored sections indicate the hot and cold water, respectively. Such a design cannot be realized using conventional CNC machining, but additive manufacturing enables the realization of such a monolithic structure. High temperature resist was used (EnvisionTEC HTM140) which can withstand temperatures up to 140 ºC. The sidewalls of all channels were angled at 45 degrees to print the structure without internal support material, as this would be impossible to remove from the monolithic structure. Figure 18 (e) and (e) show the manifold after printing. The slits visible in Figure 18 (c) connect to the inlet and outlet of the silicon microchannel cold-plates. The total volume of this manifold is only 35 cm^3.



(a)



(b)

(c) **(d)** **(e)**

Figure 18: (a) Bottom side of the Aluminum CNC-machined manifold with 20 silicon microchannel cold plates and (b) top side with a polycarbonate lid. (c) CAD model of the 3D-printed manifold (d) Top side of the manifold after 3D printing. (e) Bottom of the manifold which shows the slits that connect the manifold to the microchannel cold-plates.

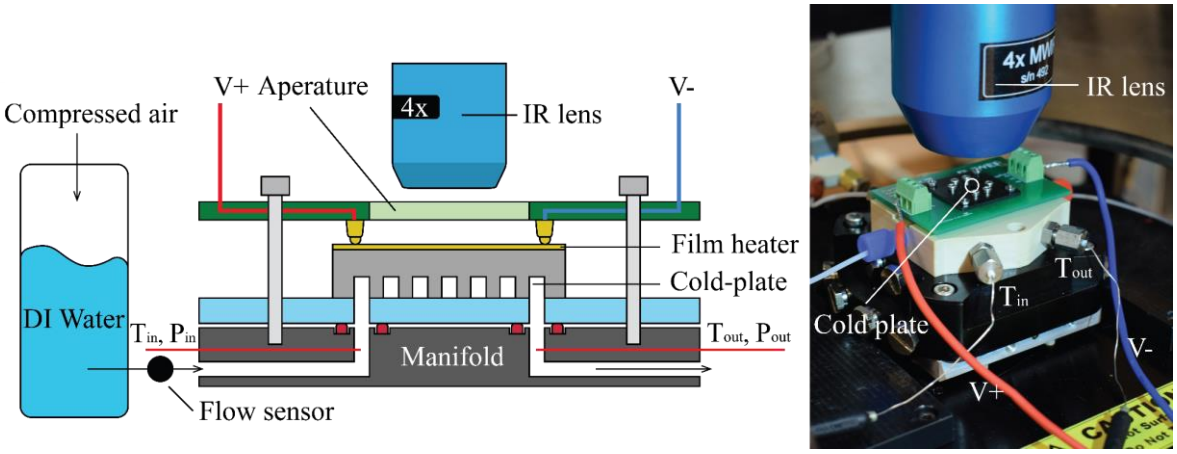
3.2.2 Experimental Evaluation

Micro-channel Cold Plates

A test setup was developed to experimentally investigate the performance of microchannel cold-plates of various channel dimensions. This setup, illustrated in Figure 19 (a), contains a pressure regulator that pressurizes a reservoir with deionized (DI) water. The DI water flows, through a flow meter into the test section that contains an individual microchannel cold-plate. This test setup includes 2 calibrated thermocouples that measure the water temperature before and after the cold-plate and a pressure sensor to determine the pressure drop over the cold-plate.

To investigate the properties of each individual cold plate in this setup, a thin metal film was deposited on the backside of the cold-plate by electron-beam physical vapor deposition to function as a resistive heating element emulating the power dissipated by each transistor. This heating element allows an easy variation of the dissipated power, and the absence of R_{int} and $R_{j\text{-}c}$ enables an accurate measurement of the convective thermal resistance.

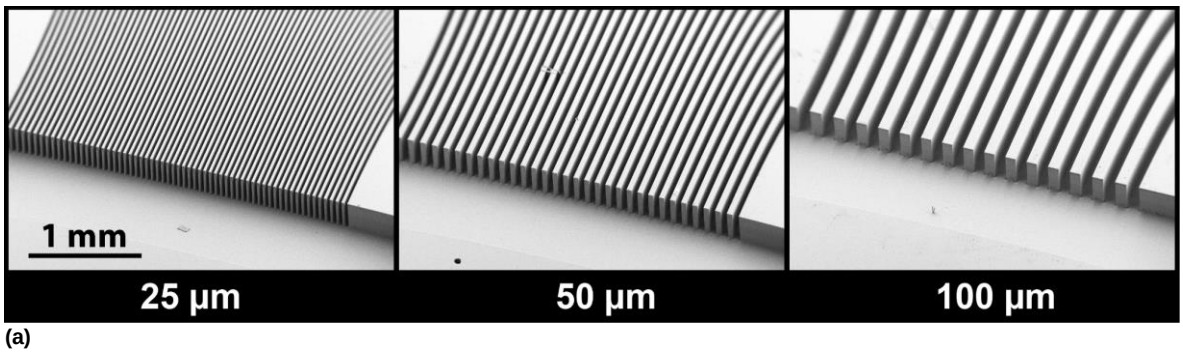
A PCB connected the heating element to a regulated power supply and the temperature at the surface of the cold-plate was measured using an infrared (IR) microscope. The IR microscope was pixel-by-pixel calibrated by flowing water at various fixed temperatures through the cold-plate using a thermostatic bath. Power dissipation was determined using an energy balance to account for any heat that leaks out of the setup by convection to the ambient or by conduction through the test section. This calculated power was within 95% of the total dissipated electrical power, which confirms a sufficiently isolated test setup. Thermal resistance was determined by taking the slope of the surface temperature rise versus power dissipation.



(a) (b)

Figure 19: (a) Schematic illustration of the cooling performance evaluation setup. (b) Picture of the test section underneath an IR camera.

Figure 20 (a) shows SEM images of the 3 cold-plates evaluated in this study (w_c = 25 µm, 50 µm and 100 µm). The experimental temperature rise between the surface of the cold-plate and the inlet temperature of the coolant versus power dissipation for these cold-plates at a flow rate of 1 ml/s is shown in Figure 20 (b). The slope of the linear fit through these measurement points gives the thermal resistance, R. The experimental COP is shown in Figure 20 (c) along with lines corresponding to the analytical model from (9), confirming that smaller sized channels can handle higher heat loads more efficiently. A reasonable match between the experimental results and the model was obtained, which validates our initial design approach. Based on the experimental results, R_{conv} was determined to be approximately $3.3 \cdot 10^{-2}$ cm^{2}K/W, $6.9 \cdot 10^{-2}$ cm^{2}K/W and $1.1 \cdot 10^{-1}$ cm^{2}K/W for w_c = 25 µm, 50 µm and 100 µm, respectively.



(a)

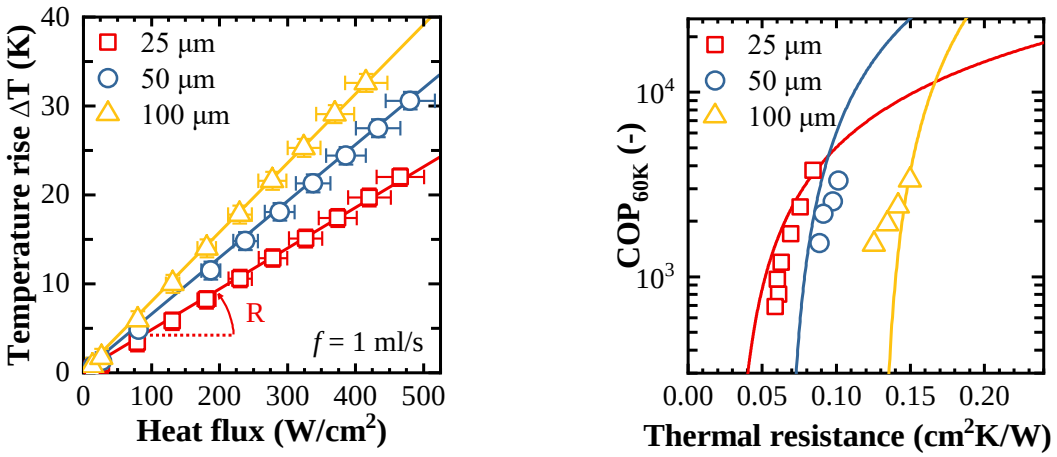


Figure 20: (a) SEM images of the 3 evaluated microchannel cold-plates. (b) Temperature rise between the inlet temperature of the coolant and the surface of the cold-plate versus heat flux. Slope of the linear fit through the data points indicates the thermal resistance, R. The coolant inlet temperature was 25 °C. (c) COP versus thermal resistance. Experimental measurements are indicated by the markers and the lines indicate the results using the analytical model.

Manifold

The hydraulic performance of the heatsink was measured using pressure sensors mounted inside the inlet and outlet manifold region. Figure 21 hows the experimentally observed pressure drop versus flow rate, as well as the predicted pressure drop based on the analytical model in (8). As indicated before, (8) neglects the pressure drop due to the inlet and outlet contraction and expansion, as well as any developing flow phenomena. The measured flow resistance was 15.7±0.51 mbar·s/cm^3, compared to a predicted 13.0 mbar·s/cm^3 based on the analytical model.

The exact power dissipation per transistor must be known to determine the total thermal resistance. For this purpose, the converter was operated such that all transistors were operating in continuous conduction mode, and all power was equally dissipated over the 20 transistors. By sweeping the power dissipation and measuring the temperature rise of the device, the thermal resistance was obtained from the slope of temperature rise versus power dissipation. This measurement was repeated for multiple flow rates, to isolate the flow rate-dependent caloric resistance (R_{cal}) from the fixed geometry-dependent thermal resistance (R_{conv} + R_{int} + $R_{j\text{-}c}$). By combining this information with the previously determined R_{conv}, and the datasheet values of $R_{j\text{-}c}$, we estimated all thermal resistances in our system, which is valuable for optimization purposes.

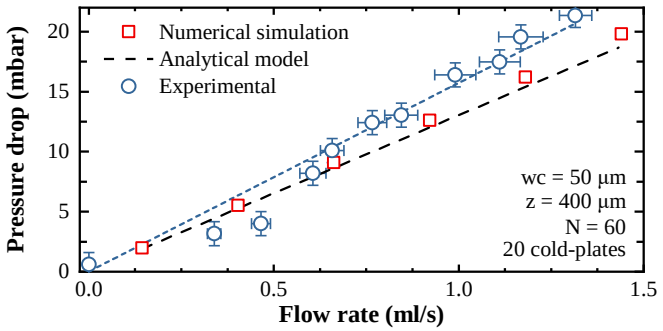
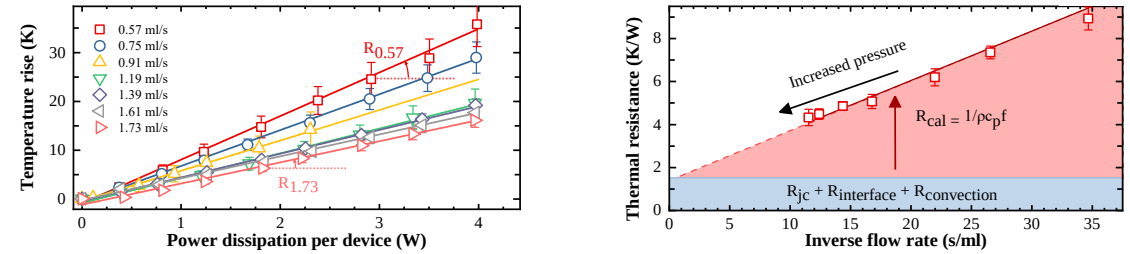


Figure 21: Experimentally observed and predicted pressure drop versus flow rate of the manifold heat sink. Analytical prediction was based on (9), considering fully developed laminar flow without inlet and outlet effects.

Figure 22(a) shows the temperature rise between the device and the inlet temperature of the coolant versus power dissipation per device. The temperature rise shows a linear relationship with dissipated power, the slope of which represents the thermal resistance. The thermal resistance was determined for 7 flow rates, between 0.57 ml/s and 1.73 ml/s. The flow rate dependent thermal resistances, extracted from the slope of the curves in Figure 22(a), are plotted in Figure 22(b). The contribution of the thermal resistance marked in red indicates the caloric thermal resistance, showing a clear f^{-1} relation ($R_{cal} = 1/\rho C_p f$). The contribution marked in blue in Figure 22(b) corresponds to the fixed part of the thermal resistance ($R_{conv} + R_{int} + R_{j\text{-}c}$), which is approximately 1.45±0.086 K/W, which corresponds to the predicted thermal resistance at infinite flow speed. The junction to case thermal resistance is provided by the manufacturer (0.55 K/W) and the convective thermal resistance was determined in the previous section to be approximately 0.25 K/W, corresponding to a base-effective heat transfer coefficient of $1.4 \cdot 10^5$ W/m^{2}K. We can now deduce that the interface thermal resistance is approximately 0.65 K/W.



(a) (b)

Figure 22: (a) Temperature rise versus power dissipation. Lines indicate a linear fit and the slope gives the total thermal resistance. Flow rates are combined values for all 20 devices, whereas power dissipation was measured per device. (b) Thermal resistance versus flow speed per cold-plate. The red area indicates the caloric thermal resistance, R_{cal}, whereas the blue part under the curve is the fixed part of the thermal resistance at a theoretical infinite flow rate.

Figure 23 (a) shows the experimentally obtained COP versus the power dissipation per device for ΔT_{max} = 60 K. The dashed line corresponds to the analytical model of (9). As can be seen, a reasonable correspondence was obtained between the two, thus validating the modeling and optimization approach. The slightly lower COP at higher power levels can be accounted to a higher pressure drop at high flow rates than predicted by the model. Figure 23 (b) shows the required pumping power at different expected loading of the converter, based on a 94% efficiency of the converter and assuming an equal distribution of losses. Based on these assumptions, up to 5 kW of transferred power can be delivered while requiring less than 50 mW of pumping power. Figure 24 shows and overview of commercially available pumps in the low-power range. The high COP and resulting low pumping power requirements enables the use of small piezoelectric micropumps which helps achieving high system-level power density. For a maximum device temperature rise of 60 K, a predicted 41 W per transistor could be cooled down using this approach, which corresponds to a combined 820 W of losses that can be extracted from this system. If all losses were to be distributed equally over the 20 transistors on a converter with 94% efficiency, this would enable a predicted maximum transferred power of 14 kW. The TIM dominates the thermal resistance, which stresses the importance of improving the thermal interface resistance to achieve a lower $R_{total.}$

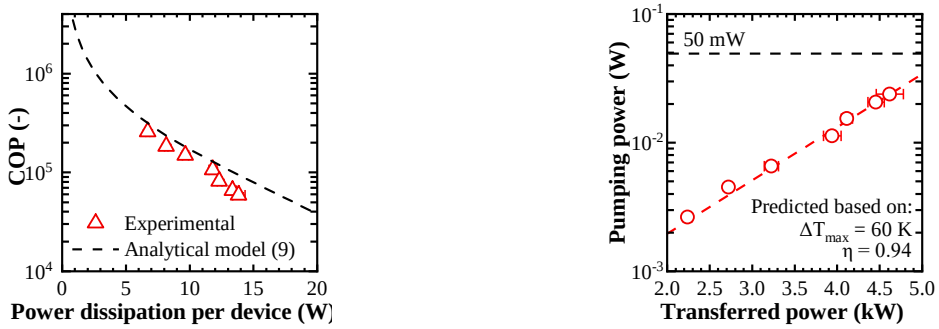


Figure 23: (a) Comparison of COP versus maximum power dissipation between the predicted COP from (9) and the experimentally derived COP of the fabricated manifold heat sink. (b) Pumping power versus predicted converter output power based on $\Delta T_{max} = 60\ K$.

Figure 24: Representative pumps for selected power ratings. (a) 50 mW: Bartels Mikrotechnik GmbH, (b) 1 W: TCS Micropumps Ltd, (c) 10 W: Flight Works, Inc.

3.2.3 Full System Testing

The microchannel cold-plate manifold heat sink was evaluated during operation of the converter for an output power up to 2.5 kW, while the flow rate was fixed at 1 ml/s. Figure 25 shows the temperature rise per transistor during operation of the converter at a loading of 1 kW. Since the total mass of the silicon cold-plates is low, the system has a small thermal inertia and thus steady state is obtained within a few minutes. A large spread in maximum temperature rise was observed among different transistors. At 1 kW, Q_{a4} reached a steady state temperature rise of 25 K whereas the temperature rise on Q_{P5} did not surpass 8 K. Figure 25 also shows the steady state temperature map at 1 kW transferred power. A clear pattern can be seen where the Q_a and Q_b transistors heat up more than the Q_P and Q_N transistors. This large spread in temperature can be accounted by the difference between the 2 types of power devices used and the electrical design of the converter, as well as the uneven stress on the devices due to the selected converter topology [46]. Despite this large temperature spread, the temperatures rise of all devices stayed well below the limit of 60 K over the entire range of measured transferred power up to 2.5 kW.

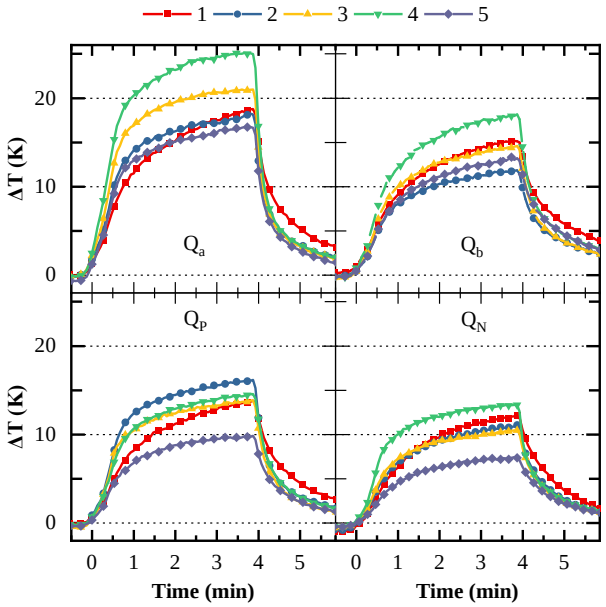


Figure 25: Transient temperature rises between the device and the coolant inlet temperature at 1 kW transferred power for all 20 transistors.

3.2.4 Cooling Systems Comparison

To compare the thermal performance with conventional heat sinks, we repeated the experiment using a 10 cm x 10 cm x 4.5 cm aluminum heat sink on top of the converter with a thermal resistance of 1 K/W at natural convection. Note that this value is 10x higher than the thermal resistance of the microfluidic heat sink, whereas its volume is 13 times larger. This shows that the microfluidic heat sink is 130 times more volume efficient than conventional heat sinks. Three cases were evaluated, as shown in Figure 26: In *Case A* no fan was used, in *Case B* a fan was added with a flow rate of 1.0 m^3/min and in *Case C* the 3D printed manifold heat sink was evaluated. Figure 26 shows the average temperature rise for these three scenarios, revealing the much more efficient cooling of the proposed microfluidic heat sink. For a 1 kW of transferred power, *Case A* showed an average temperature rise of 43 degrees, which was reduced to 26 K in *Case B* and in *Case C* the average temperature rise was only 10 K. The offset in temperature rise at zero transferred power for *Cases A* and *B* was due to the constant losses in the power supplies that drive the transistors.

By moving from an air-cooled converter to a liquid-cooled converter, the maximum converter power can theoretically be increased from 1.4 kW to 6 kW, which results in a more than 10-fold increase in power density, ρ_P, up to 30 kW/l, revealing the clear benefit of this new cooling technique.

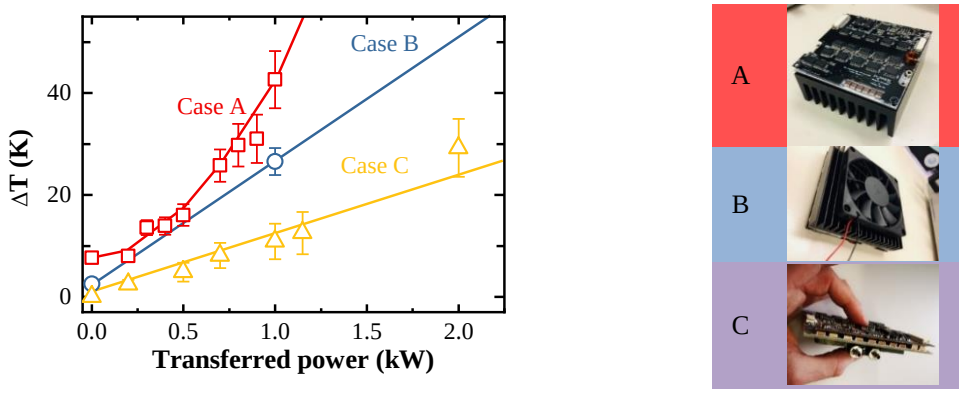


Figure 26: Temperature rise between the device and the coolant inlet temperature versus converter power for *Case A:* Converter with aluminum heat sink, *Case B:* Converter with heat sink and fan and *Case C:* Converter with 3D-printed microfluidic heat sink.

3.2.5 Discussion and Future Work

The microfluidic manifold heat sink can handle higher heat loads in a smaller volume compared to conventional air-cooled approaches and is therefore a promising approach for high power density application. However, the evaluated converter was not specifically designed to have equal losses over all transistors, causing a large temperature spread. The single outlier at Q_{a4} limits the maximum power in the current setup, which raises an interesting possibility for design optimization. If the power dissipation per components is known, cold-plates with customized geometries can be designed for each transistor to achieve a uniform temperature distribution. Equal temperature distribution can easily be obtained by increasing the number of parallel channels on the devices with high heat loads and by reducing the number of channels on the devices with low heat loads. Changing the number of channels modulates the flow rate at equal pressure drop as well as the effective surface area for heat transfer. Following this approach, heat sinks can be sized in the same way as transistors and passive components to achieve an optimum design, which adds a new layer of co-engineering to the design process. **We believe that this extra layer of optimization and design flexibility bridges the gap between electric design and thermal management which helps increasing power density in future power electronics applications.**

3.3 Miniaturization of Power Converters

GaN technology offers the unique potential for monolithic integration of several devices on the same chip, enabling the beginning of a new era of power integrated circuits (ICs). That means that modular multilevel converters, as the nX described here, can now be seen as power chips with multiple driving and power inputs/outputs. This renders the idea of magnetic-free topologies even more favourable for future power conversion applications. In this part of the report, we investigate the integration of several Tri-Anode Schottky Barrier Diode to demonstrate the first full bridge rectifier on a single GaN chip.

3.3.1 Development of a GaN Tri-Anode Schottky Barrier Diode

Despite the significant progresses on integrated gate driver solutions [47], [48], the development of lateral GaN SBDs still faces a more challenging path. In particular, the high electron concentration of the two-dimensional electron gas (2DEG) results in a large electric field peak at the Schottky barrier, drastically limiting the device blocking capabilities. Different schemes have been proposed to overcome these shortcomings, such as recessed anodes [49]–[51], field plates [52], [53] and Tri-Gate / Tri-Anode hybrid structures [54]–[58]. In particular, GaN SBDs adopting a Tri-Gate architecture have demonstrated large breakdown voltage (VBR) up to 2 kV with low turn-on voltage and on-resistance. In addition, the Tri-Gate technology provides several other advantages such as high transconductance [59], small subthreshold swing (SS) [60], high ON/OFF-state current ratio [61], and diminished short channel effect [61], [62], along with the ability to control multiple channel heterostructures [56], [63], [64].
To fully exploit the remarkable potential of Tri-Anode SBDs, we perform a thorough switching performance characterization and comparison against GaN diodes based on a planar architecture and typical fast recovery Si diodes.

Fabrication

The devices were fabricated on a GaN-on-Si heterostructure consisting of 4.2 µm of buffer, 420 nm of unintentionally doped GaN(u-GaN) channel, 20 nm of $Al_{0.25}Ga_{0.75}N$ barrier and 2.9 nm of u-GaN cap-layer. The electron concentration and mobility of the 2DEG from Hall measurements at room temperature were 1.25×10^{13} cm^{-2} and 1700 $cm^2/V{\cdot}s$, respectively. The fabrication process started with electron- beam lithography to define the mesa and nanowires in the anode region. The sample was then etched by Cl_2-based inductively coupled plasma etching (ICP) to a depth of 220 nm. The width of the nanowires in the anode was varied from 100 nm to 300 nm (W100, W200 and W300), while the nanowires spacing was fixed to 100 nm. The cathode contact was formed by a stack of Ti (20 nm)/Al (120 nm)/Ti (40 nm)/Ni (60 nm)/Au (50 nm) and annealed at 780 °C for 30 s. 20 nm-thick SiO_2 was conformally deposited over the nanowires by atomic layer deposition (ALD) and then removed in the Tri-anode region by wet etching with HF 1%. A Ni/Au metal stack was then evaporated to form the anode contact (50 nm/150 nm) followed by 1 µm thick metal pads. No passivation layer was deposited on top of the devices. A Scanning Electron Microscope (SEM) image of the SBD is shown in Figure 27, which highlights the Tri-Anode and Tri-Gate region. The cathode to anode distance was set to 16.5 µm and 50 alternating anode-cathode fingers were designed for a total device width of 9.9 mm. Scaled devices are desirable to reduce the effect of the parasitics of the measurement circuit, which are typically comparable to the capacitance value of small area devices. Planar diodes without any Tri-Anode structure were co-fabricated on the same chip and used as the device of reference. In order to ensure a fair comparison, the same total field plate length has been designed for both the Tri-anode devices and the planar reference.

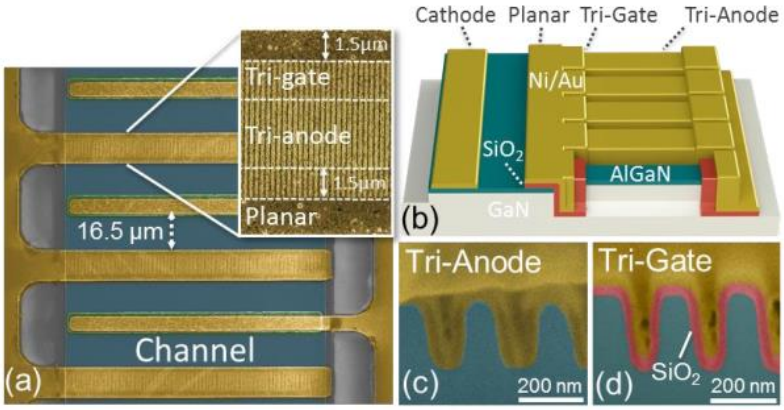


Figure 27: (a) SEM image of the scaled up SBD fingers. The right-hand inset zooms on the anode finger, highlighting the Tri-Anode, the Tri-Gate, and the planar region. (b) Device schematics (c-d) Focused Ion Beam (FIB) cross section of the TriAnode and the Tri-Gate structure.

Switching Characteristics

The reverse recovery curve for the Tri-Anode SBD against the planar reference is shown in Figure 28. The measurements were obtained with a double-pulse tester (DPT) circuit, able to provide high di/dt transitions of 280A/µs. A first pulse charges the inductor to the desired current, which is then forced through the diode during the dead time. A second pulses then causes the SBD abrupt transition to the off-state, allowing the measurement of the recovery time and charge. The diode forward current (I_F) was set to 1 A and the reverse voltage to -100 V. A significant reduction in the reverse recovery charge (Q_{rr}) and current undershoot (I_{rr}) is observed for the Tri-Anode SBDs with respect to the planar reference, resulting in a 40% decrease in I_{rr} and a two-fold reduction in Q_{rr}. This is of fundamental importance as it shows that the Tri-Anode architecture leads to faster devices with lower switching losses. In addition, a major improvement is observed for the Tri-Anode SBDs with respect to a commercial 1000V-rated fast-recovery Si diode(FRD) and even to a 200V-rated Si SBD with similar current rating.

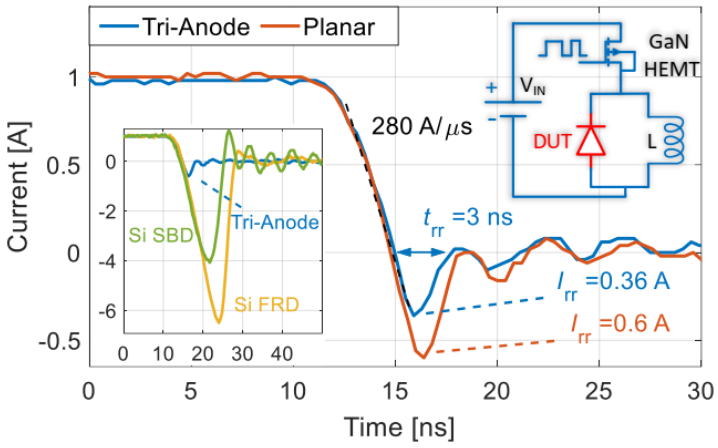


Figure 28: Reverse recovery measurement for a Tri-Anode and a planar GaN SBD with w of 200 nm. The di/dt was set to 280 A/µs and the reverse voltage to -100 V. The double pulse circuit used in the experiment is show on the top right. The left-hand inset shows the reverse recovery for Tri-Anode GaN SBDs compared with a commercial Si SBDs and Si fast recovery diode.

To understand the advantageous switching characteristics of the Tri-Anode architecture, the off-state C-V curve of the SBDs under study was experimentally extracted using a Keysight B1505 analyser (Figure 29(a)). This shows a first step at V_G=-5 V, in correspondence to the planar region depletion,

and a second and third steps, close together, corresponding to the depletion of the Tri-Gate and Tri-Anode regions, which move to smaller V_G as the fin width is reduced and result in a significant capacitance decrease. This behaviour, which is in contrast with the results from doped bulk Fin-FETs, originates from the conduction through the 2DEG rather than at the nanowire/oxide interface and can be readily understood by considering the total charge (Q_{CV}) stored in the reverse region. Figure 29(b) presents the Q_{CV} obtained from the integration of the C-V curve which shows a consistent decrease in value as the width of the Tri-Anode is reduced. Such a result is caused by the partial removal of the 2DEG due to the nanowire etching in combination with the fin sidewalls depletion and the AlGaN barrier strain relaxation which lead to a charge decrease in the nanowire, reflected in the shift of the second capacitance step towards 0 V. The capacitive charge reduction with the fin width is consistent with the Q_{rr} trend extracted from the reverse recovery measurement. However, while the capacitive charge is a precious tool to gain insights on the Tri-Anode physics, Q_{rr} better reflects the device operation in a real circuit as it also takes into account the charge stored during forward conduction.
It is noteworthy that the Tri-Anode architecture leads to a major reduction in the $R_{ON}{\cdot}Q_{rr}$ figure-of-merit compared to planar devices, and nearly a threefold decrease when reducing the nanowire width from 300 nm to 100 nm. Such an improvement is achievable thanks to the substantial charge decrease for smaller Tri-Anode widths, which leads to only a minor degradation of the on-resistance. The slight increase in the diode R_{ON} is due to the partial 2DEG removal in the Tri-Anode region and it can be overcome by employing a high-conductivity heterostructure such as the Multi-Channel platform. The reduced Q_{rr} is highly beneficial for the diode frequency operation as illustrated in Figure 29(c) which shows the half-wave rectification with minimum signal distortion during zero crossing for a 250 V peak-to-peak signal at 1 MHz.

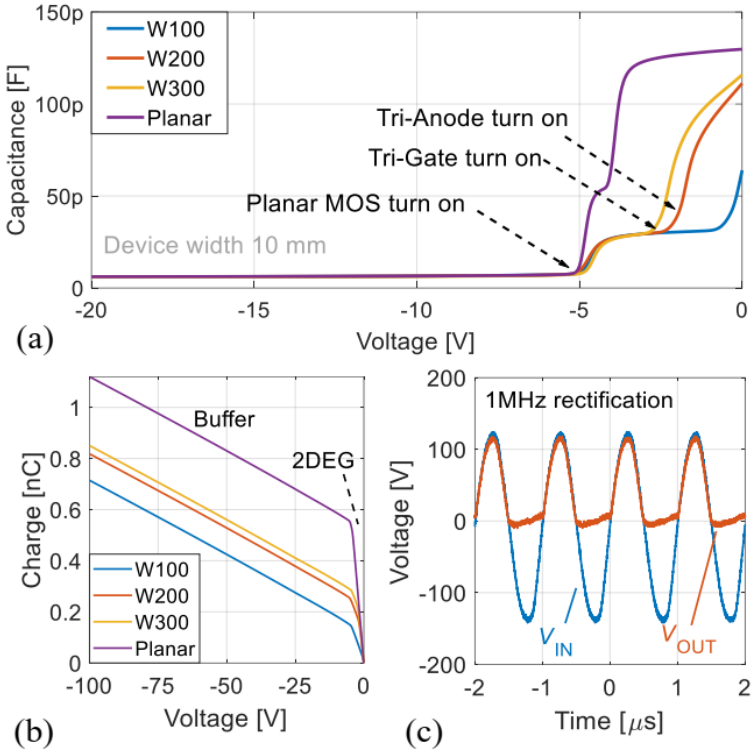


Figure 29: (a) Capacitance versus reverse voltage (VR) curve for Tri-Anode and Planar diodes. (b) SBD reverse charge obtained by integrating the capacitance curve. (c) Half-wave rectification for a Tri-Anode SBD with fin width of 200 nm for a 1 MHz input signal with peak-to-peak amplitude of 250 V

3.3.2 Monolithically integrated Full Bridge Rectifier

Here the promising potential of GaN technology for monolithic integration are investigated, by demonstrating the first scaled-up diode bridge rectifier on a single GaN substrate. Additionally, a new thermal management paradigm for direct cooling of GaN-on-Si power IC's is examined, in which the silicon substrate functions as a microfluidic heat sink, turning GaN-on-Si into a cost-effective, high thermal performance substrate. To combine these two novel structures, a sophisticated PCB is developed, which serves for both the electrical connections and the coolant distribution at the same time.

Device Fabrication

To demonstrate the potential of lateral GaN technology for integrated power ICs topologies, four of the presented diodes were monolithically integrated to form a scaled-up Full Bridge Rectifier (FBR). Figure 30 (a) shows a picture of the fabricated device and the corresponding circuit schematics. The Tri-anode/tri-gate SBD were developed on an AlGaN/GaN-on-silicon wafer with an epi-structure, following similar fabrication process as that of the single tri-gate SBD, which is graphically presented in Figure 30 (b). Four gold bond-wires of 25 µm diameter were used to connect the integrated FBR to the PCB that holds the output filtering capacitors and the input/output connectors, as shown in Figure 30 (c)

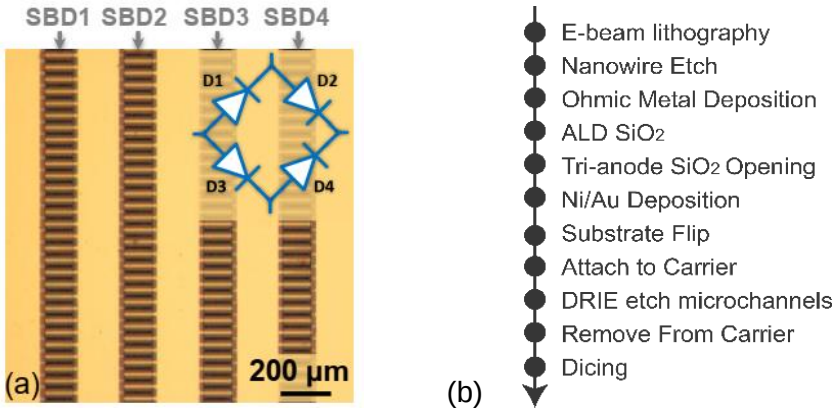


Figure 30: (a) Optical microscope image of the integrated full bridge rectifier and corresponding circuit schematics (b) Fabrication process.

Near-Junction Cooling

As already mentioned, the high level of integration of a power converter in a reduced die size results in high heat fluxes that need to be addressed to allow miniaturization and optimum device performance. To effectively cool down the developed power IC, **we expand our initial idea of microfluidic cooling by embedding the microchannels directly on the substrate of the device, as depicted in** Figure 31**.** This structure, called *direct cooling*, removes most of the thermal resistance components, allowing for a high COP.

The well-established micro-fabrication processed developed for Silicon can be used to turn the substrate into a high-performance liquid-cooled microchannel heat sink [31] using standard low-cost MEMS fabrication methods [65]. The wafer was temporarily bonded to a carrier wafer before microchannels were etched in the backside using deep reactive ion etching to a depth of approximately 500 µm. Figure 31 (c) shows a SEM of the sharp sidewall profile of the microchannels etched in the back of the power IC.

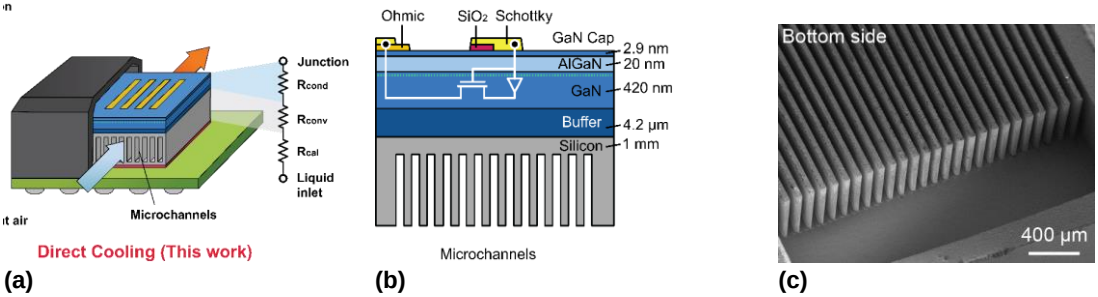


Figure 31: (a) Embedded liquid cooling. (b) Epi-structure and cross-section of device. (c) SEM of the microchannels etched in the backside of the FBR.

PCB Fabrication

A new PCB concept was developed that incorporates both the electrical connections and the liquid distribution system. A simplified representation of the designed 6-layer (3-boards) PCB is given in Figure 32 (a). The top board is reserved for the electrical connections, including the bond wiring and the output filter capacitors. The middle board was milled to allow the coolant to flow under the FBR chip. Blue and red coloring in Figure 32 (a) highlights liquid flow. The input and output electrical connections are also located in the middle board and connected to the top one through filed-vias. The bottom board acts only as a sealing of the liquid distribution system. A 3D representation of the GaN-on-Si power IC with substrate embedded microchannels can be seen in Figure 32 (b) and the developed prototype in Figure 32 (c). With only 40mm length and 15mm width the micro-converter prototype resembles a USB stick.

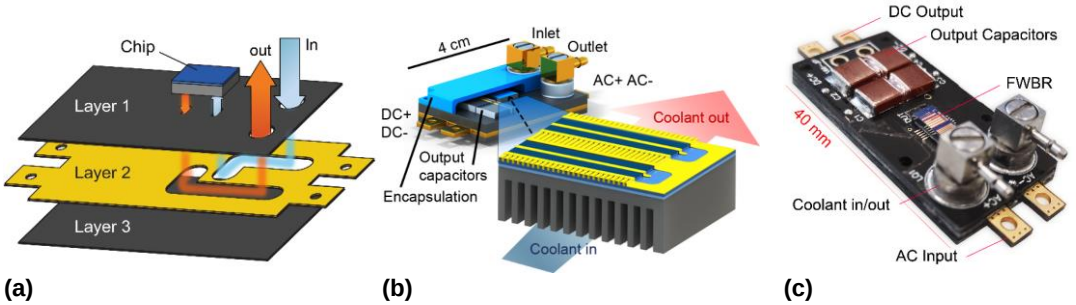


Figure 32: (a) Concept of Through-PCB coolant delivery, where liquid flows through a milled middle layer of a 3-layer PCB. (b) Concept of a GaN-on-Si power IC with substrate embedded microchannels mounted on a micro-converter with through-PCB coolant delivery. (c) Picture of the realized micro-converter prototype before encapsulation.

Experimental Results

cooled FBR. Three modes of operation were evaluated, full-wave rectification, AC-DC conversion using an output capacitor, and voltage doubler by connecting one AC terminal to the neutral point between the two output capacitors. Figure 33 (b) shows the measured current and voltage waveforms of the input and rectified output, at a peak-to-peak voltage of 150 V, corresponding to 70 W of transferred power. Figure 33 (c) shows the waveforms during high-power operation as voltage doubler up to 70 W and as AC-DC rectifier up to 120 W, measured using a 50 Ω load.

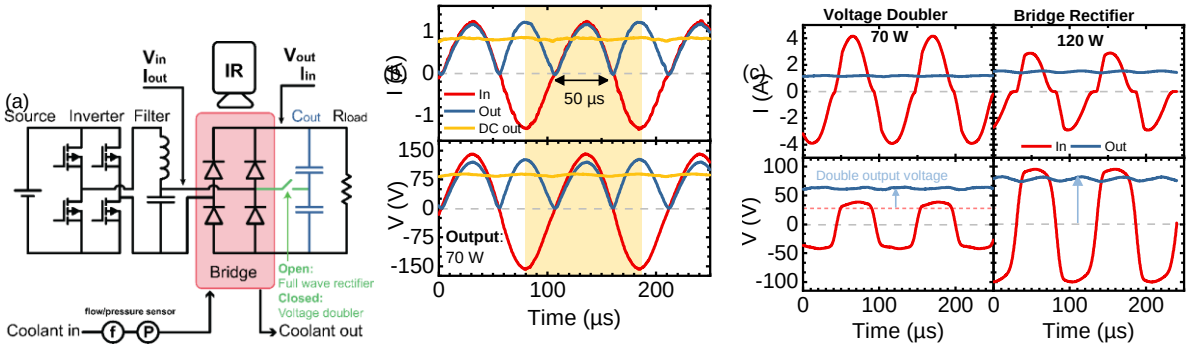
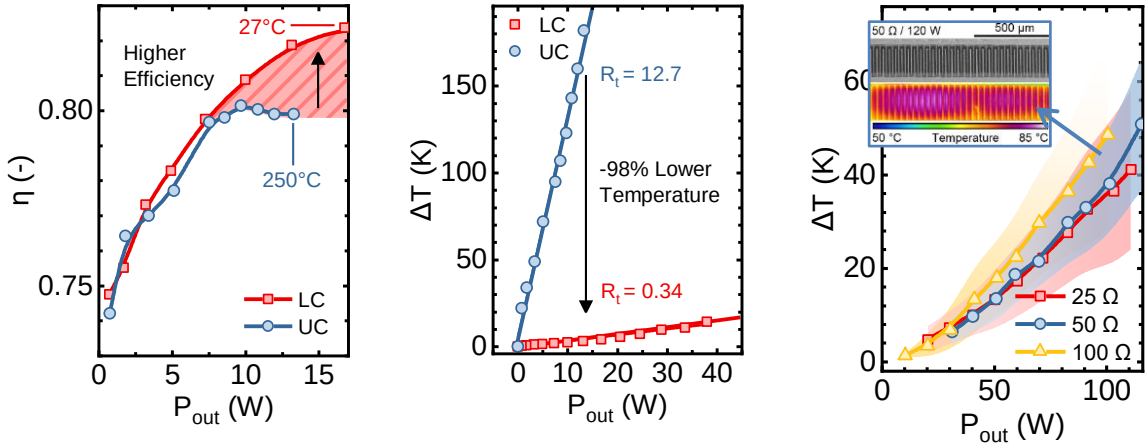


Figure 33: (a) Experimental setup for evaluating the liquid cooled SBD FBR; output capacitors are placed such that the setup can be used both as rectifier and voltage doubler. (b) Input and output waveforms during rectification of an AC input with a 50 Ω. (c) Input and output waveforms of the diode bride operating as 70 W voltage doubler and 120 W bridge rectifier.

Figure 34(a) shows the conversion efficiency versus transferred power for two situations, a regular FBR bonded to a PCB under a fan (indicated as UC), and the FBR with embedded liquid cooling (LC). The efficiency of UC peaks at approximately 9 W of output power, after which the rectifier is thermally limited at a maximum temperature of 250 ºC, while the maximum temperature of the LC was only 27 ºC . Over the entire measured range, LC showed a higher conversion efficiency due to its reduced temperature. Figure 34 (b) shows a comparison of temperature rise versus output power of UC and LC, with a measured thermal resistance of 12.7 K/W and 0.34 K/W, respectively (defined as temperature rise per output power). This corresponds to a 98% reduction in temperature rise by using embedded liquid cooling. Finally, Figure 34 (c) show the temperature rise for varying loads, highlighting a low temperature rise over the entire measured range of power and load conditions. The experimental results reveal the advantage of co-designing the electronics with the cooling system to achieve record power densities by integrating GaN power devices with substrate embedded microchannels



(a) (b) (c)

Figure 34: (a) Conversion efficiency versus output power, (b) temperature rise versus output power of the uncooled and liquid cooled integrated SBD FWBR, showing a reduction of more than 98% in temperature rise at identical output power and an increase in conversion efficiency. (c) Temperate increase during rectification including output filtering, for a load of 25 Ω, 50 Ω and 100 Ω. SEM image of the FBR and IR thermographs of the FBR for an output power of 120W

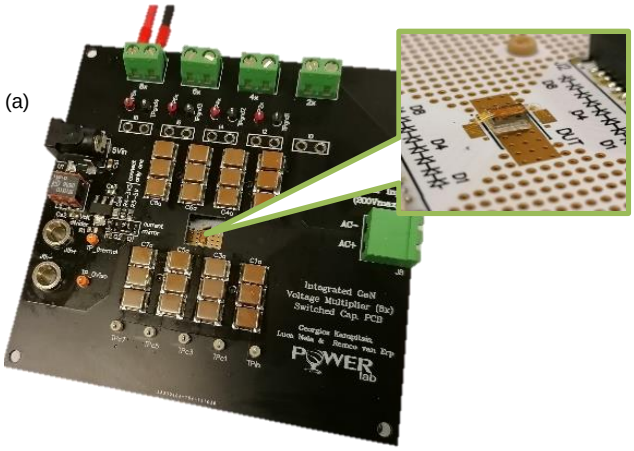
Discussion and Future Work

By combining advanced materials with advanced fabrication techniques we demonstrated the first monolithically integrated full bridge rectifier of 120W that occupies the size of a USB flash drive. The foundation of this promising technology is the TriAnode SBD that exhibits reduced reverse recovery charge and capacitance with respect to the planar architecture, allowing for high-frequency operation. We demonstrated that our TriAnode SBDs combine excellent static and dynamic characteristics and can be a fundamental building block for future power GaN ICs. Also, the direct-cooled power IC, in combination with a novel PCB-based coolant delivery resulted in a compact 120 W AC-DC converter. This new cooling paradigm is a promising step towards high performance power ICs, as embedded liquid cooling on cost-effective GaN-on-Si platform can be an enabling technology for reaching an ultrahigh power density.

3.3.3 Monolithically integrated Voltage Multiplier

In the same context of monolithic integration of several GaN SBDs on the same chip, we lately demonstrated the first GaN voltage multiplier in a Cockcroft-Walton configuration. 8 scaled-up diodes were fabricated on a Si substrate and bonded on a PCB through silver-paste (inset of Figure 35(a)). This PCB serves as heat spreader with several thermal vias. Three 2.2uF multilayer ceramic capacitors were connected in parallel to form each switching capacitor, mounted on the top side of the PCB. Multiple test points were provided to measure the voltage boost at different levels and monitor the diode current. Figure 35 (b) shows the voltage multiplication of a squarewave input by a factor of 4x, 6x and 8x. The transferred power was measured at 70W but further experiments need to be performed to exploit the full potential of this power IC.

(a)



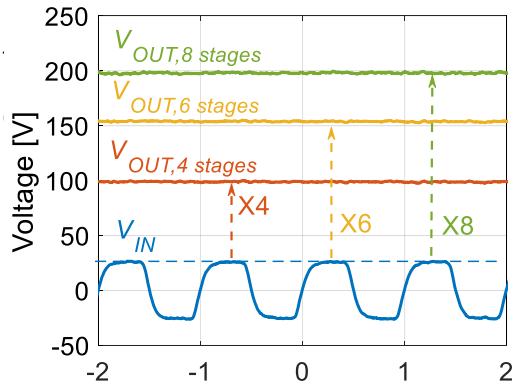


Figure 35: (a) Monolithically integrated voltage multiplier and peripheral switching capacitors PCB. (b) 8x voltage boost of a squarewave input (from 25V to 200V).

3.4 Autonomous LED Street-Light Project

This project has been running for the past 2 years and has been supported by thorough mathematical analysis and lab testing. At this stage we focus on the practical considerations for optimizing/finalizing the entire system.

The remaining work was split in two parts, regarding the *hardware* and a *software*, respectively. The main objectives of the *hardware* section concerns the selection and testing of reliable and cost-effective energy storage system, as well as the development of custom PV module to meet the expectations of both the designer and the engineer teams. These updates lead to the development of a new control circuit that incorporates the power conversion stages, protection circuitry and communication interface. The purpose of the *software* section is to realize an online connectivity for storing and managing useful data (e.g. produced and consumed power) and to establish an accurate weather prediction, important for an efficient energy management.

3.4.1 The Solar Panel

As a reminder of the system specifications, we report here some key data: the autonomous street-light needs to function for 5 consecutive days without any sunlight and should be able to recharge completely the battery within 3 days, even at minimal irradiance (in December). Knowing the power that needs to be transferred to the LEDs (40W), we can extract the power that has to be delivered by the panel:

$$E_{night} = 6h \cdot 40W = 240Wh \tag{12}$$

which means that the power that has to be generated in one day need to be equal to or greater than

$$E_{PV} = E_{night} + \frac{4}{3} \cdot E_{night} = 560Wh \tag{13}$$

For a normal commercial monocrystalline solar cell, the efficiency is around 20%.That means that the minimum energy to be received from the sun is equal to:

$$E_{sun} = \frac{E_{PV}}{0.2} = 2800Wh \tag{14}$$

This amount of energy has to be received even in December when the irradiance is at its minimum. Taking the average irradiance at those dates, we can estimate that our panel needs a surface of:

$$S_{PV} = \frac{E_{sun}}{E_{Dec}} = \frac{2800Wh}{1000Whm^{-2}} = 2.8m^2 \tag{15}$$

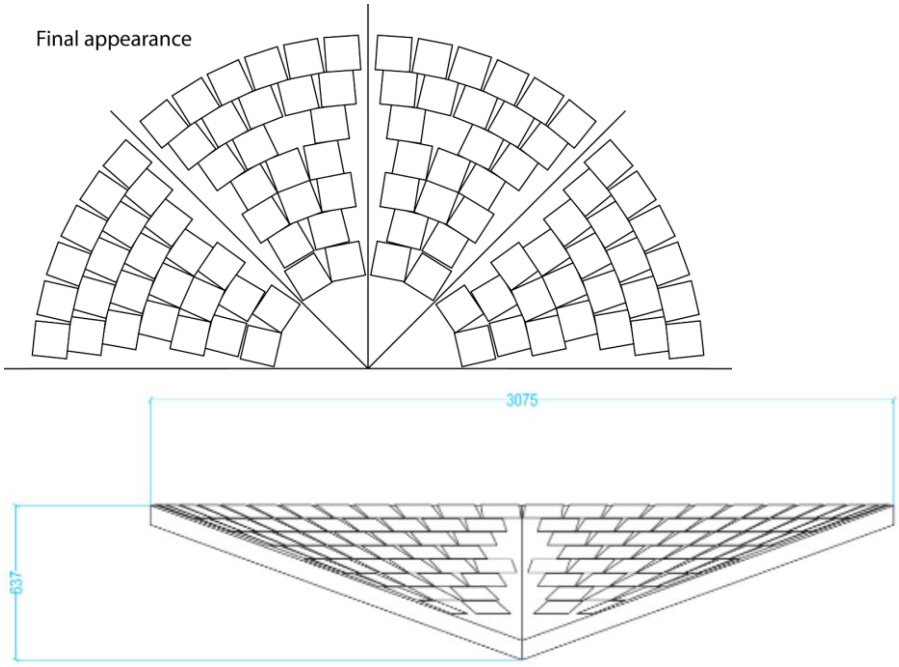
Given that the most commonly available PV cells have dimensions of 15.6cmx15.6cm, we can calculate the required number of cells:

$$N_{cells} = \frac{S_{PV}}{S_{cell}} = \frac{2.8m^2}{(15.6cm)^2} = 115cells \tag{16}$$

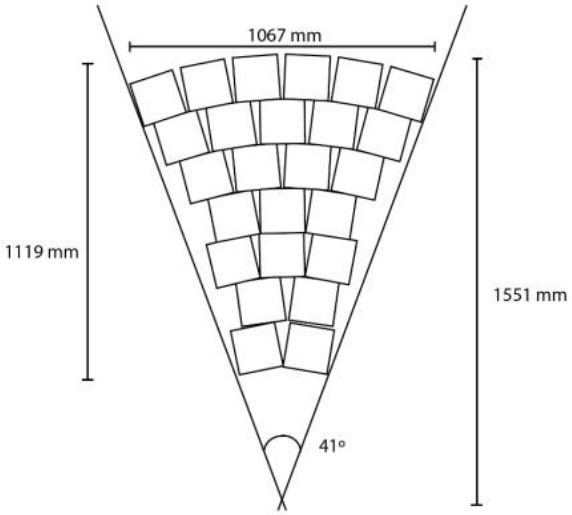
The arrangement of all cells is determined by the architectural design described in the following subsection.

Design

The architectural design of the autonomous street light was performed in close collaboration with an architectural team and is presented in Figure 36. The PV panel is separated in 4 sub-modules, each of which consists of 25 cells, relatively close to meet the electrical requirements. This separation serves two purposes: 1) to simplify the fabrication process and 2) to introduce a curvature to the final structure for aesthetic reasons. It is important to point out here that the cells are extremely brittle and any stress can break them. This means that, although desirable, curving each sub-module is an engineering challenge on its own.



(a)



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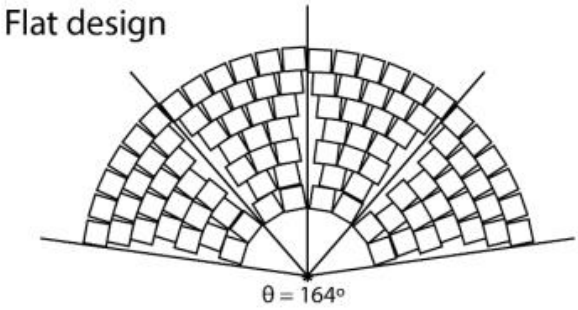


(c)

Figure 36: Architectural design of the autonomous LED light.

Fabrication

Fabrication of the PV prototype was performed in collaboration with prof. Franz-Josef Haug, affiliated to EPFL, at the Microcity Lab. The lab is fully equipped to assemble commercially available cells of standardized dimensions into a final structure, flat or even curved. The process is called encapsulation, and can be broken-down into the following steps:

Step 1: Cells Bonding

All the cells are pre-soldered, as shown in Figure 37(a), so as to facilitate the assembly of the pattern and it is the process that takes the longest time. Alternatively, cells with pre-soldered flat wires can be used to speed-up this fabrication step.

Step 2: Cells Assembly

The cell are then connected to form the pre-defined pattern using a template, as shown in Figure 37(b). All cells per sub-module are connected in series, resulting in an open circuit voltage of V_{S-M}=12.5V. A single antiparallel diode is connected across each submodule to protect against hot spot formation during partial shading conditions.

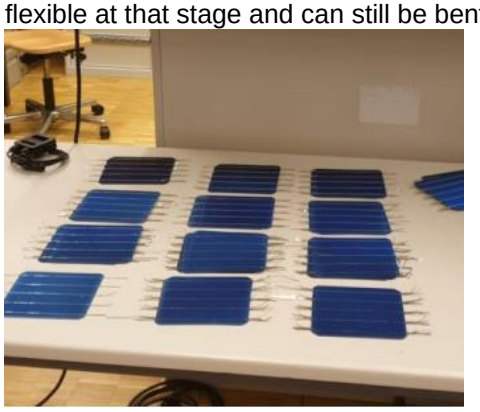
Step 3: PV panel Layers

At the moment, the only thing holding the pattern together are the solder joints between the individual cells. So different layers are added that constitute the final PV sub-module (Figure 37(c)). The base is made out of PTFE, hence its white color. Layer 2 is a thin plastic that melts under the heat and acts as a glue for the layers directly above and under it. Layer 3 is a metallic mesh that adds registry to the built.

Another layer of the plastic glue is placed on top of the fiberglass, and the cells are then slid on top. Some re-positioning is always required in order to maintain the intended pattern.

Step 4: Pressing

The stack, presented in Figure 37(d) is then slid in a press, called laminator, that heats and presses the whole construction. Another advantage of dividing the PV panel in 4 sub-modules is that each part is small enough to fit in the laminator available in Neuchâtel. The laminator heats the stack until the plastic glue melts, and then presses uniformly across the entire area with a force of 1atm. The entire lamination process takes 28 minutes. Once the lamination is finished, the final sub-module (Figure 37(e)) is removed and let to cool until the glue sets. It is worthy to note that the panel is still relatively flexible at that stage and can still be bent into a desired shape.



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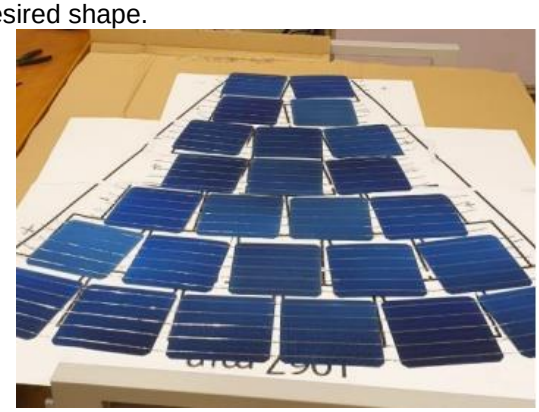

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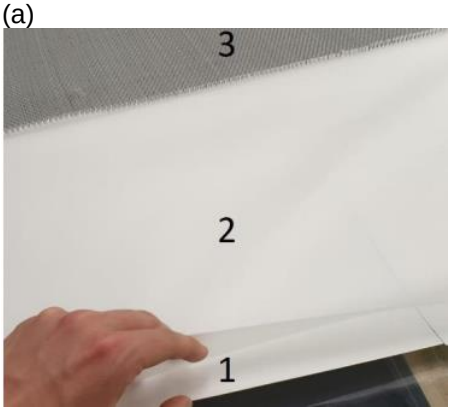

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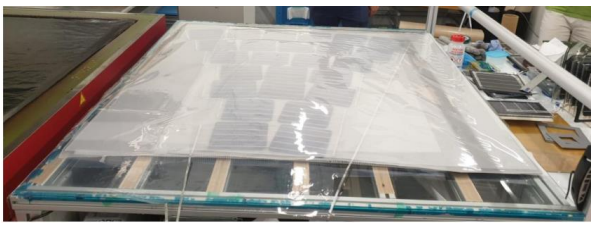
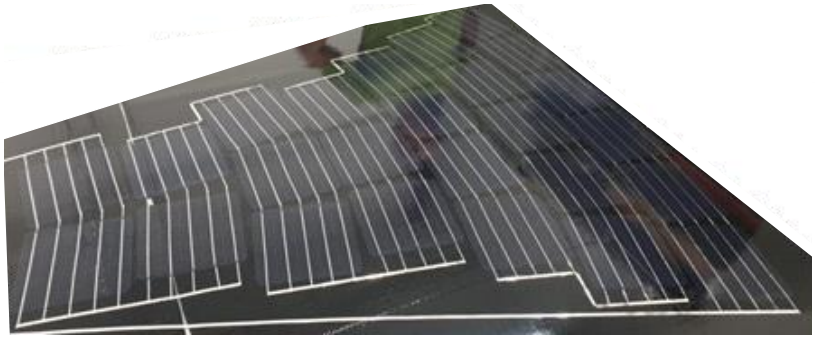


(d)



(e)

Figure 37: PV sub-module fabrication steps: (a) Cell bonding, (b) Cell assembly, (c) different layers constituting the panel, (d) construction inside the laminator and (e) final PV sub-module.

3.4.2 Energy storage

Similar to the PV panel construction, the sizing of the battery has already been done in a previous stage of the project and here we solve practical issues, considering cost, availability, lifetime, size, weight, charging and discharging current, working temperature and maintenance requirements. Given these criteria, there are two types of batteries to be considered: *Lithium* and *Lead-Acid batteries.*

The available capacity of the battery system has been calculated to be 1.2 kWh to power the LED even in the worst case conditions of 5 consecutive days without sunlight. But in order to increase the life of a battery, we should only use a certain percentage of its nominal capacity. The available range varies with the technology from only 30% of the capacity up to 70% of the capacity. The technical term is the *depth of discharge* (DOD) but we will use the term *available capacity* for clear presentation.

Technology Comparison

Lithium technology is an established technology used in the majority of the modern mobile devices. Such batteries have a higher volumetric energy density (250-693 Wh/L) and specific energy density (100-265 Wh/kg) compared to lead-acid batteries (80-90 Wh/L and 35-40 Wh/kg, respectively), which means that, for the same capacity Li batteries are smaller and lighter. At the same time they exhibit higher available capacity of 70% (compared to 30% for lead-acid ones). Among the Li technologies, the Lithium-polymer are commonly used in industrial systems, due to their reduced risk of explosion/fire, as a result of their polymer electrolyte in the form of a solid or a gel (as opposed to lithium ion that uses a liquid electrolyte). The most important aspect of the $LiFePO_4$ technology is the outstanding life expectancy of 1500-2000 cycles over 10 years, quite important for a fully autonomous system.

But Li batteries have also a serious limitation: They cannot be charged under 0°C and the charging current has to be greatly reduced between 0°C and 5°C. This is problematic for an outdoor application in Switzerland, where the temperature can easily become negative in winter. In addition to that Lithium batteries are made out of individual cells with a voltage of ~3.5V assembled in series or in parallel to make a battery pack. Complex battery management systems (BMS) need to be developed to ensure good balance between the cells. Such circuits add to the total system cost and reduce its reliability.

Contrary to lithium-ion, the charging process of the **lead-acid battery** isn't that much dependant on the ambient temperature and there is no need for a BMS. Additionally, there is no real size and weight

limitation for our application, since the autonomous LED lamp is fixed to a specific place, an there is plenty of room under a bench/compartment to store the batteries.
These factors render the lead-acid batteries the technology of choice for our system. This decision is also supported by several companies that install off-grid solar systems in Switzerland and they use lead-acid batteries, mainly due to the temperature conditions and for reliability issues. Lead-acid technology is really mature, since it was the first type of rechargeable battery, and there are plenty of resellers.

However the main disadvantages of the traditional lead-acid technology concern the available capacity, which is only 30% in average, and the need for maintenance (the electrolyte can dry out in a period of 5-10 years). This implies that a sensor is needed to measure the electrolyte level inside the battery and alert in case is too low. This is not realistic for an autonomous system and lead the research to a different type of lead-acid technology, namely the Valve Regulated LeadAcid (VRLA). As the name implies, this family is characterized by a sealed battery with a small valve to let some potential fumes out without letting anything in. This small addition takes care of one of the fumes and allows the placement of VRLAs inside a closed environment.

Two types are available with similar characteristics: the first variant are the so-called Gel batteries. In this technology, the liquid electrolyte is replaced by a gel, which prevents drying out or leaks. That means that Gel batteries require no maintenance, can stand cold temperatures and can be used within a closed environment. The second variant are the AGM batteries, standing for Absorbed Glass Mat batteries. The liquid electrolyte is stored inside fiberglass sponge, which again prevents drying out and acid spills. The only notable difference between the two types is the charging current, which is lower in a Gel batteries.

Battery Selection

Given the aforementioned practical challenges and limitations we decided to utilise VRLA AGM batteries that can be safely work in a cold environment, require no maintenance, they are readily available at a low cost. The selection of AGM batteries over the Gel once derives from the fact that the charging current is defined by the illumination conditions and cannot be regulated to a fixed value (because that would mean loss of solar energy). In fact, the charging process of AGM batteries is very “forgiving” and takes away the concern of having a complicated voltage and current management across the battery terminals.
The entire system will ultimately be powered by two 90 Ah, 12V AGM deep cycle batteries from *Victron Technology*. We place them in series to reach 24V to reduce the charging and load current. The entire ESS can be seen as a whole block (a single battery) of twice the voltage, i.e. a 90Ah, 24V capable of storing 2160 Wh of energy. This battery can be discharged down to 50% without any significant degradation on its life.

3.4.3 Circuit Design

Given the system specifications, already defined in the 2018 annual report “High-efficiency power converters for potentially-large energy-savings applications” and the new requirements, set by the technical considerations, we redesign the electronics that manage the energy production, storage and delivery.

Block Diagram

The solar panel is composed of 100 cells producing 0.5V and 9 A each. The output of the entire PV module is, thus, 50V and 9A under standard test conditions, i.e. 1000W/m^2 at 25 ^{o}C. A step-down converter is therefore needed to interface the PV panel with the battery bank (24V), as shown in Figure 38. On the load side, a boost converter is needed to boost the voltage from the dc-bus level to

the LED nominal voltage (V_{LED} = 48V). Given that both step-down and -up conversion ratios are close to ½ and 2x, respectively, the simple buck and boost converter topologies are used, each of which requires just a single transistor and one diode.

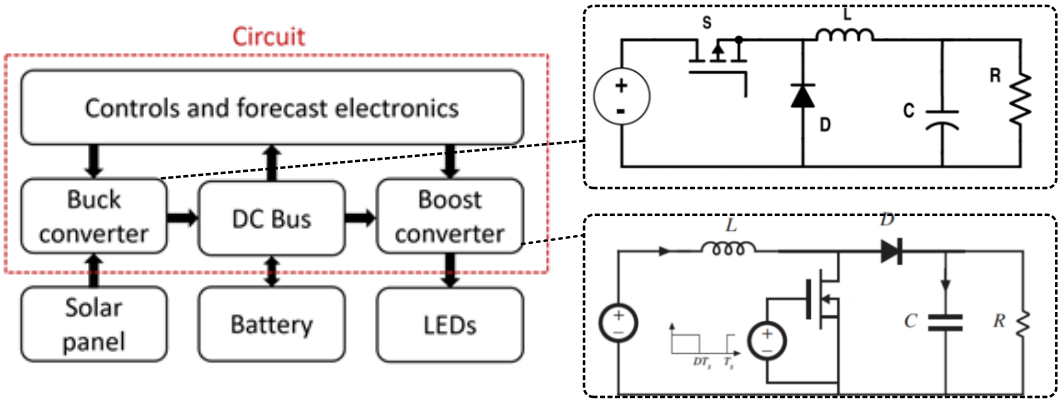


Figure 38: Simplified block diagram of the power electronics circuit and the two converter topologies.

The maximum inductor current can be calculated by (17). Considering an acceptable current ripple of 10% and a switching frequency of 100kHz we can extract the inductor value from (18). A 47uH COILCRAFT AGP4233 inductor of 24A current rating was chosen for the buck converter.

$$\mathrm{I}_{\max} = I_{PV} \cdot \frac{V_{PV}}{V_{DC}} = 9 \cdot \frac{50}{24} = 18.75A \tag{17}$$

$$L = I_{PV} \cdot \frac{V_{PV} - V_{DC}}{2 \cdot \Delta \mathrm{I}_{\max}} \cdot DT_s \tag{18}$$

The input capacitance, C_{PV}, is an important parameter that ensures a smooth operation of the PV generator with small ripple voltage. 4 electrolytic capacitors of 220 µF each constitute C_{PV}. The space occupied by the input capacitance is not significant due to the low voltage rating of the system. On the contrary, there is no need for a large output capacitance, given that the output voltage is determined by the battery bank.

The GaN GS61008T was selected as the main power switch due to its small footprint and high switching frequency capability. Two MBR40250G diodes are connected in parallel to share the relatively large switching current. Lastly, a unidirectional hall-effect current sensor monitors the PV-side input current and a bidirectional current sensor measures the charging and discharging battery current.

An enhanced *maximum power point tracking* (MPPT) algorithm with variable step and execution frequency of 250Hz was developed to always extract the maximum available power from the PV generator. The MPPT operation is bypassed if the battery has reached 100% of its state of charge (SOC).

The boost converter has smaller power rating, defined by the LED maximum power (48W). A single 220 µF electrolytic capacitor guarantees that the output voltage will be stable (ripple-free) and a 680µH DC630R inductor limits the ripple current to 10% of its nominal value. The same transistor and diode models are used as in the buck converter, to reduce large scale production cost. The boost converter operates with constant output current, regulated through a proportional-integral controller. As will be shown later, the LED power consumption and thus the reference current level is defined by the online weather prediction system.

Huge effort has been placed this year in transferring the successful electronics designs of the past years to a commercial-like product. A key factor throughout this process was *reliability*. We developed several different protection circuitry that ensure a long lifetime of the system.

Protection against reverse polarity, both for the PV and the battery, is of paramount importance. The simple but efficient circuit presented in Figure 39 was used, constituting of a low on-resistance Si MOSFET in series with the power line and a voltage regulator that controls the transistor's gate. In case of a fault connection of the PV generator or the battery, the transistor will not conduct. In normal connection, the regulator will bias positively the gate and the transistor will turn-on reducing its power losses. Decoupling capacitors across the voltage regulator and the transistor gate guarantee a stable voltage level, even in noisy environments.

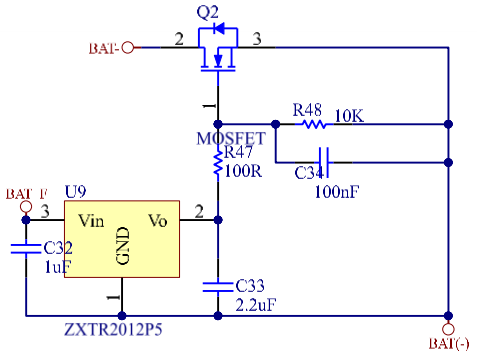


Figure 39: Protection circuit against reverse polarity.

A 30A fuse is also placed right at the battery input to protect the circuit from fire in case of a malfunction.

Three low-power LEDs are placed on-board to indicate:

- the power flow. Switching green LED for battery charging and constant green LED for battery discharge to the load.
- the battery state of charge. Green if V_{DC} >24V, orange (produced by simultaneously lighting the integrated green and red LEDs) when 18 ≤ V_{DC} ≤ 24V and red when V_{DC} < 18V.
- WiFi connectivity with a blue LED.

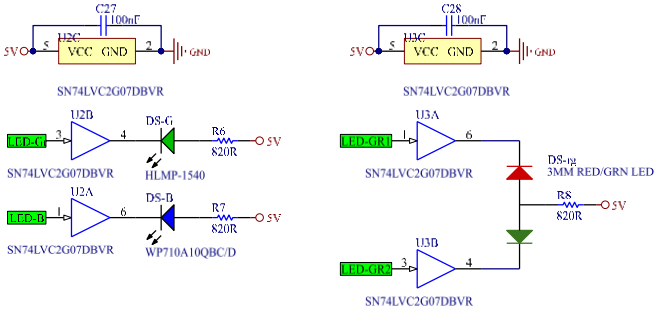


Figure 40: Low-power indication LEDs.

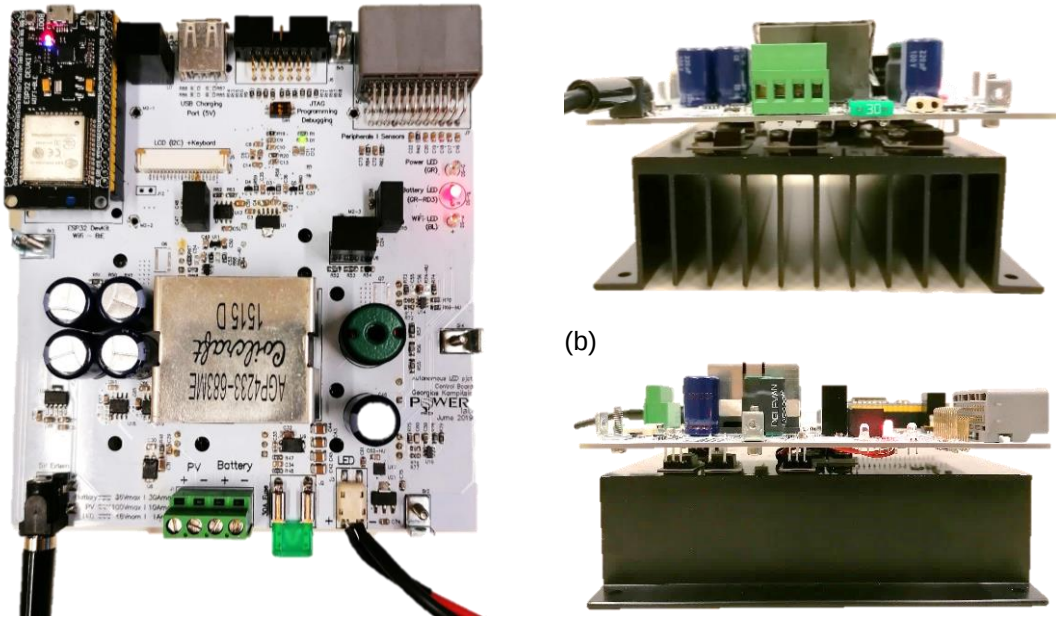
A set of sensors was also added to the final design to expand the capabilities of the system. More specifically we included:

- Four temperature sensors. One is mounted on the heatsink to constantly monitor the power electronics temperature and protect from potential overheating. Two more are keeping track of the battery temperatures and the 4th is placed outside the enclosure to measure the ambient temperature.
- The last temperature sensor is co-packed with a humidity sensor. Both measurements are important to gather information about the installation environment in relation to the produced power from the PV.
- Two motion sensors are placed on the top section of the autonomous LED structure. These sensors will help save energy in critical conditions, by dimming the light when necessary and illuminate in full power when people are in a radius of 10 meters.
- Two low-power consumption fans. One fan is dedicated to cool down the transistors if necessary and the second facilitates to circulate the air within the enclosure box.
- A USB port for charging external devices. This feature is particularly useful in public places (e.g. campus, parks) where people/users can charge their mobile devices.

Development

The developed system is shown in Figure 41. All the power inlets/outlets are aligned to the bottom edge of the board and all the small-signal connectors (sensors, programming ports, I^{2}C connector,

USB) are placed on the top edge. That leaves room for mechanical mounting brackets on the side of the board (see Figure 41(c)).
As can be seen, a single heatsink is used with exactly the same dimensions as the PCB. This will help build a simple enclosure from molded plastic or milled aluminum. The backside of all transistors/diodes are mounted on the heatsink via a thermal interface material pad.



(a) (b) (c)

Figure 41: Developed system for regulating the autonomous LED light. (a) Top view and (b)-(c) side views.

3.4.4 Online Connectivity

The purpose of an online data acquisition system is to optimize the energy consumption of the autonomous light, through accurate weather forecast. At the same time, the internet connection offers the possibility to store useful data, such as power production/consumption per lighting system, temperature and humidity measurements, number of users/people passing from the installation area and more.
The complete wireless connection system is presented in Figure 42. As can be seen, two microcontrollers (MCU) are needed:

- the first MCU is a Texas Instruments F28035 that regulates the operation of the entire system (*master*). It is responsible for controlling the power conversion stages, the indication LEDs, the air-circulating fans and collecting all measurements (analogue signals). The numerous peripherals of the F28035 (PWM generators ADC modules, I^2C bus, etc.) render it ideal for industrial applications.
- The second MCU is an ESPRESSIF ESP32, which has a WiFi/Bluetooth module and is used to establish the online connectivity with the weather forecast database and the data collection server.

The two MCUs are linked with an I^2C bus to share all measurements and with 3 unidirectional lines for digital indications. Even if the system becomes more complicated, the use of two microcontrollers is necessary to decouple the two function and ensure reliable operation even when no connection is available. Additionally, the ESP32 doesn't have enough analogue pins for the required measurements when the Wi-Fi is on.

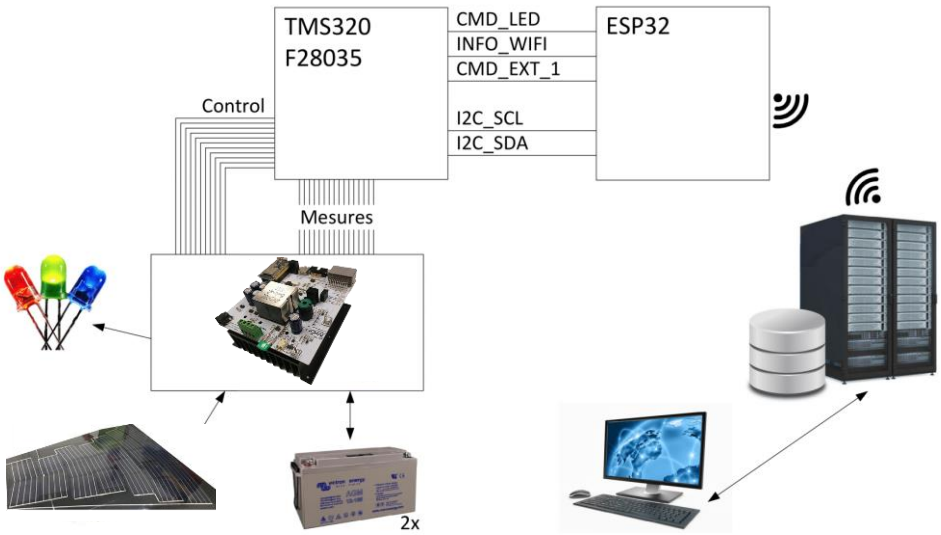


Figure 42: Overview of the Wi-Fi communication system.

The realization of the online connectivity (from the ESP32) can be divided in 3 task: 1) Communication between the microcontrollers, 2) WiFi connectivity to get the weather forecast and execute the energy saving algorithm and 3) Web-Page and database development for storing and presenting the collected information. These tasks are implemented with the firmware code, an overview of which is presented in Figure 43.
In the main loop the I^2C is performed and the three digital lines connected to the TI MCU1 are written/read. The Wi-Fi code is executed synchronously under the module *realTime* and the *algoBattery* is calculated for the energy saving function.

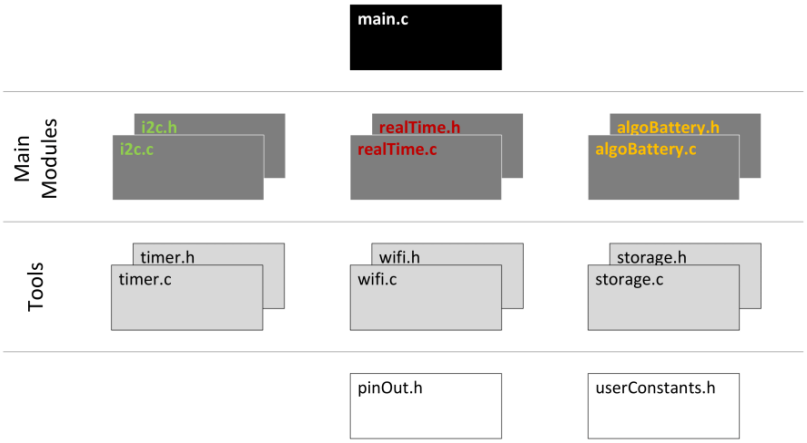


Figure 43: Basic structure of the online connectivity code.

Microcontrollers Communication

The I2C protocol 5 allows serial communication using only two lines : one for the clock (SCL) and the other for the data (SDA). More than two devices can be connected to the bus, but each transfer takes place between two of them. The devices are either slaves, with a distinct address, or masters. Only the masters (TI in our case) can begin a communication, given that the bus is free.

As shown in Figure 44, three kinds of data are transferred through the I^2C bus:

- measurements taken every 10 minutes:
  - Battery Voltage
  - Battery State of Charge (SoC)
  - Battery Temperature
  - PV Power Production
  - LED Power Consumption
  - Battery Power Transfer
- measurements taken every day
  - Daily Energy Production from the PV Generator
  - Daily Energy Consumption of the LED
- LED light intensity, given as a duty cycle variable, which determines the system energy consumption.

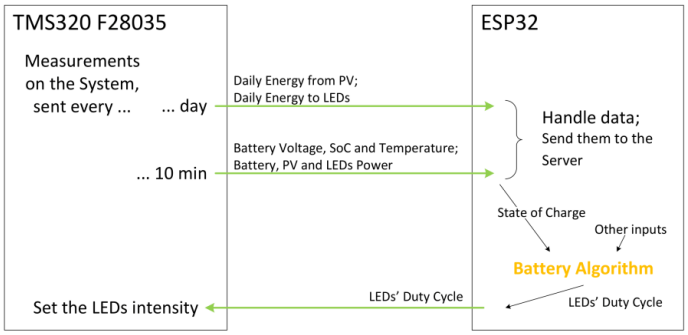
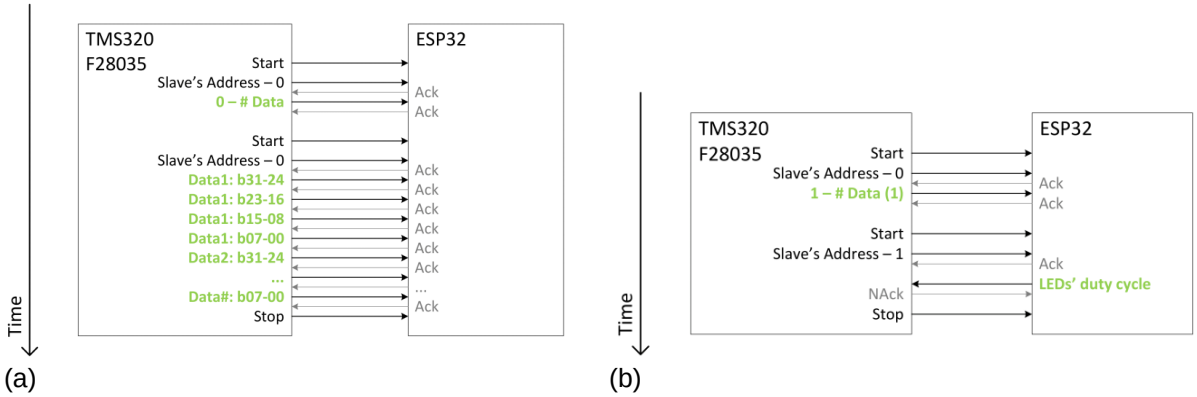


Figure 44: Data transferred through I^2C bus.

At the beginning of the communication, the master resets the data line when the clock is highs. From this moment, the master makes the clock line oscillate and sends a byte containing the slave's address followed by a bit-value at the list significant bit (LSB): 0 for sending data or 1 for receiving data. The slave generates a bit of acknowledge after each received byte. If this is omitted, the master considers that the slave didn't receive the byte, and it stops writing data. Then, the master can continue sending other bits until the end of the communication, when a stop signal is set (both data line and clock go high). The entire process of data transmitting (from TI to ESP32) is depicted in Figure 45(a). Similarly the process of receiving data (only the LED intensity duty cycle value) is shown in Figure 45(b). The only parameters that change are the MSB of the indicative byte and the number of data to send (only 1 byte).Also the master now generates a bit of acknowledge after each received byte. All operations are done synchronously, through interrupts that are carefully timed to allow a full transmission of all data from one microcontroller to the other, as seen in Figure 45(c).



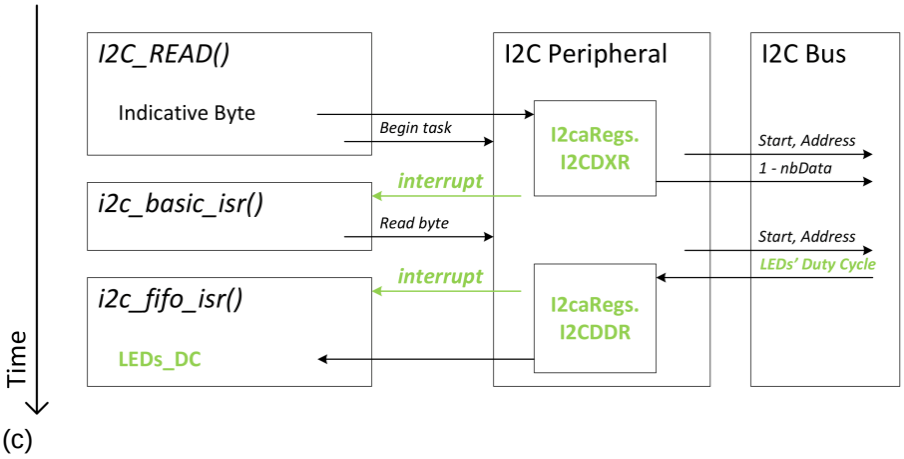


Figure 45: (a) Transfer of measurements form TI to ESP32. (b) Receiving the LED intensity duty cycle from ESP32 to TI MCU. (c) Synchronous I^2C operation from the TI side.

WiFi Connectivity

ESP32 Wi-Fi peripheral can work in station mode, in access point mode or in a combined mode. In this project, the MCU connects to an access point. The program was implemented for WPA2-Personal protocols for secure communication with local username and password. The WiFi module works synchronously through interrupts, as shown in Figure 46(a). For connection to the server, the HTTP protocol was used, as in Figure 46(b), which means that an HTTP client must first be created before a request is called from the ESP32 MCU.

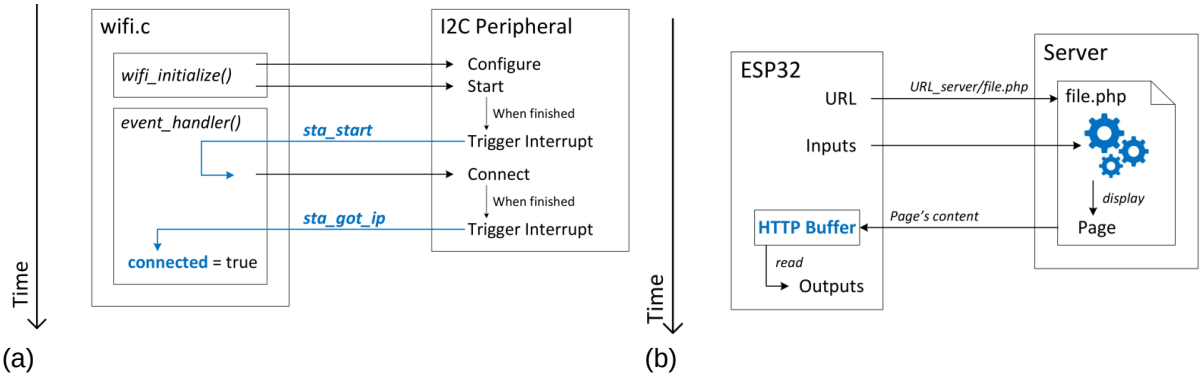


Figure 46: (a) Transfer of measurements form TI to ESP32. (b) Receiving the LED intensity duty cycle from ESP32 to TI MCU. (c) Synchronous I^2C operation from the TI side.

Energy Saving Algorithm

This algorithm is executed continuously in the ESP32 MCU and regulates the system energy consumption, by defining the intensity of the LED light, in the form of a duty cycle value. The algorithm needs as inputs the state of charge of the battery (calculated in the TI MCU through measurements) and the irradiance forecast, taken from the online database *Meteotest*. More specifically the *SolarForecast* was used in this project, which gives the irradiance (global and on an inclined plane) and temperature predictions for one week. The daily energy that the system needs to receive is computed by (19). In this function, all hourly predicted powers are summed and stored and the nominal energy consumed by the LED is subtracted.

$$Energy_i = \sum_{\forall hours/day_i} P(PV) - \Delta T_{night-i} \cdot \min\left(P(LED)\right) \quad (19)$$

If the sum of the available energy over the next 5 next days is positive, the excess energy can be equally distributed within the 5 upcoming days and allow the LED to light in higher intensity. If, on the other hand, the sum is negative, the LED duty cycle is reduced in order to meet the minimum battery state of charge requirements at the 5th day. This process is graphically depicted in Figure 47. The predictions and measurements are continuously adjusted and the duty cycle is updated every 10 minutes. An alert mechanism can be added when Meteotest forecasts critical weather, like too high or low temperature for the battery, strong wind or snowfall.

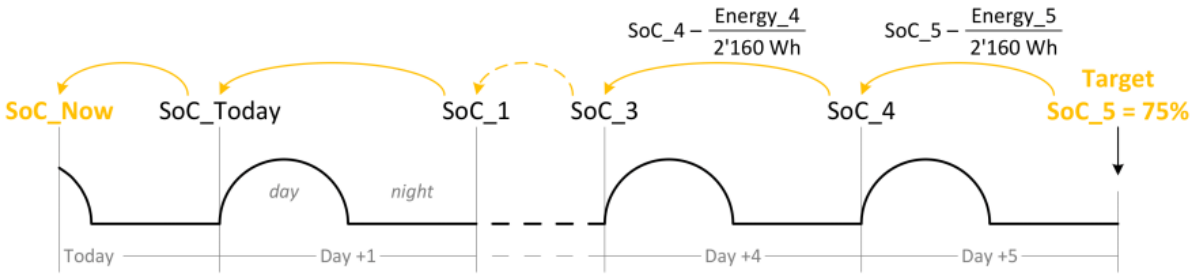


Figure 47: Energy saving algorithm process

A *Real Time Clock* is also implemented in the code to precisely know the duration that the LED needs to light. A *timer peripheral* was used for this purpose that was reset every day at sunrise, through the information acquired from the weather forecast server. The time was expressed in seconds from midnight. The update rate of the timer was set to 2048 Hz to minimize the clock lateness within one day. It is estimated that in 24h the maximum delay will be less than one second.

3.4.5 Data Acquisition – Server

The server hosts one web pages for the ESP32 and one for the users. It is also linked to a database to store useful information, such as the extracted measurements. The microcontroller page is implemented on PHP functions, the database is developed with MySQL and the webpage, accessible by the users, is structures in HTML and contains plots that graphically dhow the measurements done on the system.

The database contains 2 tables, which include the measured values and divided by their frequency of acquisition, as shown in Figure 48. More specifically, the table named *streetlights_10min* stores data only for 4 consecutive days; the old data are deleted. On the other hand, the *streetlights_daily* never erase data in order to keep an overview on the system for a long period. A simple PHP algorithm is developed to store the new information in the database when the ESP32 gives the respective request.

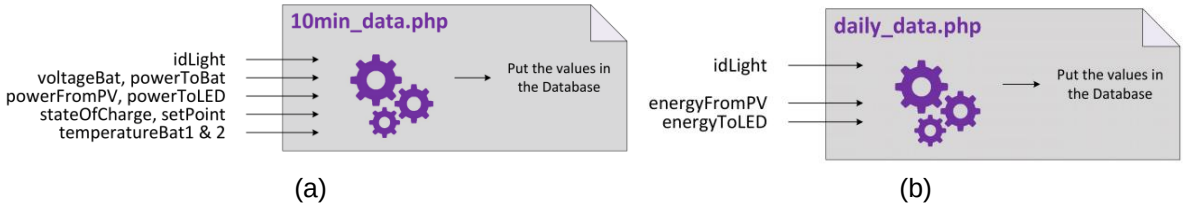
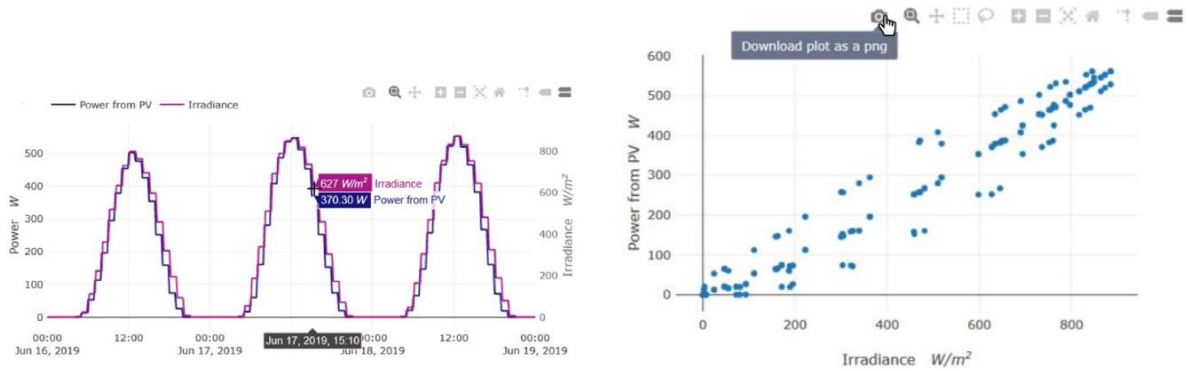


Figure 48: Measurements stored in the database Data captured every (a) 10min and (b) one day.

3.4.6 Demonstration

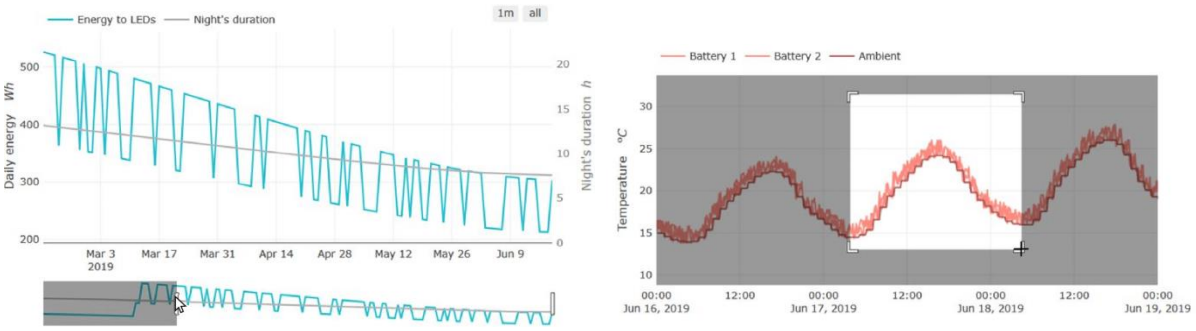
A webpage that includes and displaces all valuable measurements was developed. Its purpose is to show the database content with interactive plots, made in *Plotly JavaScript Library*. A few examples of these plots are presented here.
The produced PV power with respect to the irradiance is shown in Figure 49, which indicates that when the user is moving the cursor over the curve, values for the nearest point appear. At the top of the plot, a tool bar can be used to zoom, to change the axis or to export the plot as an image, as can be seen in Figure 49(b).



(a) (b)

Figure 49: (a) Power received form PV and Irradiance for 4 consecutive days (b). X-Y plot of the same data.

Since the time axis for the daily data is not limited, a range selector was added for these plots (see Figure 50(a)). Clicking and moving the cursor on the plot allows zooming, as demonstrated in Figure 50(b). Depending on the direction that the cursor moves, zoom along each axis or in a box can be performed.



(a) (b)

Figure 50: (a) Energy consumption by the LEDs for every day since the beginning of the measurements. (b) Battery and ambient temperature variation.

4 Conclusions

This project has led to a significant advancement of the GaN power electronics technology, due to our bottom-up approach, starting from the physics level, all the way up to the system level. Our main goal was to investigate and demonstrate novel concepts that can lead to large energy saving in two main directions: solar and street lighting applications. From an early stage we realized that GaN technology has the potential to revolutionize energy conversion; but in order to take full advantage of the new material we had to revisit the fundamentals of power electronics, search for new topologies and reconsider the entire system design.

GaN-based magnetic-less DC/DC converters

We focused our attention on magnetic-free GaN converters, which showed remarkable efficiency (>99% per cell) and outstanding power density (> 11 kW/l), due to the small footprint of GaN HEMTs and the absence of magnetic components. The developed bidirectional 10x converter was constructed with 20 commercial GaN transistors and showed a flat efficiency curve up to 2.5 kW. We then combined each of these converters with one PV panel of 250W to form a non-regulated, high voltage PV module. This allowed us to connect all PV modules in parallel, thus addressing the effects of partial shading, which accounts for up to 20% energy loss in residential rooftop/ façade PV systems with low installation height. Since these converters have a fixed step, we added a secondary DC/DC stage in order to introduce controllability of the operating point of all PV modules simultaneously.

It is important to note that the proposed converter can be directly used to other applications with large energy requirements, such as data centers or electric vehicles charging. This fact creates the basis for further investigation of such topics in future projects.

Near-Junction Microfluidic Heatsinks

In parallel, we developed novel liquid-cooling systems, co-designed with the power electronics, to address the high heat fluxes associated with the large energy transfer in a small GaN footprint. We performed a thorough mathematical analysis to optimize the cold plates in terms of microchannel width flow rate and pressure drop. We perfumed finite element method (FEM) simulations to determine how the micro-channel architecture and the liquid distribution manifold affects the cooling process. We increase the reliability of our liquid cooling circuit by developing a monolithic coolant distributors (3D printed and CNC milled aluminum) and selecting appropriate filters to prevent clogging of the microchannels. We believe that the transistor heat-up is going to be the limiting factor in future power electronics applications and our approach of co-designing the electronics with a dedicated cooling system will serve as an effective solution.

Monolithic integrated GaN power ICs

One of the most exciting and novel aspects of this project was the development of monolithically integrated power converters on a single GaN chip in our laboratory. We got motivated by the exceptional performance of the magnetic-free DC/DC converters and moved on demonstrating a similar concept with our devices integrated on the same substrate. We first developed scaled-up Schottky barrier diodes and investigated their switching performance through a double pulse tester (DPT). We then combined four of these diodes on single chip and demonstrated the first monolithic GaN full bridge rectifier. We also evolved our idea of the micro-fluidic cooling and etched microchannels directly at the substrate of the device. Instead of a manifold, the liquid distribution was performed inside the PCB. We tested the system up to 120W and 100V, while the device temperature was kept bellow 60 ^{o}C.

In the same context we lately developed a fully integrated 8x voltage multiplier based on our high-performance SBDs. This is a first demonstration that the function of the magnetic-free converter can be performed by a single chip.

5 Outlook and next steps

Our lab will keep working on this promising field of magnetic-free power converters and the potential of integrating multiple devices on a single chip, since we believe such systems could have a large impact on future energy market.

In future work, we aim to provide appropriate power-up and shut-down procedures for a safe and reliable operation of all our capacitor-clamped circuits (both with discrete transistors and integrated diodes). We also plan to move forward with the integration of several transistors on the same chip and add more functionalities, such as gate drivers and protection circuitry. Our ultimate goal is to replace all 20 transistors of the magnetic-free converter with a single power IC developed in our laboratory, and increase even further the power density, efficiency and reliability of such systems.

6 National and international cooperation

To execute this project, we have established collaborations at a national level with companies and laboratories, such as Schrèder and Microcity Lab in Neuchatel. More specifically, the architectural design of the autonomous street light (section 3) was performed in close collaboration with the Aebischer & Bovigny company, based in Lausanne, while the fabrication of the PV prototype was performed in the Microcity Lab. In addition, we are currently establishing collaboration projects with other large semiconductor Swiss company such as ABB. We have also established collaborations with a Swiss company Montena to design high power pulse generators.

We have also established collaborations in the international level with Texas instruments, which continuously provide us with Silicon-based circuit demonstrators and workshops. In particular, they have kindly presented a workshop about Power Lab Management Kits for power supply design at EPFL, which benefited several students in educating them on the design of power supply. In addition, they have supplied us with several kits for our Master students, including a solar inverter kit which help us to understand the important parameters of current designs.

This project was a major enabler for us to establish major collaboration with large European companies and laboratories, through an European Union H2020 ECSEL projet (UltimateGAN), which awarded 48M Euros for 26 partners in Europe.

7 Communication

Our work attracted a lot of attention both from the research community and industry. We presented our work in the international conference IEEE APEC, where we were granted the best presentation award. Our work was also featured in the prestigious *IEEE power electronics magazine* with a dedicated article. We disseminated our results through 3 publications in high impact factor journals (see next Section) and we currently have 5 more papers under review. We also communicated our work to the general public by taking part in the "*EPFL open doors*", a festival for celebrating the 50 years of EPFL.

8 Publications

During the past year, 5 papers related to this project were published and 5 more are currently under review.

Published paper:

[D.1] L. Nela, G. Kampitsis, J. Ma and E. Matioli, “Fast-switching Tri-Anode SBDs for monolithically integrated GaN-on-Si power circuits”, *IEEE Electron Device Letters*, Dec. 2019.

[D.2] R. Faraji, H. Farzanehfard, G. Kampitsis, M. Mattavelli, E. Matioli and M. Esteki, “Fully Soft-Switched High Step-up Non-Isolated Three-Port DC-DC Converter Using GaN HEMTs” acceoted for publication in IEEE Transactions on Industrial Electronics, Nov. 2019.

[D.3] J. Ma, G. Kampitsis, P. Xiang, K. Cheng and E. Matioli, “Multi-Channel Tri-Gate GaN Power Schottky Diodes With Low ON-Resistance”, *IEEE Electron Device Letters*, Vol.40 No. 2, Feb 2019.

[D.4] G. Kampitsis, Remco van Erp and E. Matioli, “Ultra-High Power Density Magnetic-less DC/DC Converter Utilizing GaN Transistors”, in IEEE APEC, CA USA, May 2019

[D.5] Remco van Erp, G. Kampitsis and E. Matioli, “A manifold microchannel heat sink for ultra-high power density liquid-cooled converters”, in IEEE APEC, CA USA, May 2019

Papers under review:

[D.6] G. Kampitsis, E. Batzelis, R. van Erp and E. Matioli, “Parallel PV Configuration with Switched-Capacitors Module-Level Converters for Partial Shading Conditions”, *IEEE Transaction on Sustainable* Energy, under review.

[D.7] R. van Erp, G. Kampitsis and E. Matioli, “Efficient Microchannel Cooling of Multiple Power Devices with Compact Flow Distribution for High Power-Density Converters”, *IEEE Transactions on Power Electronics*, under review.

[D.8] N. Perera, G. Kampitsis, J. Ancay, M. Samizadeh, R. van Erp and E. Matioli “Sawyer-Tower Circuit for Large-Signal Coss Analysis: Technical Considerations”, *IEEE Journal of Emerging and Selected Topics in Power Electronics*, under review.

[D.9] R. van Erp, G. Kampitsis, L. Nela, R. Soleimanzadeh and E. Matioli, “Embedded Microfluidic Cooling for High Power-Density GaN Power Integrated Circuits”, in *IEEE ITHERM 2020*, under review.

[D.10] [D.8] L. Nela, G. Kampitsis, H. K. Yildirim, R. van Erp, J. Ma and E. Matioli, High-Frequency GaN-on-Si power integrated circuits based on Tri-Anode SBDs, in *IEEE ISPSD 2020*, under review.

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