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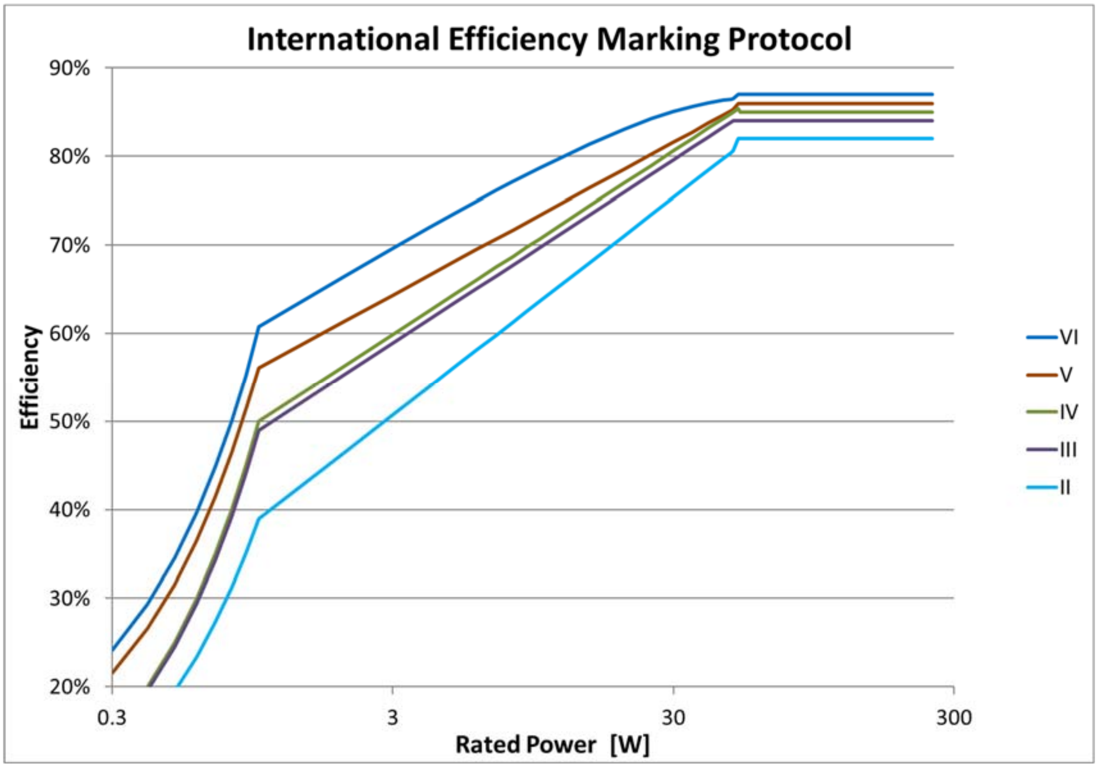
Final report

Best Available Technology of Switching Power Supplies Concerning Efficiency



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The author of this report bears the entire responsibility for the content and for the conclusions drawn therefrom.

Zusammenfassung

Gegenstand dieser Untersuchung ist das Potential zur Effizienzsteigerung und Reduktion der Standby-Verluste externer Schaltnetzteile mittels der besten heute verfügbaren Technologie. Diese optimale Technologie wurden aus Sicht der Schaltungstopologien, als auch aus Sicht der Halbleiterkomponenten analysiert. Der Fokus lag dabei auf den neuen Wide Band Gap Werkstoffen. Hier verspicht vor allem Galliumnitrid gute Resultate. Im Gegensatz dazu bringt Siliziumkarbid für die betrachteten Anwendungen kaum Vorteile.

Die gesetzlichen Bestimmungen in Europa und den Vereinigten Staaten bezüglich Wirkungsgrad und Standby-Verlusten wurden untersucht und dienen als hauptsächliche Referenz. Die technischen Möglichkeiten wurden vorwiegend analytisch evaluiert und zum Teil durch Messungen ergänzt. Eine Auswahl bestehender Geräte wurde getestet und einem Vergleich mit den normativen Anforderungen unterzogen.

Die Resultate zeigen, dass vor allem bei Geräten sehr kleiner Leistung, d.h. unter ca. 10 W mit den gegenwärtig besten verfügbaren Technologien ein realistisches Potential vorhanden ist, um die bestehenden Normen zu straffen. Möglichkeiten wurden vor allem auch beim Standby-Verbrauch festgestellt. Im höheren Leistungsbereich besteht ebenfalls die Möglichkeit einer Steigerung der Performance, die es erlauben würde, der zurzeit noch als Empfehlung geltende Code of Conduct, Version 5, Tier 2 zur zwingenden Norm zu erklären. Dieser Schritt war ursprünglich bereits auf Juli 2018 vorgesehen, wurde aber bis dato nicht umgesetzt.

Eine weitere Verschärfung der Anforderungen scheint möglich, bedeutet aber den Einsatz von Technologien, für welche die Industrietauglichkeit noch abschliessend zu bewiesen ist.

Summary

The goal of this investigation was to evaluate the potential of the best available technology with regard to improving the efficiency and standby losses of external power. The prospects with respect to the optimal circuit topology, as well as, the most favorable semiconductor materials were evaluated. In the latter case, the focus was placed on the new wide band gap materials. Particularly, gallium nitride yields promising results, while silicon carbide offers hardly any advantage for the applications considered.

The current legislation in Europe and the United States regulating efficiency and standby losses was analyzed and served as references. The technical feasibilities were primarily evaluated analytically and complemented with some measurements. A limited number of existing products were tested against the current limits.

Particularly at low power, i.e., below approximately 10 W, the results indicate, that the currently best available technology provides a realistic potential to tighten the current legislation. This applies in particular to the standby losses. An improved performance is also possible at higher power levels, which would allow declaring the Code of Conduct, Version 5, Tier 2 as law. Currently, these limits are published as a voluntary guideline. Legislation to this effect was originally scheduled for July 2018, however, it has not been implemented as of the writing if this report.

Restricting the rules even further appears possible, but it requires the implementation of technologies, for which the suitability for series production must be validated first.

Contents

1 Introduction

1.1 Scope

This report focuses on the power losses and relating standards of external power supplies (EPS). External power supplies are devices used to convert household electric voltage into DC voltage (or lower AC voltage) to operate a consumer product. These include power supplies for a wide variety of household and office products, such as notebooks, tablets, smartphones, displays, tv-sets, printers, routers, modems, cameras, handheld tools and musical instruments, just to name a few examples. The conversion efficiency has historically been relatively low, where the definition of what low means, depends on the power level.

In 2009 it was estimated that in Europe alone the power consumption due to conversion losses and standby losses of EPS amount to 17 TWh annually, with a predicted increase to 31 TWh by 2020, if no regulatory action is taken to reduce these losses [1]. 31 TWh corresponds to roughly half of Switzerland’s total annual electricity consumption. Similar considerations have prompted the California Energy Commission CEC to set forth efficiency standards as early as 2004, which became law in 2006. The main driving forces behind such legislation are the European Union and the United States of America. Additional countries have adopted these rules, such as Switzerland, Canada and Australia.

1.2 International Efficiency Marking Protocol for External Power Supplies

The US Environmental Protection Agency (EPA) has developed performance levels for the efficiency and standby power of EPS. Today, the Department of Energy (DOE) maintains this protocol. Thus, in this document, these levels are referred to as DOE levels. They are to some degree harmonized with international efforts to reduce power losses, in particular with standards developed by the European Union. The levels are marked with roman numerals ranging from I to currently VI and can be extended further in the future. The respective level is printed on the nameplate of the EPS.

The specified efficiency refers to an average taken at 25 %, 50 %, 75 % and 100 % of the nameplate power. At levels V and VI somewhat relaxed efficiency requirements apply for EPS with low output voltage. Low voltage refers to outputs lower than 6 V and at the same time currents greater or equal to 550 mA. Also at level V standby power limits for EPS with alternating current (AC) outputs are defined separately.

Table 1: International efficiency marking protocol [4]

Mark	Nameplate Output Power P_n	Average Efficiency1[1]	Nameplate Output Power P_n	Standby Power [W]
I	Used if no standards are met.			
II	$0 \leq P_n < 1$ W	$\geq 0.39 \cdot P_n$	$0 \leq P_n \leq 10$ W	≤ 0.75
	$1 \leq P_n < 49$ W	$\geq 0.107 \cdot \ln(P_n)+0.39$	10W $< P_n \leq 250$ W	≤ 1
	49 W $< P_n$	≥ 0.82		
III	$0 \leq P_n \leq 1$ W	$\geq 0.49 \cdot P_n$	$0 \leq P_n <$ 10W	≤ 0.5
	1 W $< P_n <$ 49 W	$\geq 0.09 \cdot \ln(P_n)+0.49$	10 W $\leq P_n \leq$ 250 W	≤ 0.75
	49 W $< P_n \leq$ 250 W	≥ 0.84		
IV	$0 \leq P_n < 1$ W	$\geq 0.5 \cdot P_n$	$0 \leq P_n \leq 250$ W	≤ 0.5
	$1 \leq P_n \leq 51$ W	$\geq 0.09 \cdot \ln(P_n)+0.5$		
	51 W $< P_n \leq$ 250 W	≥ 0.85		
V	$0 \leq P_n \leq 1$ W	BV[2]: $\geq 0.48 \cdot P_n+0.14$ LV: $\geq 0.497 \cdot P_n+0.067$	$0 \leq P_n < 50$ W	DC[3]: ≤ 0.3 AC: ≤ 0.5
	1 W $< P_n \leq$ 49 W	BV: $\geq 0.0626 \cdot \ln(P_n)+0.622$ LV: $\geq 0.075 \cdot \ln(P_n)+0.561$	50W $\leq P_n \leq$ 250 W	≤ 0.5
	49 W $< P_n \leq$ 250 W	BV: ≥ 0.87 LV: ≥ 0.86		
VI	Single Voltage			
	$0 \leq P_n \leq 1$ W	BV: $\geq 0.5 \cdot P_n+0.16$ LV: $\geq 0.517 \cdot P_n+0.087$	$0 \leq P_n \leq 49$ W	DC: ≤ 0.1 AC: ≤ 0.21
	1 W $< P_n \leq$ 49 W	BV: $\geq 0.071 \cdot \ln(P_n)-0.0014 \cdot P_n+0.67$ LV: $\geq 0.0834 \cdot \ln(P_n)+0.\ 0014 \cdot P_n+0.609$	49 W $< P_n \leq$ 250 W	≤ 0.21
	49 W $< P_n \leq$ 250 W	BV: ≥ 0.88 LV: ≥ 0.87	250 W $< P_n$	≤ 0.5
	250 W $< P_n$	≥ 0.875		
	Multiple Voltage			
	$0 \leq P_n \leq 1$ W	$\geq 0.497 \cdot P_n+0.067$	any	≤ 0.3
	1 W $< P_n \leq$ 49 W	$\geq 0.075 \cdot \ln(P_n)+0.561$		
	49 W $< P_n$	≥ 0.86		

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[1] Efficiency averaged over 25 %, 50 %, 75 % and 100 % of nameplate power.

[2] LV → Low Voltage: nameplate output voltage less than 6 V and current greater or equal to 550 mA.
BV → Basic Voltage: all other cases.

[3] Standby power limits at level V and VI distinguish between EPS with DC and AC output.

1.3 European Efficiency Requirements and Standby Power Limits

The European Commission issued regulation (EC)278/2009 on April 6, 2009 [1], which went into effect two years later in 2011. The regulation is almost identical to DOE Level V. The differences are:

- The boundary between the first and second power range is set at 51 W as opposed to 49 V in the DOE rules.
- Separate values for the no load losses at basic voltage and low voltage outputs are defined.

Table 2: European limits

Nameplate Output Power P_n	**Average Efficiency**[4]	**Efficiency at $0.1 \cdot P_n$**	**Nameplate Output Power P_n**	**Standby Power [W]**
Regulation (EC)278/2009, April 6, 2009 corresponds to DOE Level V with minor differences		Based on Code of Conduct, Version 4 As of Oct. 2018 mandatory standard in EU		
$0 \le P_n \le 1$ W	BV[5]: $\ge 0.48 \cdot P_n + 0.14$ LV: $\ge 0.497 \cdot P_n + 0.067$		$0 \le P_n < 51$ W	BV,DC: ≤ 0.3 BV,AC: ≤ 0.5 LV: ≤ 0.3
1W $< P_n \le 51$ W	BV: $\ge 0.063 \cdot \ln(P_n) + 0.622$ LV: $\ge 0.075 \cdot \ln(P_n) + 0.561$		51W $< P_n$	BV: ≤ 0.5 LV: ≤ N/A3
51W $< P_n$	BV: ≥ 0.87 LV: ≥ 0.86			
Code of Conduct, Version 5, October 29, 2013:		**Tier 1**		
$0 \le P_n \le 1$ W	BV: $\ge 0.5 \cdot P_n + 0.146$ LV: $\ge 0.5 \cdot P_n + 0.086$	BV: $\ge 0.5 \cdot P_n + 0.046$ LV: $\ge 0.5 \cdot P_n$	0.3 W $\le P_n < 49$ W	≤ 0.15
1 W $< P_n \le 49$ W	BV: $\ge 0.0626 \cdot \ln(P_n) + 0.646$ LV: $\ge 0.0755 \cdot \ln(P_n) + 0.586$	BV: $\ge 0.0626 \cdot \ln(P_n) + 0.546$ LV: $\ge 0.072 \cdot \ln(P_n) + 0.5$	49 W $\le P_n <$ 250W	≤ 0.25
49 W $< P_n \le$ 250W	BV: ≥ 0.89 LV: ≥ 0.88	BV: ≥ 0.79 LV: ≥ 0.78	Mobil handheld: $P_n < 8$ W	≤ 0.075
Code of Conduct, Version 5, October 29, 2013:		**Tier 2**		
$0 \le P_n \le 1$ W	BV: $\ge 0.5 \cdot P_n + 0.169$ LV: $\ge 0.517 \cdot P_n + 0.091$	BV: $\ge 0.5 \cdot P_n + 0.06$ LV: $\ge 0.517 \cdot P_n$	0.3 W $\le P_n < 49$ W	≤ 0.075
1W $< P_n \le 49$ W	BV: $\ge 0.071 \cdot \ln(P_n) - 0.00115 \cdot P_n + 0.67$ LV: $0.0834 \cdot \ln(P_n) - 0.0011 \cdot P_n + 0.609$	BV: $\ge 0.071 \cdot \ln(P_n) - 0.00115 \cdot P_n + 0.57$ LV: $\ge 0.0834 \cdot \ln(P_n) - 0.00127 \cdot P_n + 0.518$	49 W $\le P_n <$ 250W	≤ 0.15
49 W $< P_n \le$ 250W	BV: ≥ 0.89 LV: ≥ 0.88	BV: ≥ 0.79 LV: ≥ 0.78	Mobil handheld: $P_n < 8$ W	≤ 0.075

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[4] Efficiency averaged over 25 %, 50 %, 75 % and 100 % of nameplate power.

[5] Low Voltage: $V_{out} < 6$ V and $I_{out} > 550$ mA; Basic Voltage otherwise

On October 29, 2013 the European Commission issued Version 5 of the Code of Conduct (CoC) on Energy Efficiency of External Power Supplies [2]. Two sets of values are defined, referred to as Tier 1 and Tier 2.

Effective dates as voluntary code of conduct (not as mandatory requirement):

- Tier 1: January 1, 2014
- Tier 2: January 1, 2016

It is expected that Tier 2 will become mandatory in the near future. The original plan was January 2017 for Tier 1 and July 2018 for Tier 2 [3]. However, neither of the two has become law as of the writing of this report.

A comparison of these requirements with DOE Level VI, the current mandatory US standard, reveals that there are some differences. They are:

- The CoC introduces an additional requirement for the efficiency at 10 % of the rated power.
- At rated power greater than 49 W: CoC Tier 1 and Tier 2 are more stringent than Level VI.
- At rated power smaller than 49 W: CoC Tier 1 is more relaxed then Level VI, whereas Tier 2 is almost identical to Level VI.
- Standby power limit: CoC Tier 1 is more relaxed and Tier 2 is more stringent than Level VI.

The DOE level VI distinguishes between direct and indirect operation products. A direct operation EPS is a device that can be operated without the assistance of a battery, irrespective of whether the battery can actually be removed or not. In an indirect operation product the battery must be present in order to work. Level VI only applies to direct operation EPS, whereas indirect operation EPS fall under the category battery charger, where the less restrictive Level V rules apply [5].

1.4 Timeline

2004	The California Energy Commission (CEC) defines their Tier 1 efficiency standards which became DOE Level III.
2005	Energy Star V 1.1 is introduced, a globally recognized voluntary efficiency program according to Level III.
	The European Union approves Directive 2005/32/EC establishing rules for the so-called eco-design. External power supply efficiencies are not yet regulated within this framework [6].
2006	In California DOE Level III becomes mandatory.
2008	The USA enacts the Energy Independence and Security Act (EISA), which implements the CEC Tier 2 requirements, equivalent to DOE Level IV [7].
2009	Energy Star removes the external power supply category from its listing with the argument that it is part of an end-use product and should not be treated separately [8].
2010	The EU implements ErP Directive Phase 1, equivalent to DOE Level IV (ErP = energy related product).
2011	The USA and Europe implement Level V. In the USA as CEC Tier 3 and in Europe as ErP Phase 2. The external power supply requirements are defined in regulation (EC)278/2009 of April 6, 2009. This is the currently mandatory standard in Europe [1].
2014	The European Union publishes the voluntary code of conduct CoC Tier 1, which is more stringent than Level V limits [2].
2016	In the USA the DOE Level VI standard goes into effect. This is the currently mandatory standard in the USA [9].
	Europe introduces the CoC Tier 2 levels, which roughly corresponds to Level VI [2].
2018	Tier 1 and Tier 2 of the EU CoC are currently under review to become mandatory.

1.5 Currently Mandatory Standard Levels

Currently the following standards are mandatory in various countries.

USA: Level VI: Published by the Department of Energy. Effective since February 10, 2016

EU: Level V: Defined in regulation (EC)278/2009 of April 6, 2009. Effective since 2011.

Canada: Level IV: Implemented by Natural Resources Canada.

Australia: Level III: Minimum Efficiency Performance Standard MEPS (Level IV voluntary)

2 Comparison of Regulatory Limits

The following graphs compare the required efficiency levels according to Table 1 (DOE Levels in Figure 1) and Table 2 (European Levels in Figure 2) for basic and low voltage outputs. For the latter case the requirements are somewhat relaxed. Low voltage applies if the rated output voltage is less than 6 V and the rated current is greater than 550 mA. If only one out of the two criterions apply, the device is categorized as basic voltage.

In this discussion, the efficiency refers to an averaged value over four operating points at 25 %, 50 %, 75 % and 100 % of the rated power.

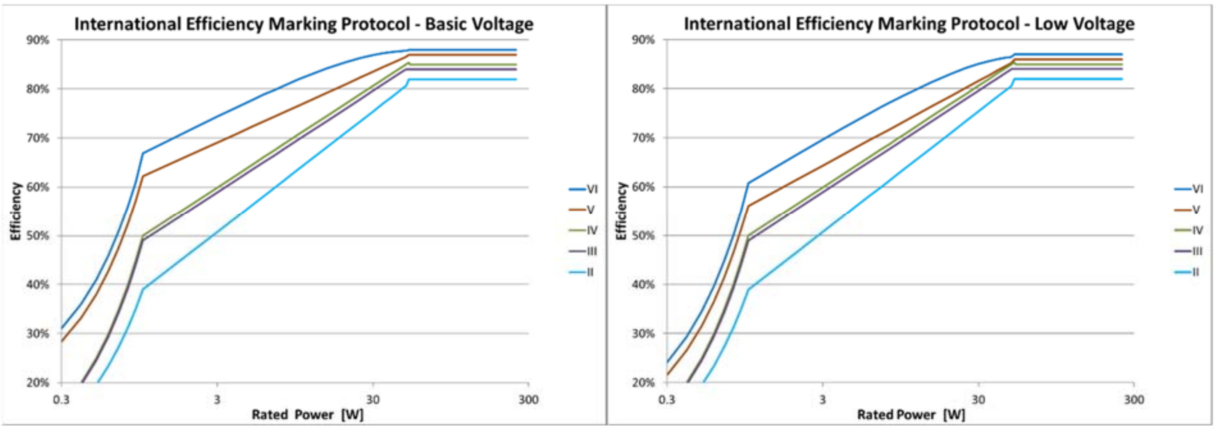

Figure 1: The internationally adopted efficiency levels for EPS (DOE levels), left: basic voltage; right low voltage

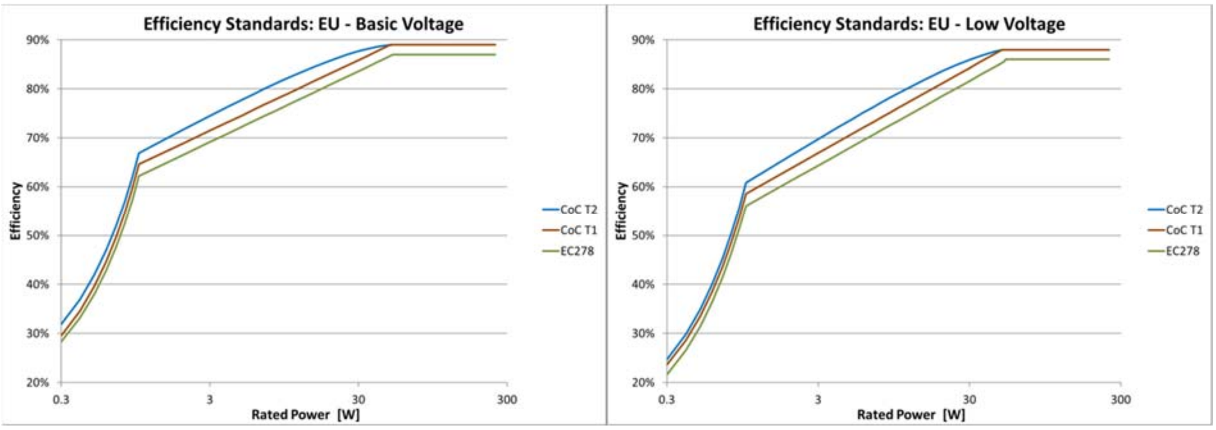

Figure 2: Mandatory European level ((EC)278/2009) and Code of Conduct, Version 5, Tier 1 and Tier 2.

A comparison of the currently mandatory values in the European Union with those applicable in the U.S. shows that the American standard is more stringent, particularly for EPS with a rated power in the range from 1 to 49 W, as shown in Figure 3. However, the EU Code of Conduct, Version 5, Tier 2 sets somewhat tighter limits than currently mandatory in the U.S. standard (Figure 4).

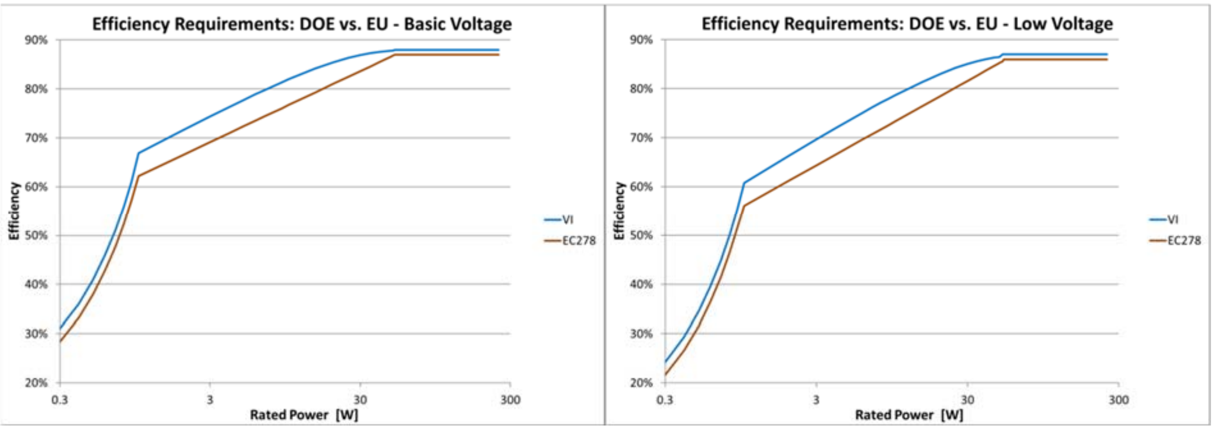

Figure 3: Comparison between mandatory levels in U.S. (DOE Level VI) and Europe ((EC)278/2009).

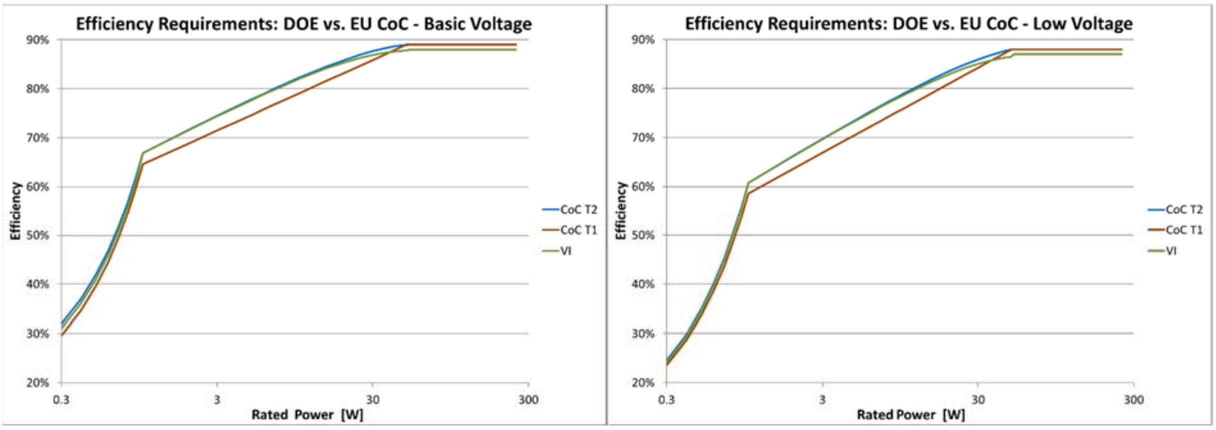

Figure 4: Comparison between mandatory level in U.S. (Level VI) and EU Code of Conduct, Tier 1 & 2.

The Code of Conduct additionally defines minimum requirements for the efficiency at 10 % of the rated power. The computed values are displayed in Figure 5.

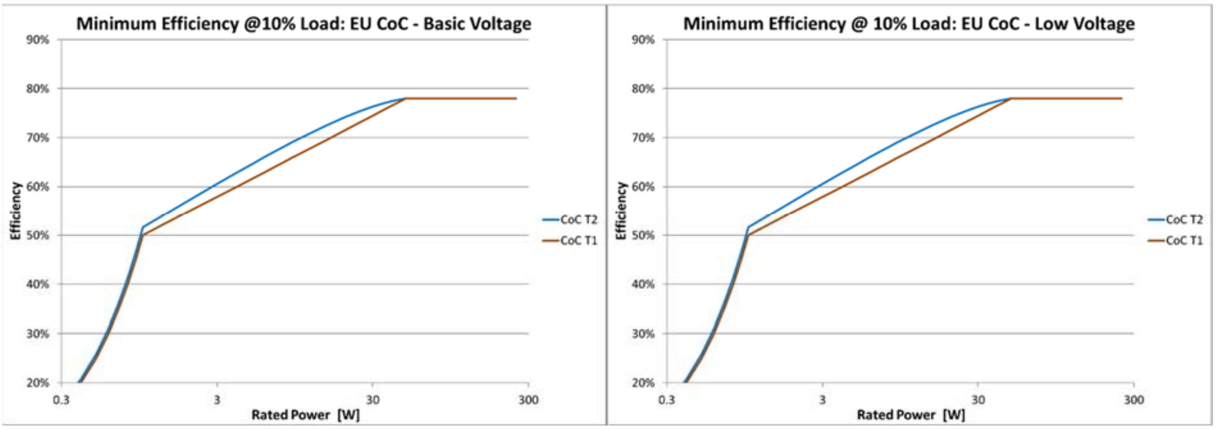

Figure 5: Required efficiency at 10 % of rated power according to EU Code of Conduct, Tier 1 & 2.

The following graphs show a similar comparison of the defined standby power limits. Figure 6, left displays the limits according to the International Efficiency Marking Protocol (DOE levels) and on the right the limits defined by the European Commission. Note the different standby power scales in the graphs on the left and right hand side.

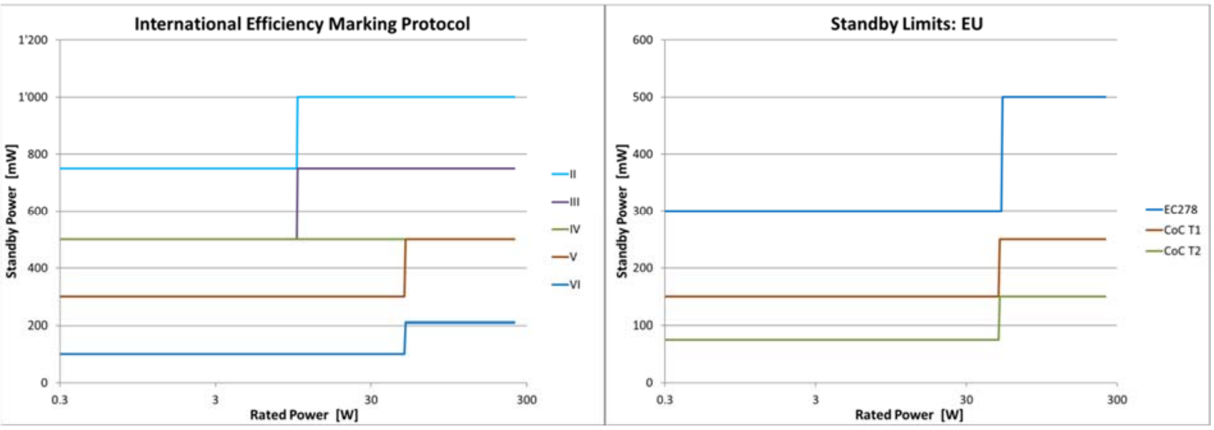

Figure 6: Standby losses according to DOE levels (left) and EU limits, including Code of Conduct.

Figure 7, left compares the currently mandatory standby power limits in Europe with those in the U.S., where the latter imposes much more stringent values. The comparison with the EU Code of Conduct results in a similar situation as with the efficiency. Tier 1 is more relaxed and Tier 2 is more stringent than the U.S. regulation.

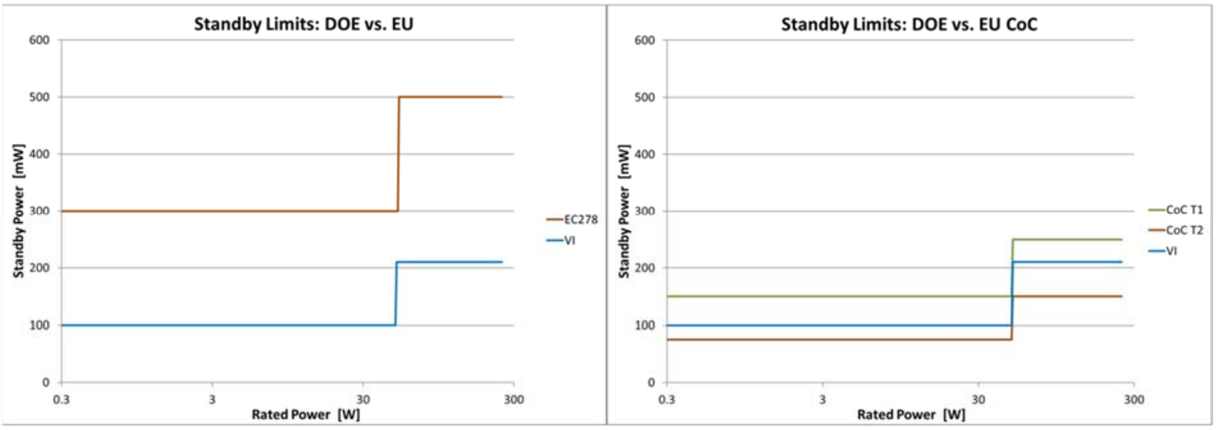

Figure 7: Comparison of standby limits between U.S. and EU, left: mandatory, right: Code of Conduct.

3 Analysis of Technology

3.1 State of the Art Applications

As the number of applications for EPS is extremely large, so manifold is the technology employed to realize these devices. A vast number of circuit topologies have been implemented in various designs and even a greater number has been proposed in technical literature. For the purpose of this investigation, the focus is placed on a few representative designs. To make a meaningful assessment, it must be distinguished between low power and high power EPS. A logical boundary between the two groups can be placed at 75 W. For power levels greater than 75 W an active power factor corrector function (PFC) must be implemented on EPS sold in most countries. This always increases the complexity, reduces the efficiency and increases the standby power losses. At power levels below 75 W an active PFC is not required by the current regulation. However, some EPS include it on a voluntary basis, if the rated power is close to 75 W.

3.2 Low Power EPS

3.2.1 Topologies

In the low power range a typical realization includes a passive full bridge rectifier, followed by a bulk capacitor which decouples the AC and DC sides. The bulk capacitor serves as input of an isolated switched mode converter. A very popular topology for this application is the flyback converter, as it provides the necessary functions quite naturally. A simplified circuit diagram of the power processing part is shown in Figure 8.

In its basic implementation this topology is not very efficient and would in most cases satisfy neither the EU nor the U.S. regulations. The main reasons are:

- The flyback transformer exhibits non-ideal magnetic coupling between the windings. This results in a leakage inductance L_σ, where energy is stored due to the currents in the windings. After the switching instant, this energy is dissipated in the clamp network consisting of D_5 and D_6. For topological reasons the energy loss per switching is much greater than the amount that can be calculated by $W = ½ I^2 L_\sigma$. This generally leads to considerable power losses.
- The principle of the flyback operation requires all of the converted energy to be stored at some time in the transformer. Magnetic energy storage, however, is much less efficient than for example the capacitive counterpart.
- Compared with other topologies, the apparent power on the main switch Q (the product of on-current and off-voltage) is larger than in other converters with similar power ratings. This leads the larger switching losses.
- The losses on the secondary diode D_7 can be quite significant. In devices with an output voltage of 5 V it alone causes an efficiency drop of 6 to 8 % at all power levels.

This gives rise to the question, as to why the flyback converter is so popular for such applications. There are also clear advantages:

- The simplicity of the circuit.
- It can easily deal with large conversion ratio ranges. Implementing universal input range (from 85 to 256 V) is easily possible.

Therefore, a number of modifications have been proposed over recent years. All of them are trying to alleviate some of the above listed drawbacks. Some extensions are visible in the (still simplified) circuit diagram in Figure 9; others are related to the mode of operation in combination with the design of the power components.

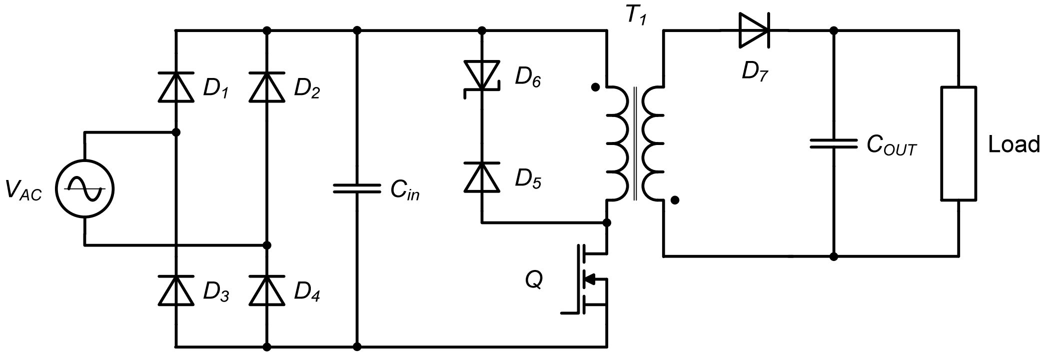

Figure 8: Typical off-line converter for low power applications (without PFC)

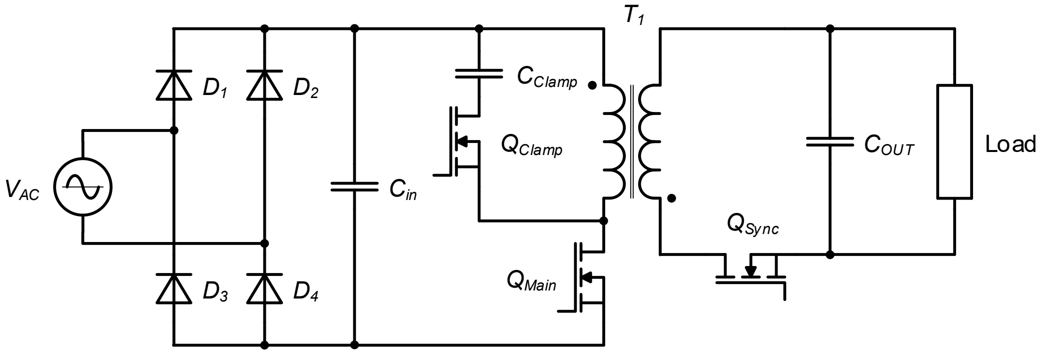

Figure 9: Off-line converter with active clamp and synchronous rectification

The topology shown above is an active clamp flyback converter with synchronous rectification. The following sources of power losses can be reduced with this circuit.

- The rectifier diode is replaced by an active switch Q_{Sync}, which leads to lower conduction losses.
- The energy stored in the leakage inductance is temporarily stored in the clamp capacitor C_{Clamp}, from where it can be recovered and recirculated into the circuit.
- Additionally, the active clamp allows the implementation of soft switching in order to reduce the switching losses. This requires a proper design of the passive components combined with a specific switching pattern between the three MOSFETs.
- Alternatively, other concepts, such as valley switching can be implemented to alleviate the switching loss issue.

These modifications, combined with an operation in burst mode at very light load, allow compliance with the efficiency standards with a flyback implementation. Other optimizations to the flyback converter have been published in recent years, with similar effects [10, 11].

Alternative approaches with other topologies suffer from problems coping with the wide input voltage range, even if they show higher efficiencies in many other applications. Once a forward converter is conditioned for universal input range from 85 to 230 Vac its advantage over the flyback is lost [12].

3.2.2 Loss Evaluation

The sources of individual loss contributions can be traced to distinct components and effects in the circuit. Below is a listing of the most important loss mechanisms, including an assessment of their relevance related the typical low power topology in Figure 9:

3.2.2.1 Conduction Losses at the Input Rectifier P_{rec}

The input rectifier is a major source of losses, especially at low line voltage, i.e. on 100 or 115 V grids. The losses can be calculated approximatively by:

$$P_{rec} = 2\,V_D \cdot \frac{P_{in}}{V_{ac,rms}}$$

where:

P_{in}: input power of the EPS

V_{ac}: line voltage

V_D: forward voltage drop on rectifier diodes

These losses are very comparable in all low power EPS, as the forward voltage drop V_D is the only parameter available to affect them. Line rectifiers have been in use for decades and the technology is well matured. The technical limits are reached. No improvement can be expected in near future.

New materials, such as silicon carbide do not provide better behavior. They exhibit clear advantages at very high frequencies, as they show a superior switching performance. This comes at the cost of a somewhat higher forward voltage drop V_D, which is higher than in silicon diodes. According to above formula this leads to higher conduction losses P_{rec}. At line frequency, i.e. 50 or 60 Hz, the low number of switching instants (only 100 or 120 per second, respectively) the better switching behavior is of no relevance, as the higher conduction losses clearly dominate.

There are topologies that can eliminate the input rectifier, or at least reduce the number of diodes from four to two [13,14,15,16]. These topologies, however, are always much more complex, with additional active switches that must be controlled. For low power devices discussed here, the necessary control and drive power might offset the intended power savings entirely or at least to a large degree. In addition, if implemented, the cost of low power EPS would increase unreasonably. Thus, it seems realistic to assume that in this power class, passive input rectification will remain the standard solution.

3.2.2.2 Conduction Losses in the Main MOSFET $P_{Q,on}$

The conduction losses caused by the main MOSFET can be expressed as follows:

$$P_{Q,on} = \frac{1}{2D}\left(\frac{P_{in}}{V_{ac,rms}}\right)^2 R_{dson}$$

with:

$$D = \frac{1}{1+\frac{\sqrt{2}\,n\,V_{ac,rms}}{V_{out}}}$$

where:

R_{dson}: on-state resistance of the MOSFET according to the data sheet

D: duty ratio at which the converter operates

n: turns ratio of the transformer

V_{out}: output voltage of the converter

It can be shown that the optimal turns ratio *n* for an universal input design is such, that the resulting duty cycle *D* becomes approximately:

$$D = 0.17 \quad \text{for} \quad V_{in,rms} = 230\, V_{ac}$$

$$D = 0.3 \quad \text{for} \quad V_{in,rms} = 110\, V_{ac}$$

Here, the relevant parameter is the on-state resistance R_{dson}, as the other quantities are given by the application and cannot be affected. The MOSFET technology has experienced tremendous advances in the past decade. The values have improved significantly, which undoubtedly had a positive impact on current EPS designs already.

3.2.2.3 Turn-on Losses at the MOSFET $P_{Q,sw}$

One of the disadvantages of the flyback converter is the higher switch stress over a comparable design with other topologies such as the forward converter. The blocking voltage together with the parasitic output capacitance of the MOSFET is mainly responsible for the turn-on losses, which can be approximatively calculated by

$$P_{Q,sw} = \left(\frac{V_{ac,rms}}{1-D}\right)^2 C_{O(er)}\, f_S$$

where:

$C_{o(er)}$: the energy related output capacitance of the MOSFET according to the data sheet

f_S: switching frequency

This formula applies to the brute-force hard switched case only. The implementation of an active clamp (Figure 9), allows realizing soft switching, which significantly reduces the turn-on losses.

3.2.2.4 Gate Drive Losses P_{Qg}

The gate drive losses can be estimated by:

$$P_{Qg} = Q_G V_G\, f_S$$

where:

Q_G: total gate charge of the MOSFET according to the data sheet

V_G: gate drive voltage

Here, the total gate charge is one of the parameters to be optimized. The other one is the gate drive voltage. Both of them affect the gate drive losses proportionally. However, reducing V_G increases the R_{dson} and at the same time increases the conduction losses $P_{Q,on}$ as described in 3.2.2.2. This may offset some or all of the intended benefit.

It is important to note, that there is a tradeoff between the selection of R_{dson}, $C_{o(er)}$ and Q_G. Choosing a MOSFET with lower R_{dson} always increases the other two values. The lowest losses do not coincide with the lowest available R_{dson}. This particularly applies to low power designs. The conduction losses $P_{Q,on}$, the turn-on losses $P_{Q,sw}$ and the gate drive losses P_{Qg} must always be considered together, when selecting a MOSFET.

The introduction of new materials, such as gallium nitride GaN, will provide a strong efficiency benefit with respect to switching and also gate drive losses, as the above mentioned parameter values are significantly smaller. Today, the number of available GaN devices is still limited. Also the costs are still clearly higher in contrast to comparable silicon devices. However, the GaN technology is a strongly growing market. GaN-on-silicon transistors are expected to reach price parity with silicon MOSFETs as early as by 2020 [17].

3.2.2.5 Clamp Losses P_{Cl}

The clamp losses can be approximated by:

$$P_{cl} = \frac{1}{2}\, I_{Qmax}^{2}\, \frac{L_{\sigma}\, f_{S}}{1-\frac{V_{out}}{n\, V_{cl}}}$$

with:

$$I_{Qmax} = \frac{P_{in}}{\sqrt{2}\, D\, V_{ac,rms}} + \frac{D\, V_{ac,rms}}{\sqrt{2}\, L_{P}\, f_{S}}$$

where:

L_P: inductance measured on the primary side of the transformer

L_σ: primary side leakage inductance

f_S: switching frequency

V_{cl}: clamp voltage, zener-voltage on D_6 in Figure 8

Increasing the clamp voltage reduces these losses. However, it must be kept smaller than the maximal allowable drain to source voltage V_{DS} minus the peak of the highest possible line voltage, i.e.:

$$V_{cl} \leq V_{DS,max} - \sqrt{2}\, V_{ac,rms,max}$$

These expressions describe the clamp losses in a passive circuit. With an active clamp an estimated 75 to 80 % of these power losses are recovered and can be further processed.

3.2.2.6 Conduction Losses in the Secondary Rectifier P_{rec}

Low cost versions implement simple diode rectification on the output side. In that case the conduction losses can be calculated relatively simple with:

$$P_{rec} = P_{out} \frac{V_{Dsec}}{Vout}$$

where:

V_{Dsec}: forward voltage drop of the secondary diode

P_{out}: output power

V_{out}: output voltage

Due to the low output voltage of the EPS considered here, schottky diodes can be employed, which do not suffer from reverse recovery losses. They are negligible and do not need to be accounted for. However, at low output voltage, e.g. 5 V, diodes exhibit a forward voltage of approximately 0.4 V. This means, this single component alone accounts for 8% of the power losses.

More advanced designs replace the diode with a synchronous rectifier to reduce these losses. The expression for the conduction losses becomes:

$$P_{rec} = \frac{1}{1-D} \left(\frac{P_{out}}{V_{out}}\right)^{2} R_{ds,rec}$$

where:

$R_{ds,rec}$: on-resistance of the synchronous rectifier

Here are the conduction losses dominating over the turn-on losses. At the secondary side the voltage is considerably lower, which reduces the turn-on losses significantly. Thus, they are not considered here.

3.2.2.7 Gate Drive Losses of Synchronous Switch *PQg,rec*

Similarly as above, the gate drive losses can be estimated with:

$$P_{Qg,rec} = Q_G V_G f_S$$

With the appropriate value for Q_G.

3.2.2.8 Winding Losses in the Transformer Windings, Including Proximity Effect $P_{Cu,ac}$

In order to determine the expected winding losses, the dimension of the magnetic component must be known. The size depends on the electric and magnetic properties. The following set of equations assist an appropriate core selection.

$$L_P = \left(2\frac{B_{max}}{\Delta B} \cdot \frac{V_{ac,max}\, D_{min}}{V_{ac,min}\, D_{max}} - 1\right)\frac{V_{ac,min}^2\, D_{max}^2}{f_S\, P_{in}}$$

$$I_{Pmax} = \frac{P_{in}}{\sqrt{2}\, D_{max}\, V_{ac,min}} + \frac{D_{max}\, V_{ac,min}}{\sqrt{2}\, L_P\, f_S}$$

$$A_{Fe}\, A_W \geq \frac{2}{0.5+D} \cdot \frac{L_P\, I_{Pmax}^2}{K_f B_{max}\, J_{max}}$$

where:

I_{Pmax}: peak value of the primary current

L_P: inductance measured on the primary winding

B_{max}: maximum permissible flux density to avoid saturation of the core material

ΔB: maximum flux swing (limited by the core losses discussed in the next section)

K_f: fill factor of the winding (typical value: 0.4 - 0.5)

J_{max}: current density in the windings (typical value for efficient designs: 4 A/mm^2)

A_{Fe}: magnetic cross section

A_W: available winding area on the bobbin

With the above equations the area product $A_{Fe} \cdot A_W$ of the required core/bobbin combination can be determined. Once a core size is selected, also the mean length per turn ℓ_W is known. This can now be used to compute the conduction losses in the transformer windings using the following formulas:

$$A_{W,P} = \frac{0.5-D}{2} A_W$$

$$R_{Cu,P} = \frac{L_P^2\, I_{Pmax}^2\, l_W\, \rho}{B_{max}^2\, A_{Fe}^2\, A_{W,P} K_f}$$

$$P_{Cu,P,ac} = \frac{1}{D}\left(\frac{P_{in}}{V_{ac,rms}}\right)^2 R_{Cu,P}$$

where:

$A_{W,P}$: winding window allocated for the primary winding

$R_{Cu,P}$: DC resistance of the primary winding

$P_{Cu,P,ac}$: conduction losses of primary winding

The above procedure allocates the winding areas between primary and secondary such that the resulting losses are identical in both windings. Under this condition, the combined losses are minimized.

Additionally, the determined resistive losses are multiplied by a factor of 2 to include AC losses due to the proximity effect. This factor of 2 is based on commonly applied design recommendations concerning the proximity effect.

Similarly on the secondary side:

$$A_{W,S} = A_W - A_{W,P}$$

$$R_{Cu,S} = \frac{L_P^2\, I_{Pmax}^2\, l_W\, \rho\, n^2}{B_{max}^2\, A_{Fe}^2\, A_{W,S} K_f}$$

$$P_{Cu,S,ac} = \frac{1}{1-D}\left(\frac{P_{out}}{V_{out}}\right)^2 R_{Cu,S}$$

where:

$A_{W,S}$: winding window allocated for the secondary winding

n: turns ratio of the transformer

3.2.2.9 Core Losses in the Transformer P_{Fe}

Besides conduction losses in the windings, the transformer also generates core losses. They can be approximatively determined with the Steinmetz formula:

$$P_{Fe} = V_{Fe}\, C_O\, f_S^x\, \hat{B}^y$$

where:

V_{Fe}: effective volume of the core selected in the previous section in cm^3

$\hat{B}$: peak value of the AC flux (half of flux swing $\frac{\Delta B}{2}$)

The following three coefficients depend on the core material. The ferrite material designated 3C95 from Ferroxcube is used as reference. This is one of today’s typically employed materials for this type of application. The Steinmetz coefficients are:

C_O: $239.5 \cdot 10^{-6}$

x: 1.824

y: 2.875

To optimize the losses in the flyback transformer core and windings must be considered together. The performance can be substantially influenced by the construction. The dependencies are well-known and described in literature. We can assume that manufacturers apply these rules to a large degree already, such that there is little potential for improvement.

Unlike in the case of semiconductors, advances in the properties of the involved materials will not allow a significant reduction of the losses in the near future. Copper resistance will continue to remain the same and the properties of ferrite materials have improved only incrementally over the last two decades.

The only real degree of freedom designers have at their disposal is the operating frequency. Increasing it reduces $\hat{B}$ as the product $f_S \cdot \hat{B}$ remains constant. As a result, increasing the frequency reduces the core losses, since in the Steinmetz coefficients above, *x* is smaller than *y*. However, raising the frequency jeopardizes other loss contributions, such as the winding losses due to the proximitiy effect, turn-on losses, gate drive losses and clamp losses. Thus, high frequency operation is only an option with more advanced versions of the flyback converter, such as in Figure 9, where the contribution of some of the frequency dependent losses is reduced by topological measures.

3.2.2.10 Power Consumption of Controller P_{cont}

The power consumption of the controller can be estimated based on specifications in the data sheets of available control ICs. Low power versions which allow secondary side control require as little as 50 mW. Primary side controllers consume even less power, however, the quality of the output regulation is insufficient for most EPS applications.

3.2.3 Design Example

Based on the above discussion two versions of a universal input EPS were designed. Considered are a design at 5 W and the second at 50 W rated power, both with an output voltage of 5 V.

Table 3: Key data of considered designs

	Design 1	Design 2
Power	5 W	50 W
Output voltage	5 V	5 V
Input range	Universal	Universal
Main switch	IDP80R1K4P7	IPD80R280P7
Synchronous Switch	IDP220N06L3	IPI020N06N
Core size	EE19/8/9	RM12/I
Core material	3C95	3C95
Switching frequency	135 kHz	100 kHz

The following table contains the calculated losses of all considered sources according to the above description. The outlined calculation in the previous section focuses on a selection of possible effects and does not account for every single loss source. In our experience, the effectively occurring total losses in a design are 1.5 to 2 times larger than the calculation would suggest. This empirical factor is included in the results at the bottom of Table 4 and Table 5. The optimistic scenario adds 50 %; the realistic one adds 100 % to the calculated values.

Table 4: Itemized losses in the 5 W EPS at rated power

		Power Loss [mW]			
		Conventional Technology[6]		**State of the Art Technology[7]**	
		230 Vac	**110 Vac**	**230 Vac**	**110 Vac**
Input rectifier		41	85	41	85
Main switch	conduction	4	10	4	10
	switching	83	27	21	7
	gate drive	16	16	16	16
Transformer	primary	6	16	6	16
	secondary	15	17	15	17
	core	28	17	28	17
Clamp	passive	263	334		
	active			66	84
Output rectifier	passive	400	400		
	synchronous			30	36
	gate drive			26	26
Controller		50	50	50	50
Total Estimated Power Loss and Efficiency at Rated Power					
Optimistic estimate	total loss	1.38 W	1.47 W	466 mW	545 mW
	efficiency	78.5 %	77.4 %	91.5 %	90.2 %
	four point average efficiency			88.5 %	88.0 %
Realistic estimate	total loss	1.83 W	1.94 W	621 mW	727 mW
	efficiency	73.2 %	72 %	89.0 %	87.3 %
	four point average efficiency			85.3 %	84.6 %

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[6] Conventional Technology: Typical EPS realization according to Figure 8.

[7] State of the Art Technology: With current State of the Art possible solution according to Figure 9.

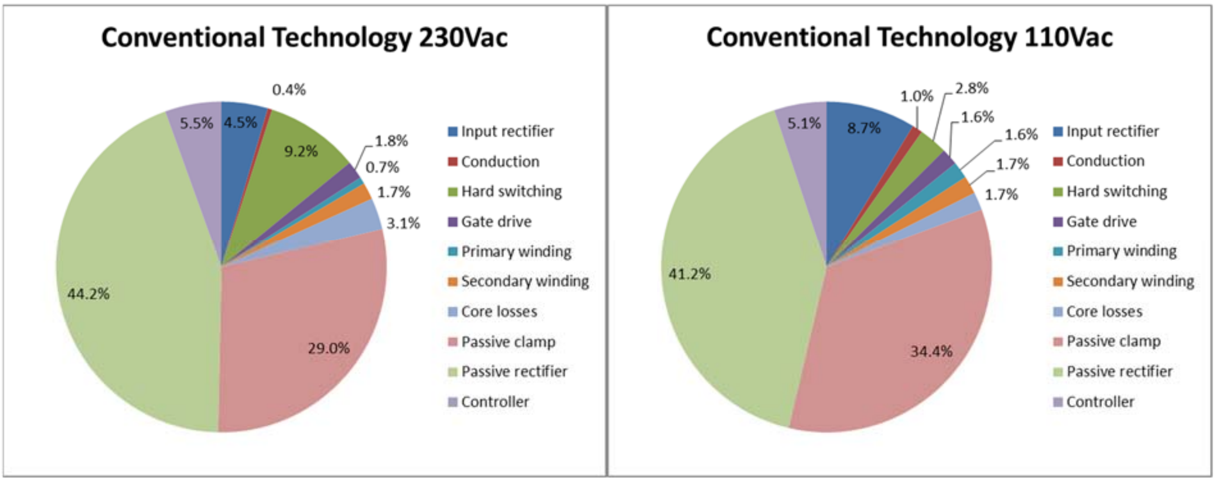

Figure 10: Loss breakdown in percent of conventional technology at high and low line voltage.

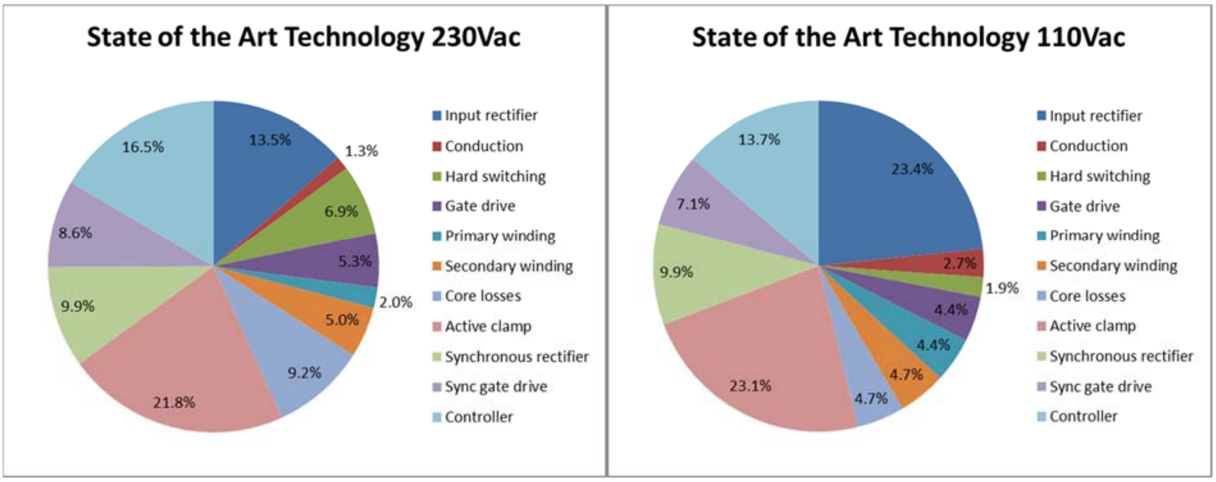

Figure 11: Loss breakdown in percent of the state of the art technology at low and high line voltage.

Table 5: Itemized losses in the 50 W EPS at rated power

		Power Loss [mW]			
		Conventional Technology		**State of the Art Technology**	
		230 Vac	**110 Vac**	**230 Vac**	**110 Vac**
Input rectifier		406	849	406	849
Main switch	conduction	80	198	80	198
	switching	292	94	73	24
	gate drive	44	44	44	44
Transformer	primary	34	83	34	83
	secondary	76	90	76	90
	core	161	99	161	99
Clamp	passive	2222	2744		
	active			555	686
Output rectifier	passive	4000	4000		
	synchronous			259	307
	gate drive			127	127
Controller		50	50	50	50
Total Estimated Power Loss					
Optimistic estimate	total loss	11.1 W	12.4 W	2.86 W	3.83 W
	efficiency	81.8 %	80.2 %	94.6 %	92.9 %
	four point average efficiency			93.8 %	92.6 %
Realistic estimate	total loss	14.8 W	16.5 W	3.81 W	5.11 W
	efficiency	77.2 %	75.2 %	92.9 %	90.7 %
	four point average efficiency			91.9 %	90.3 %

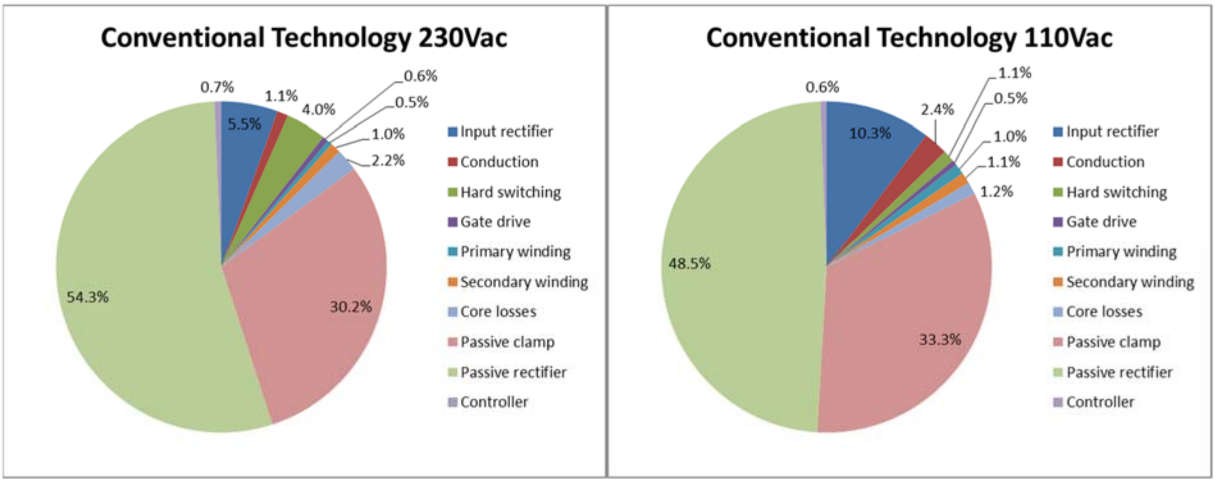

Figure 12: Loss breakdown in percent of conventional technology at high and low line voltage.

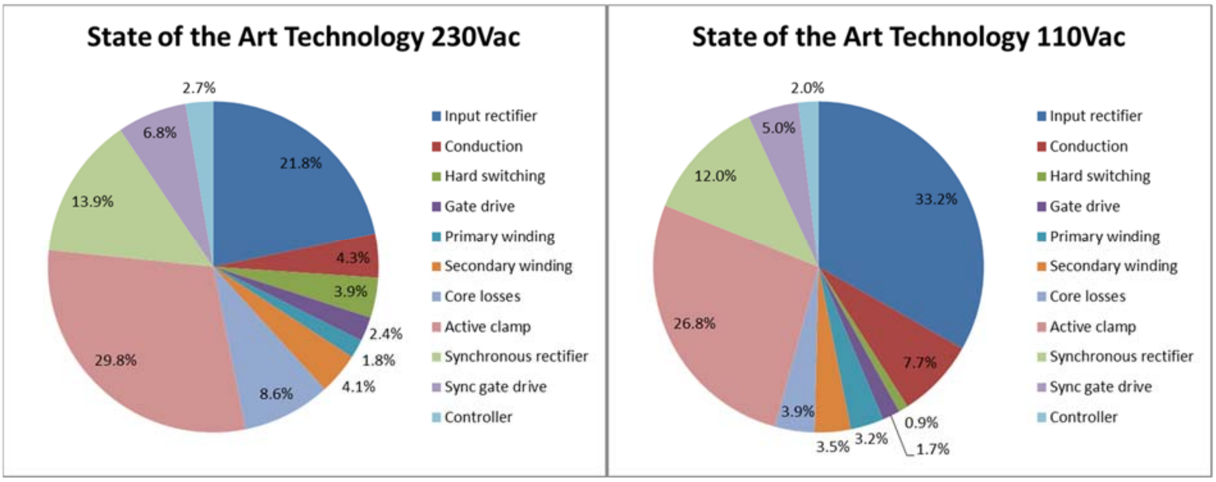

Figure 13: Loss breakdown in percent with state of the art technology at high and low line voltage.

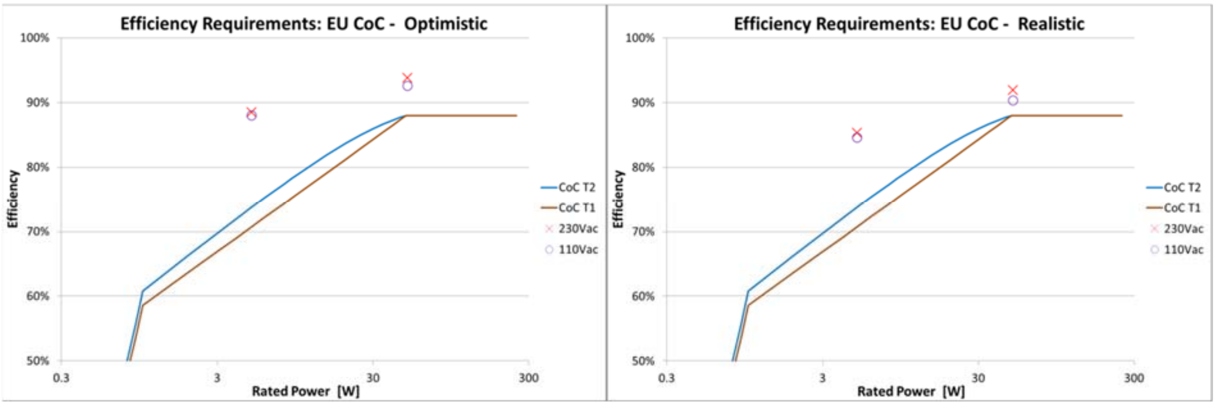

Figure 14: The estimated four point efficiencies versus the EU CoC limits.

The analytical analysis suggests that especially for the very low power cases (5 to 10 W), the limits could be raised somewhat, imposing neither unreasonable technical challenges nor unacceptably high costs. However, this investigation is considering a limited amount of cases on a purely analytical level. The results must be confirmed on real hardware samples to make a case for more stringent limits. The resulting performance always depends on a number of design choices. The size of the chosen transformer in the 5 W design is relatively large. This improves the efficiency, but results in a rather large device. In a more compact design, the results would be somewhat less promising.

The analysis was limited to converters based on the flyback Topology employing silicon based MOSFETs. The reasons are as follows:

The flyback can easily handle single stage solutions with wide input voltage range. To cover this range with other topologies causes clearly more difficulties. This in turn compromises the efficiency benefit the topology might possess in other applications. For example, a converter operating from a fixed voltage can be designed more efficiently using a forward.

Employing new materials such as silicon carbide (SiC) or gallium nitride (GaN) will not significantly improve the efficiency. SiC components are hardly available for this very low power range. Their advantage is most dominant at much higher power levels and also at higher voltages. The primary application for SiC is a replacement of IGBTs.

The main advantage of GaN components lies in the reduction of switching and gate drive losses. In the investigated case, these are clearly not the major source of losses and the cost increase might not be justified for a marginal improvement.

3.3 Higher Power EPS

3.3.1 Overview

The topological variety in the power range at 75 W and above is clearly broader. The main reason is that regulations require an active power factor correction, enforced by EN61000-3-2. This standard is also published as IEC regulation and is effective in most regions worldwide. The majority of designs employ a two-stage approach. The first stage is responsible for the input current quality and provides a pre-regulated intermediate circuit voltage, whereas the second stage operates from this intermediate circuit and provides the fully regulated output voltage. This premise allows much more flexibility in the choice of suitable solutions. Existing power supplies make use of this situation and come in a greater topological variety than the low power counterparts.

3.3.2 Present-Day Implementations

Nonetheless, a frequently implemented combination is shown in Figure 15. The PFC stage is realized by a boost converter and the galvanic isolation and output regulation is implemented with an LLC-resonant converter. Even for this circuit topology, there exist a number of different modes of operation, especially for the PFC stage at the input. It can be operated

- in continuous conduction mode CCM,
- in boundary mode BM,
- in discontinuous conduction mode DCM.

Each of these modes has its advantages and disadvantages. In the power range up to 250 W, the boundary mode typically performs the best in terms of efficiency. This includes the range covered by the efficiency standards under consideration.

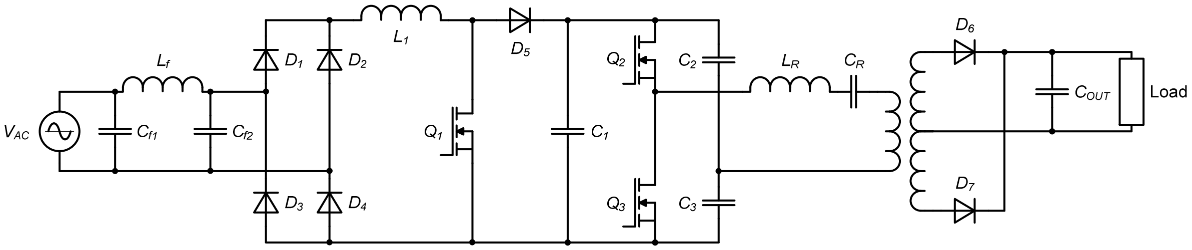

Figure 15: Typical off-line power supply topology with PFC.

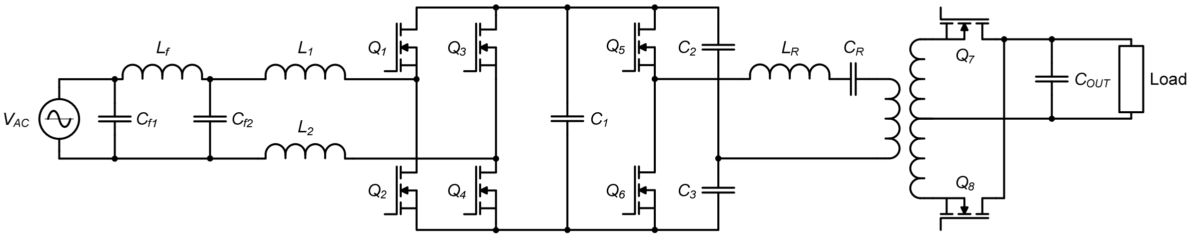

Figure 16: Improved performance with totem pole PFC and synchronous rectification.

Irrespective of the mode of operation, all versions have in common that the power is rectified by a passive full bridge (diodes D_1 through D_4 in circuit of Figure 15). The previous section (Chapter 3.2.3) has demonstrated that this rectifier contributes significantly to the total power losses. This conclusion also applies to the higher power range. Particularly at low input voltage, this often becomes the most severe single source of losses in the entire circuit.

To alleviate high rectifier losses, several bridgeless topologies have been suggested [15,16]. A popular example is the totem pole boost PFC shown in Figure 16. The circuit eliminates the diode bridge and incorporates the function of rectification into the switched mode power stage. Over the course of time, also here, several modes of operation were introduced. In terms of efficiency, the so-called triangular current mode (TCM) yields the best performance. TCM is an optimized control strategy to eliminate switching losses. Optimized in the sense that at all points of operation only the minimum necessary circulating power for soft switching is generated [18,19]. Unlike in other soft switching schemes, where excessive circulating power causes conduction losses, that can offset some of the intended savings in switching losses.

The drawback is the complexity of the control method. No commercially available ICs exist for the control and supervision circuitry. In contrast, for all operating modes of standard implementation in Figure 15 a vast number of control ICs are readily available on the market.

The controller of a totem pole PFC in TCM requires an extremely fast and accurate current measurement to detect the zero crossing of the inductor current. The complexity of the control law for TCM imperatively requires a relatively powerful microprocessor. In addition to the impact on the costs, its power consumption potentially jeopardizes partial load efficiency to some degree. Today, in some existing EPS a totem pole boost converter may be employed as a bridgeless PFC stage, however, very likely without implementation of triangular current mode and thus, not taking advantage of its full potential.

In both examples, the galvanically isolated DC/DC stage is implemented with an LLC-resonant converter. Over the past eight to ten years, this has mutated to the topology of choice for applications with relatively constant input and output voltages. At the power level discussed here, the half bridge version is a good compromise between cost and performance. Even though, there might be more efficient topologies in terms of low load efficiency, the overall performance speaks for the LLC-resonant converter.

Synchronous rectification, as shown in Figure 16, is also a worthwhile investment in this case. The lower the output voltage, the higher is the benefit in terms of efficiency.

3.3.3 Design Example

The following table compares the estimated losses of a conventional boost PFC converter in boundary mode with a totem pole in TCM at 110 W and an output voltage in the range of 20 V. The values are generated partially through circuit simulations. Therefore, no formulas are stated here as opposed to the low power case in Section 3.2.

It is evident, that the input rectifier contributes a major portion to the overall losses in the boost realization, particularly at low line. With the totem pole in TCM an improvement of 1.5 to 2 % in efficiency appears possible, as shown in Table 6.

Here, the controller losses are assumed considerably higher than in the low power case, irrespective of the converter topology. The main reason for this is the more complicated control circuit. This includes several required measurements at the line voltage level. A more detailed discussion on this topic is presented in Chapter 3.431.

Table 6: Itemized Losses of PFC stage with state of the art boost converter and TCM totem pole converter

		Power Loss [mW]			
		Boost in boundary mode		**Totem Pole in TCM**	
		230 Vac	**110 Vac**	**230 Vac**	**110 Vac**
Input rectifier	conduction	1247	2443		
MOSFET	conduction	74	294	593	1235
	switching	1367	1314	571	522
	gate drive	339	127	294	190
Diode	conduction	362	362	5	5
Inductor	core	69	148	397	567
	winding	166	511	106	221
Controller		360	360	360	360
Total Estimated Power Loss of PFC Stage					
Realistic estimate	total loss	3.98 W	5.56 W	2.33 W	3.10 W
	efficiency	96.5 %	95.1 %	97.9 %	97.3 %

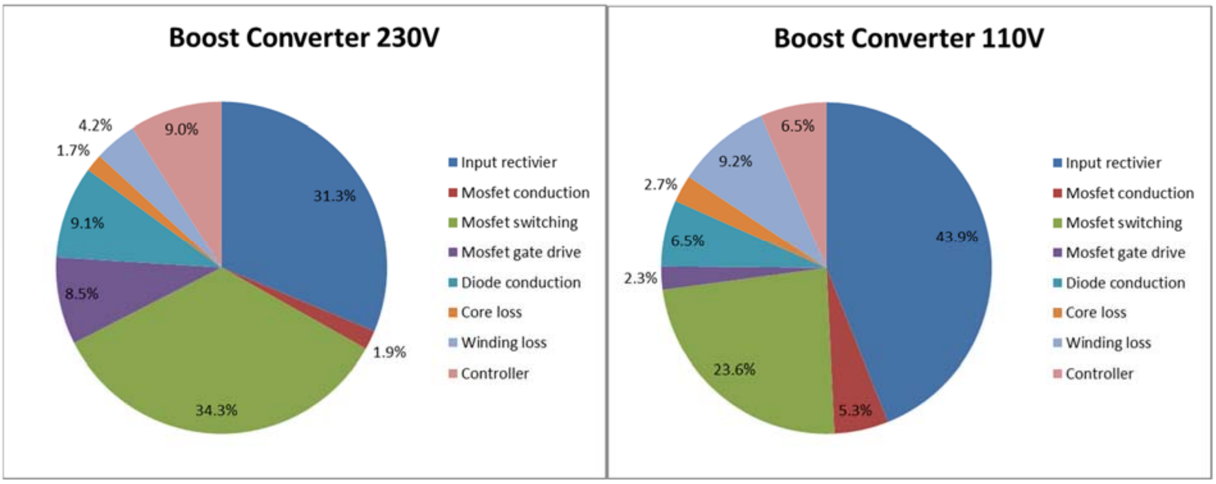

Figure 17: Loss breakdown in percent of boost converter in boundary mode at high and low line voltage.

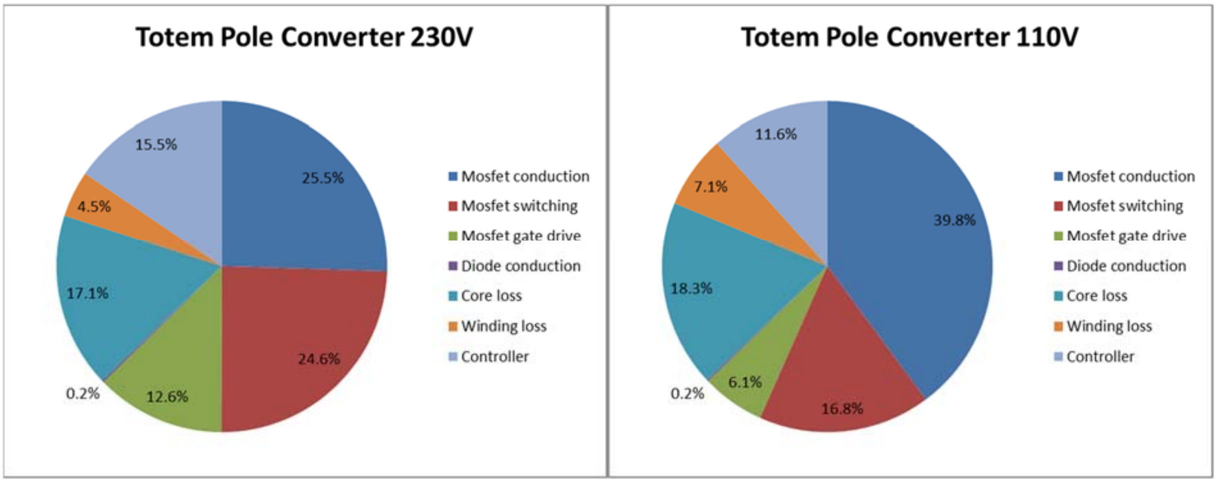

Figure 18: Loss breakdown in percent of totem pole converter in TCM at high and low line voltage.

These extra losses also affect the standby behavior. The measurements shown in Figure 29 confirm this. Not all tested devices in the upper power range meet the specs with respect to standby losses. At low power the situation looks much better.

The complete converter also includes a galvanically isolated DC/DC stage. State of the art technology for good performance at reasonable costs at the power level considered here is the half bridge version of the LLC-resonant converter. As a reference for the achievable efficiency we used one of our own designs with the following specifications:

- Output power 160 W
- Output voltage 27 V
- Input voltage 400 V

This is not exactly identical with the power considered in the input stage with 110 W. However, the values can be adjusted for the range of interest. This still provides a more accurate basis than a completely analytical consideration, as in the measurements all parasitic effects are included. Especially in an LLC-converter the analytically determined values tend to differ more from measurements than with the previously considered PWM converters. The measured four-point efficiency values are:

Table 7: Measured efficiency values on a real LLC resonant converter

Power	40 W	80 W	120 W	160 W	Average
Efficiency	91.8 %	95.2 %	96.3 %	96.7 %	95.0 %

The power level of 160 W versus 110 W is not very critical and does hardly affect the values. For an EPS of the category basic voltage the output can be as low as 6 V. At that level, we estimate the efficiency to be about 1 to 1.5 % lower. Thus, as a worst case the efficiency of the DC/DC converter is expected to be about 93.5 %. This value of course does not depend on the value of the line voltage nor on the type of PFC converter.

Table 8: Overall best efficiency estimate of EPS with PFC

	Efficiency [%]			
	Boost in Boundary Mode		**Totem Pole in TCM**	
	230Vac	**110Vac**	**230Vac**	**110Vac**
PFC: universal input	96.5 %	95.1 %	97.9 %	97.3 %
DC/DC: LLC-resonant half bridge	93.5 %	93.5 %	93.5 %	93.5 %
Overall:	90.2 %	89.9 %	91.5 %	91.0 %

Currently, the most stringent efficiency standard with an 89 % requirement is the EU Code of Conduct, Tier 2. These results suggest that there is no significant room for improvement in terms of efficiency, unless the totem pole converter in triangular current mode or a similar technology can be implemented. The expected improvement is at least 1 to 1.5 %. However, at this point this solution is still predominantly an academic issue. The number of real live implementations is still rather low. Considerable challenges must be faced, when employing this topology properly, considering also safety, reliability, electromagnetic interference and last but not least cost issues.

3.3.4 Potential for Improvements

The totem pole PFC has the potential to improve the efficiency performance of EPS in the higher power range (75 to 250 W), as it replaces the input rectifier and – if operated in triangular current mode – provides soft switching. The availability of dedicated peripheral components (controller and sensors) could greatly simplify the implementation and would make the solution more attractive. As of now, such circuits are not available. This clearly hinders the implementation of this solution.

From a topological point of view, we do not identify any significant room for improvement with respect to the DC/DC stage of the converter. Soft switching comes very natural to this topology. The synchronous rectification however, is crucial for best performance.

Therefore, the topology shown in Figure 16 belongs to the most efficient ones known today. However, particularly the implementation of triangular current mode TCM requires complex circuitry. In addition, the higher complexity potentially reduces the reliability.

An alternative approach to improve efficiency is the implementation of Gallium Nitride (GaN) components as semiconductor devices. GaN devices are expected to be reasonably priced in a few years [17], such that they become an option for designers. Today, GaN devices cover a similar voltage and power range as traditional MOSFETs. Thus, they could serve as a replacement in EPS. The primary benefit of GaN is the much better switching performance.

Even in conjunction with the standard solution of Figure 15 an efficiency gain of about 1 % can be expected, due to a considerable reduction of the switching losses. The advantage of this approach is the availability of control ICs and the proven topological concept. A simple analogue control is sufficient.

The next level of improvement is the totem pole PFC equipped with GaN devices, but operated in classical boundary mode. The advantage of this mode is the much simpler control method. This solution with standard Si MOSFETs generates significant switching losses. With GaN devices this is no longer an issue. Based on the calculation in the previous section an efficiency improvement of 1 to 1.5 % can be expected. This improvement is similar to the case of the complex triangular current mode with traditional MOSFETs.

Combining both, GaN devices and TCM, however, will provide only a marginal additional benefit if any at all. Both measures primarily reduce the switching losses and they can only be removed once.

For similar reasons, using GaN devices in the DC/DC converter will not yield a major benefit. Soft switching can be implemented very easily in the LLC converter, such that switching losses are practically non-existent.

A disadvantage of the LLC converter is the relatively large amount of reactive power in the circuit under partial load condition. This generates some extra conduction losses in the MOSFETs and transformer. Also here, there is a chance to use an “older” hard-swiched topology together with GaN. The switching losses would remain reasonably low and could be more than compensated for by the absence of reactive power, especially at partial load.

The above considerations assume that the output voltage is fixed. In case of a variable output voltage, e.g. as in USB 3.1 Power Delivery the overall efficiency will suffer by at least 1 %. An LLC-resonant converter will most likely no longer be the best choice.

It must be noted here, that these results are based first and foremost on analytical considerations and qualified estimations. In order to substantiate these findings, hardware realizations are unavoidable, as never all parasitic effects are accounted for in analytical models. Only real life circuits can conclusively confirm the performance.

3.3.5 Single Stage Approach

Over the past three decades, since power factor correction became a research topic in the power electronics community, numerous single stage solutions have been proposed [20,21,22]. These circuits provide input current shaping, galvanic isolation and output regulation in a single power processing stage. Some of these solutions provide advantages in terms of size, as the number of components is clearly reduced in contrast to standard solutions. That does not necessarily translate into lower conversion losses. These topologies have failed to prove superiority in terms of efficiency.

3.4 On Mode versus Standby

A significant number of external power supplies are connected to the grid continuously. The discussion concerning efficiency must therefore also include the aspect of standby losses. Rightfully so, all the above mentioned regulations regarding efficiency also impose limits for the maximum allowable standby power. The following two examples shall illustrate the significance of the standby losses. The first example is a smartphone charger as typically delivered together with a new phone. The subsequent calculation is based on the following assumptions, which can be considered typical for a smart phone:

- Rated power of charger 5 W
- Daily charge 10 Wh
- Daily charging time 2 h
- Daily standby time 22 h
- The efficiency and standby power levels are based on limits imposed by the listed standards

Table 9: Standby loss contribution to the energy efficiency of low power devices.

Standard	Efficiency [%]	Standby Power [mW]	Input Energy [Wh]	Conversion Loss [Wh]	Standby Loss [Wh]	Energy Efficiency [%]
EC/278-2009	68.2	300	14.7	4.7	6.6	47
DOE Level VI	73.6	100	13.6	3.6	2.2	63
CoC Tier 1	70.8	150	14.1	4.1	3.3	57
CoC Tier 2	73.8	75	13.6	3.6	1.7	66

With the current mandatory standard in Europe ((EC)278-2009), the standby losses are clearly more significant than the conversion losses, resulting in an overall energy efficiency of less than 50 %. In the U.S. the currently applicable limits are tighter, especially concerning standby. The resulting energy efficiency rises to 63 %. Even better is the situation with the European CoC, Tier 2. Adhering to this standard, which is still voluntary, raises the energy efficiency to 66 % percent. However, with one third of the energy lost, this is still an extremely poor yield. Considering the sheer number of such devices in circulation demonstrates the importance to focus on the standby losses, especially in the low power range.

The second example is based on an AC-adapter of a notebook and can also be considered a typical situation. The assumption is here again that the external power supply remains on the grid permanently. The conditions assumed for this calculation are:

- Average power of notebook while working 50 W
- Rated power of charger 65 W
- Average daily working hours (including weekends) 8 h
- Time in standby 16 h
- Output energy (delivered to the notebook) 400 Wh
- The efficiency and standby power levels are based on limits imposed by the listed standards

Table 10: Standby loss contribution to the energy efficiency of higher power devices.

Standard	Efficiency [%]	Standby Power [mW]	Input Energy [Wh]	Conversion Loss [Wh]	Standby Loss [Wh]	Energy Efficiency [%]
(EC)278-2009	86.8	500	461	60.8	8.0	85.3
DOE Level VI	88	210	455	54.5	3.4	87.4
CoC Tier 1	89	250	449	49.4	4.0	88.2
CoC Tier 2	89	150	449	49.4	2.4	88.5

In this example the standby losses account for roughly 10 % of the total energy losses under current regulation, which in turn means a drop of one to two efficiency percent. With the voluntary Code of Conduct, Tier 2 the energy efficiency falls only about 0.5 % below the conversion efficiency requirement. This reveals that for the higher power devices combined with less idle time the standby losses are considerably less critical in terms of energy efficiency.

The measurements on existing EPS in Chapter 4 indicate that the standby power increases with the rated power. A majority of the tested EPS in the 5 -10 W range adhere already to the very tight limit of 75 mW defined in CoC, Tier 2. On the other hand, the higher power devices show clearly higher standby losses. Half of them are not passing with regard to CoC, Tier 2. See Figure 29. The number of tested samples is statistically obviously too low to be relevant. However, it seems to confirm the trend a power electronics designer would expect, which is, standby losses are increasing with rated power.

This advocates the conclusion, that the standby limits for the low power range could be lowered from currently 300 mW to 75 mW, as proposes by CoC, Tier 2, without a significant impact on the complexity of EPS designs. Such a measure seems even more justified, considering the result of the above smart phone charger example in Table 9. Even if in a more extensive and thus, more representative test, a larger percentage of the low power EPS would fail to meet the CoC, Tier 2 limits, the measurements in Chapter 4 prove, that it is possible to fulfill the requirement.

In contrast, the no load losses of higher power EPSs are more difficult to reduce, a conclusion also supported by the measurements in Chapter 4. At the same time, these standby losses are clearly less significant compared to the conversion losses, as shown in Table 10. Owing to the higher complexity of the solutions, the standby losses are naturally higher in EPS with higher rated power. One of the reasons are several necessary measurements at the 230 to 400 V level [27]. Figure 19 shows a boundary mode PFC realization including the control circuit, as it is typically implemented in EPS in the 75 to 250 W range. Three signals are derived from higher voltages. These are:

- the rectified line voltage, sensed through RmultH,
- the intermediate circuit voltage of ca. 400 V, sensed through RoutH
- an independent measurement of the same voltage, sensed through RH

In order to achieve an appropriate signal level with a sufficient signal to noise ratio, typically currents of 0.1 to 0.2 mA are necessary. This leads to 100 to 200 mW of standby losses, just due to these measurements. This, of course, is not the only source of standby losses, but serves as an example for the higher value in the more complex PFC circuits. Therefore, our assessment is that in circuits, where power factor correction is required, the proposed CoC, Tier 2 limit of 150 mW is already very challenging.

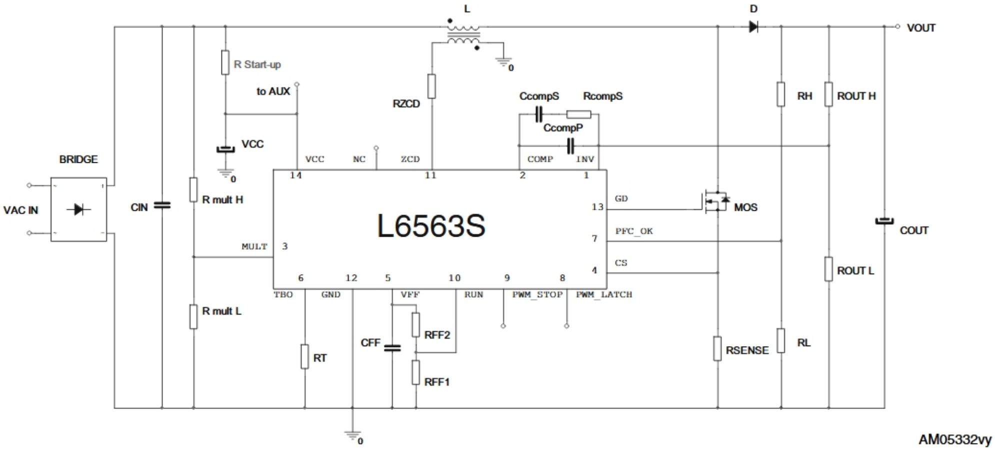

Figure 19: Typical boudary mode PFC circiut including controller.

3.5 Standby versus Idle Mode

Especially higher power EPSs must enter an active sleep mode in order to comply with the standby limits. As mentioned before, higher power includes all EPS above 75 W, as for this power level an active PFC stage is required. This stage causes additional standby losses, when running. In standby condition most of the power electronics circuits (including the PFC) are shut down. The same holds for the controller, it typically enters a sleep mode. Only a small auxiliary supply with an analogue controller continues to run and provides a minimum amount of power. This is needed to detect a potential load connected to the EPS, to wake up the controller and to initiate powering up the main converter.

At this point, the internal losses will increase significantly, even if no power is drawn from the output. The main sources for these losses are the gate drive and switching losses and the controller, which is now fully powered up.

Now this EPS is charging the battery of the device it is intended for. When the battery is fully charged, the load reduces to zero (or virtually zero), even if the cable remains connected between the EPS and the device. However, not all EPS would recognize this as a standby. One of the reasons is, that the EPS senses that it is connected to a load and must therefore be ready to charge. This can lead to considerably higher idling losses than published stand by losses in the data sheet.

Another scenario is that the output power is not exactly zero. The connected device may have its own standby consumption of a few hundred Milliwatts or even Watts. It may power a clock, an off-LED, or it must be ready to receive a remote turn-on signal to name a few reasons.

An example for this scenario is a printer for home use, which, when working, consumes an approximate power of 40 W. For the vast majority of time, it is in a standby awaiting the signal to start a print job. In this state, it consumes an estimated 3 to 5 W. Thus, the EPS must have a rated power of at least 50 W, but is working most of the time at or below 10 % of its power rating. Therefore, it is well justified that also the efficiency at 10 % of rated power is specified. The EU Code of Conduct includes this, not so however, all other considered standards.

The standby measurements in Chapter 4 were carried out with the output completely disconnected from any load. Depending on the implementation of the device this situation can be detected and the device can enter a sleep mode to reduce losses. This may not necessarily be the case with connected loads. Over the course of the measurements, it was observed that an EPS connected to an electronic device in standby may consume a considerably higher amount of power, compared to the disconnected case. In one particular case of a popular brand of a smart phone charger we measured the following behavior:

- The EPS is completely disconnected from the phone:
  measured standby power: 26 mW
- The EPS is connected to the idling phone, which is completely charged:
  Measured continuous power is appr. 100 mW, with a charging burst roughly every 15 minutes.
- The EPS is connected to the fully charged and turned off phone:
  Measured continuous power is appr. 500 mW

Other devices showed clearly higher consumption in standby, as well, if the device to be charged was still connected.

4 Measurements

In order to create a picture, on how todays external power supplies perform, 16 randomly selected devices were tested for efficiency and standby power according to the IEC recognized method defined in standard AS/NZS 4665 Part 1 and Part 2. The measurements were taken after a warm-up time of 45 minutes at rated power. Then, the load was reduced to 75 %, 50 %, 25 % and where applicable also to 10 % of rated power. Before each measurement the EPS was working for 5 minutes at the tested power level. The investigated EPS can be categorized as follows:

Table 11: Classification of the 16 tested EPS

DOE Marking	V	VI	No Marking
Basic Voltage	3	2	0
Low Voltage	4	1	1
Multiple Voltage	0	3	2

For EPS marked with DOE Level V two of the three basic voltage samples do not meet the specified efficiency level, as shown in Figure 20 (left hand side). In contrast, all low voltage devices passed the test. Their power rating is considerably lower, and thus, must comply with significantly lower limits (Figure 20, right hand side). However, all tested devices fulfill the standby requirement associated with level V (Figure 21).

Three out of the six devices marked as level VI fail to meet the specified efficiency values, as shown in Figure 22 and Figure 23. The standby power was measured on five units, where four of them passed the test (Figure 24).

All the single output devices were compared against the mandatory European efficiency requirements. In this assessment, only one unit failed to comply (Figure 25). In terms of standby losses, all tested EPS meet the requirements as seen in Figure 26.

The same measurements compared against EU Code of Conduct, Tier 1 and Tier 2 shows that the averaged efficiency goals are not reached in the majority of cases. This even holds for the more relaxed Tier 1 requirements (Figure 27). Even worse is the result concerning the 10 % efficiency limit. One single device out of the tested eleven samples adheres to the requirement according to Tier 1 and Tier 2 (Figure 28).

In terms of standby losses, the situation appears considerably better. One single unit fails against Tier 1 and three samples do not meet the Tier 2 limit.

In this context it must be noted, that in order to comply with the EU Code of Conduct, Version 5 only 90 % of a manufacturer's EPS must fulfill the specified limits.

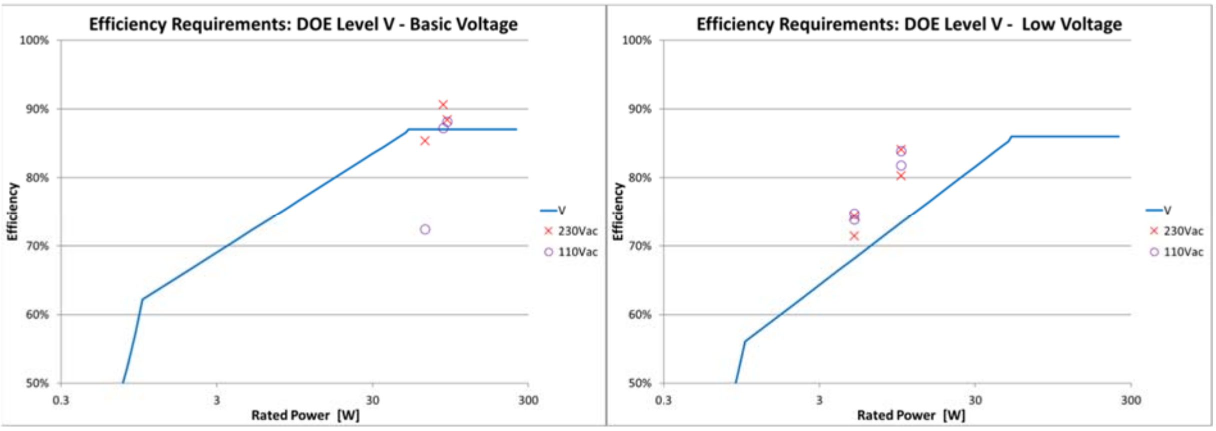

Figure 20: Comparison of measured efficiency with requirements according to DOE level V for basic and low voltage.

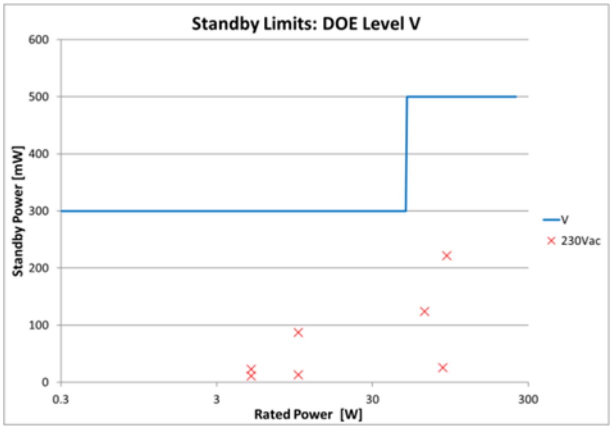

Figure 21: Comparison of measured standby losses with limits according to DOE level V.

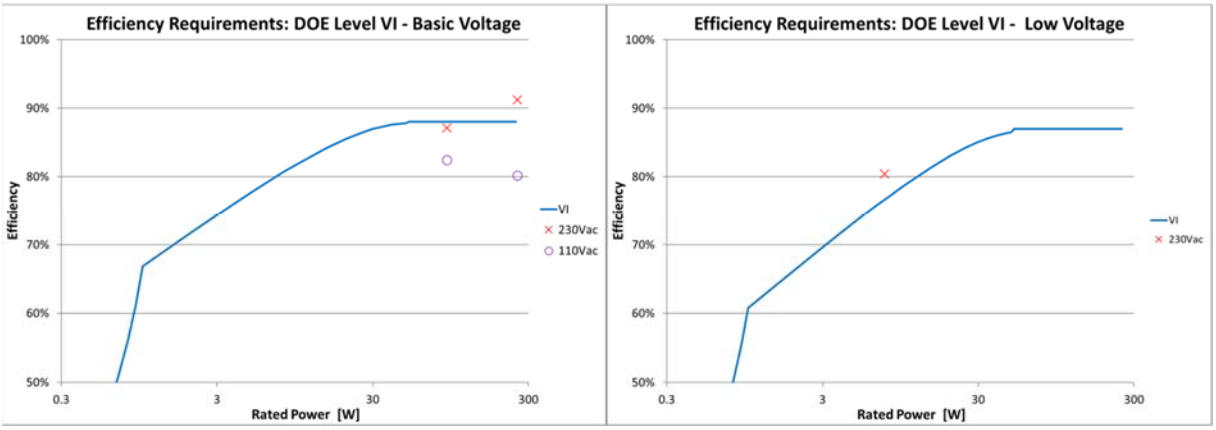

Figure 22: Comparison of measured efficiency with requirements according to DOE level VI for basic and low voltage.

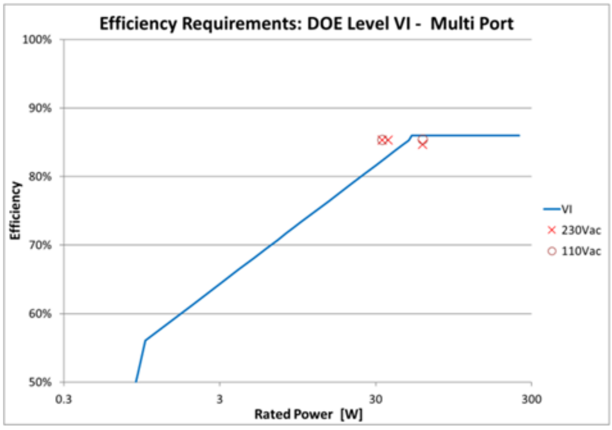

Figure 23: Comparison of measured efficiency on multiport units with requirements according to DOE level VI.

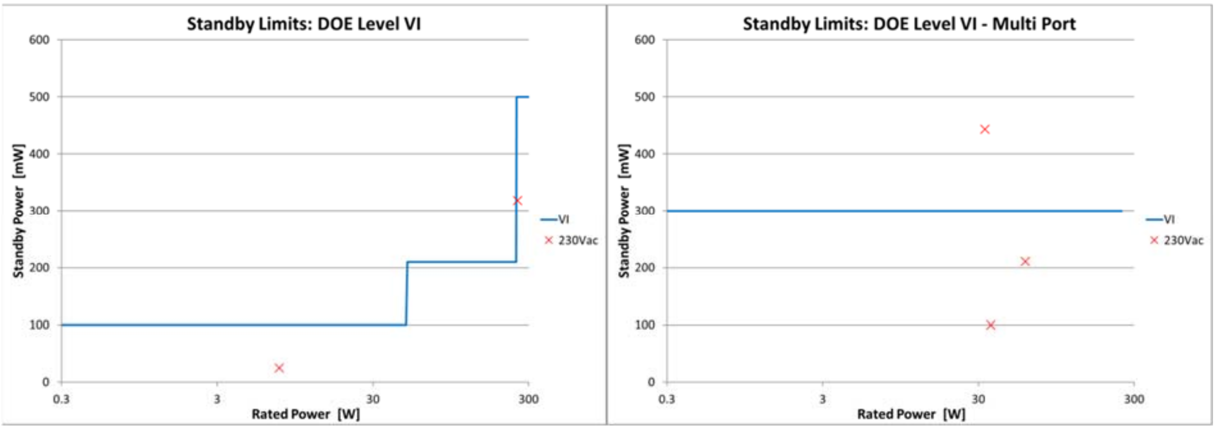

Figure 24: Comparison of measured standby losses with limits according to DOE level VI.

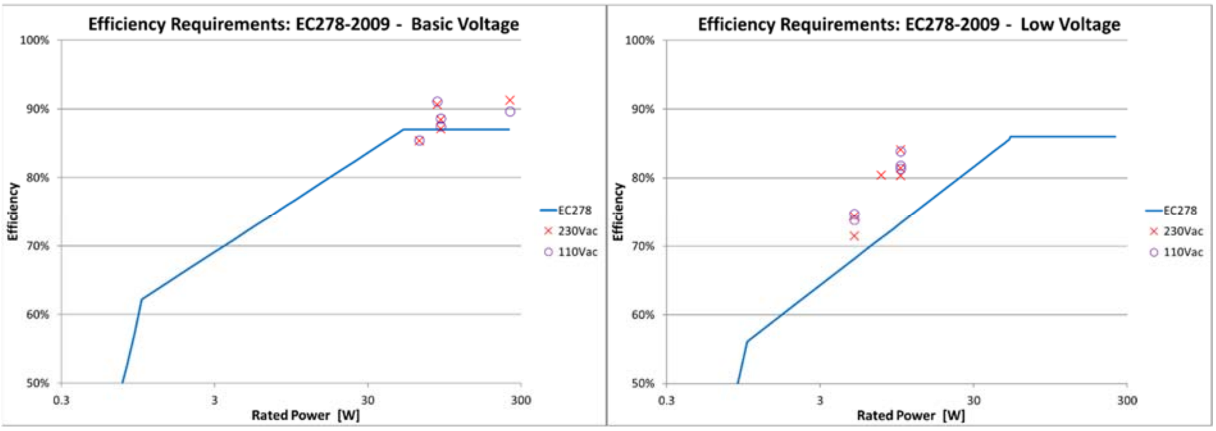

Figure 25: Comparison of measured efficiency with mandatory (EC)278/2009 standard for basic and low voltage.

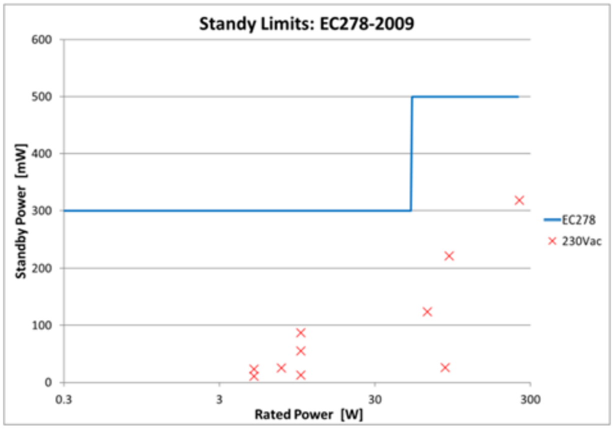

Figure 26: Comparison of measured standby losses with limits according to mandatory (EC)278/2009 standard.

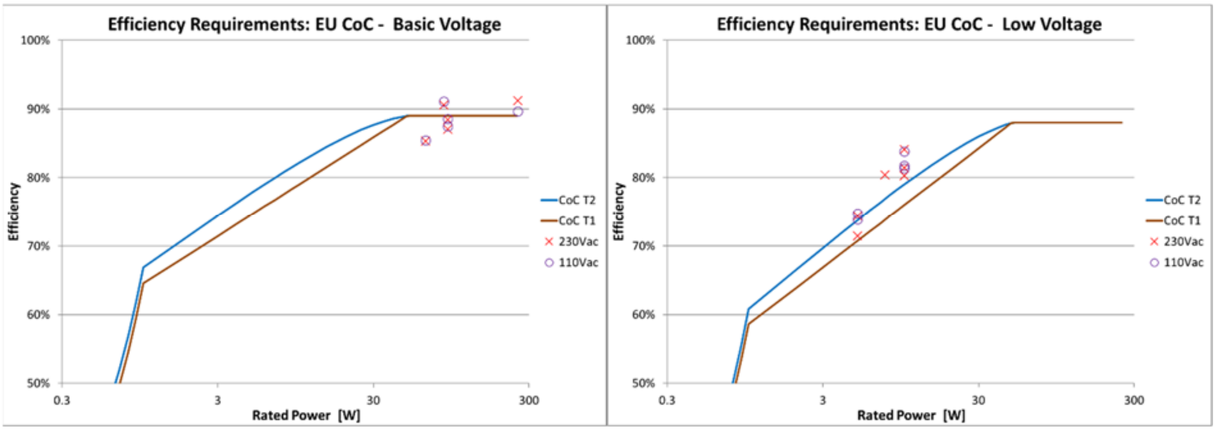

Figure 27: Comparison of measured average efficiency with requirements according to the voluntary Code of Conduct, Tier 1 & 2.

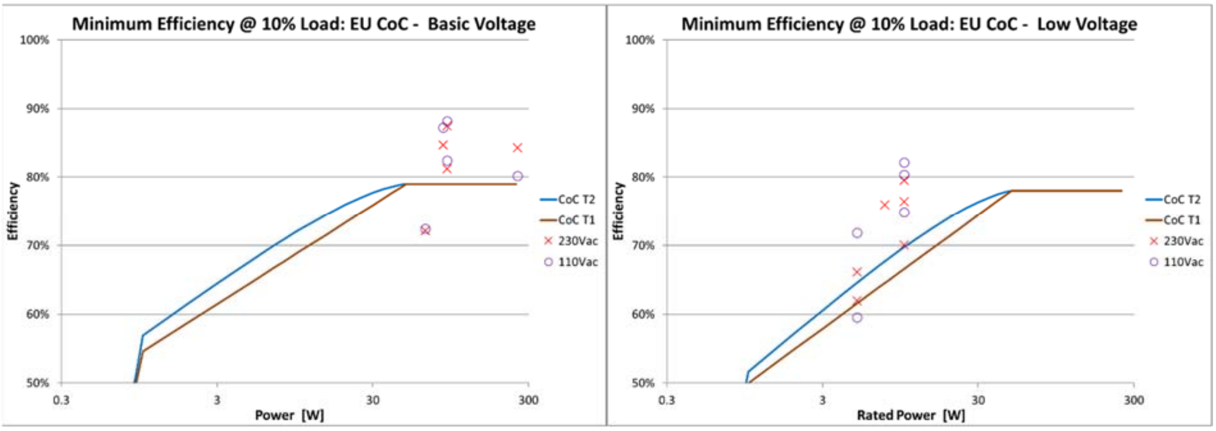

Figure 28: Comparison of measured efficiency at 10 % of rated power with requirements according to the voluntary Code of Conduct, Tier 1 & 2.

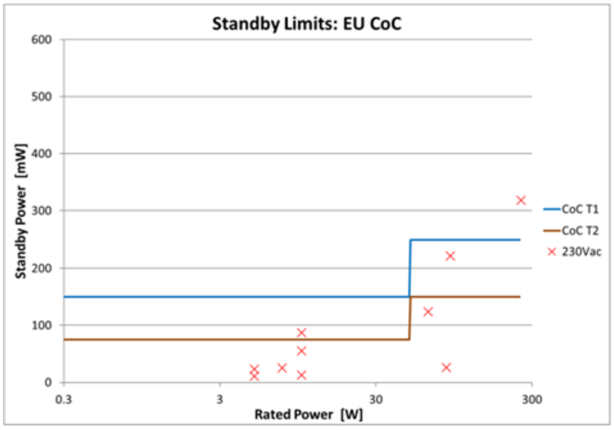

Figure 29: Comparison of measured standby losses with limits according to voluntary Code of Conduct Version 5, Tier 1 & 2.

5 Further Efficiency and Sustainability Standards

Besides the reglatory limits imposed by the gouvernments of various countries, there are a number of voluntary efforts to improve the efficiency of EPS. For completeness sake the most popular of these labels shall be mentioned in this cotext.

5.1 Energy Star

In 2009 Energy Star removed the external power supplies category from its listing, with the justification that it should be considered part of the end product. The last specified limits were equivalent to DOE level IV [23].

5.2 80 Plus

80 Plus is a North American label for internal power supplies for computers, servers and data centers. External power supplies are not covered. Six different efficiency levels are specified, from a relatively relaxed 80 Plus to the very stringent 80 Plus Titanium [24].

5.3 Blue Angel

Blue Angel is the oldest German Ecolabel, awarded to more than 12’000 products. It does not cover external power supplies as a separate category. In the category Computers and Keyboards compliance according to (EC)278/2009 is required to receive the label. The same holds for the category Cell Phones. Other categories were not considered [25].

5.4 Nordic Swan

Nordic Swan is an Ecolabel initiative of the North European countries, including Denmark, Norway, Sweden, Finland and Island. In order to qualify, external power supplies of notebooks and other computer related products must comply with DOE level V. No specifications for other applications were found [26].

5.5 Top Runner

There are Top Runner initiatives in a number of countries worldwide. The common goal is to improve energy efficiency. The implemented concepts are quite different, though. In Japan the program is very successful, as it has evolved to a major pillar in the environmental legislation. Somewhat simplified: periodically the energy consumption and efficiencies of all products within product type are recorded. The top few determine the minimum requirement to which all manufacturers subsequently have to adhere. This competitive concept adjusts itself to the technical feasible limits.

6 Conclusion

6.1 Overview

The focus of this investigation was placed on the efficiency and standby power of external power supplies EPS. The potentials of the currently best available technologies were examined in terms of the reduction of power losses. For different scenarios the possibility of tightening the relevant international standards was evaluated. The results were primarily generated by analytical methods and measurements on existing designs. Some further investigations on hardware realizations are required to substantiate the conclusions. The following sections summarize the findings.

Two different directions were considered concerning advancements in technology. These are:

- Novel circuit topologies
- New wide bandgap semiconductor materials

Both approaches provide an improvement mainly through the reduction of switching losses. This is only one out of a number of loss mechanisms in switched mode power supplies and, according th the analysis, in most cases by far not the dominant one. As a consequence, the possible benefits are quite comparable in either case. As an additional consequence, combining both effects does not result in further substantial power savings, as the switching losses can only be removed once.

External power supplies with a rated power up to 250 W were considered as this is the range covered by most of the applicable standards. For the analytical evaluation this range must be subdivied into:

- Rated power smaller than 75 W, where no limits concerning input current distortion exist.
- Rated power from 75 W to 250 W, where power factor correction is required in most countries.

This distinction is necessary, because the circuit implementation for both cases is very different.

6.2 Novel Topologies

Many drawbacks of current implementations can be improved by newer circuit topologies, comined with more advance control strategies. A number of different appoaches were published in recent years. Genereally, the solutions are considerably more complex and almost always require a microcontroller, as the complexity cannot be handled by less expensive analog controllers.

In low power EPS, particularly in the 5 to 10 W range, the standby losses are more significant in terms of energy consumption. It appears that the standby limits could be tightened, while causing only a reasonable amount of effort for the manufacturers. By mandating the European Code of Conduct, Version 5, Tier 2 limits a significant improvement could be achieved. With 75 mW this constitutes an improvement by a factor four over the currently mandatory limits of 300 mW. The feasibility of even lower limits seems possible, but would incur more costs and also efforts on behalf of the EPS designers.

Similarly, the efficiency requirements in this low power range are quite relaxed. The analyses shows, that an improvement is also possible at reasonable expenses. However, as shown above, the benefit of such a measure is limited. The losses due to standby power are in many situations more dominant.

At power levels of 75 W and above, where existing regulations require a PFC function, the room for improvement is less evident. With current technology the limits approach quite closely the technical possibilities. This holds for the standby power of 150 mW as well as the efficiency requirement of 89 %

at basic voltage and 88 % at low voltage, respectively. Raising the efficiency requirement would most likely require the implementation of new and more complex topologies, such as the introduced totem pole PFC input stage, operated in triangular current mode. Based on above analysis an efficiency gain of approximately 1.5% can be achieved.

However, there are still some open issues. The design effort and the associated costs would increase, mainly because the supporting peripherals are not readily available. In addition, the higher complexity generally reduces the reliability of the devices. The published results concerning the totem pole PFC in TCM were primarily achieved under laboratory conditions. Experience in the field is still missing to a large degree. The robustness of such circuits is not entirely proven and cannot be investigated within the scope of this study. These issues potentially pose a risk.

6.3 Wide Band Gap Devices

Wide band gab materials have the potential to significantly advance power electronics, beyond the current state of the art. This also applies to the power losses. The possible savings, however, depend on the particluar situation. Today two distinct types of such devices are commercially available:

- Silicon carbide, SiC
- Gallium nitride, GaN

Both are assessed for the implementation in EPS.

6.3.1 Silicon Carbide

MOSFETs and diodes are available based on this material. SiC diodes provide an advantage over silicon based diodes at voltage leves above 400 V. They have been widely used for over a decade. Today, they can be considered a standard component. Where appropriate, currently reached efficiency levels already assume SiC diodes.

The first SiC MOSFETs were introduced at the beginning of the current decade, i.e. about 10 years after the diodes. The main advantage of SiC MOSFETs is the much higher voltage rating, and to a lower degree, also current rating. Traditional silicon MOSFETs show their best performance at voltage ratings up to 600 to 800 V. With SiC components this level is at least twice as high, and is expected to increase far beond this. Therefore, the available components are geared towards high power applications, i.e., at least 1 kW and above. The main application of SiC MOSFETs is in three phase systems, where voltage and power is much higer than in the EPS considered in this investigation. Primarily, they are replacing IGBTs in current designs. Thus, their benefit in the context of EPS is expected to be very marginal, if there is any at all.

6.3.2 Gallium Nitride

GaN based devices are even younger than SiC MOSFETs. The first commercially available devices with a voltage rating of 600 V became available in 2015, i.e. three years ago. This voltage level is necessary for the implementation in EPS. Based on their characteristic parameters, they can serve as a direct replacement of Si MOSFETs on low power applications. The main improvement over Si devices is the much smaller parasitic capacitances and as a direct result, the considerably shorter turn on and turn off time. This reduces primarily the switching losses. The same effect as achieved with the above-discussed novel topologies. Therefore, to the first order the possible power saving is very comparable. The estimated potential for raising the efficiency by 1.5 % applies also to EPS employing GaN components.

They can be implemented in simpler, more frequently used, and therefore already proven circuit topologies. This applies particularly to the totem pole PFC, which with GaN can be operated efficiently in a boundary mode or even simple hard switched mode. For applications considered here, the main advantage of GaN devices may be the fact, that they have the potential to replace the more complex topologies with simpler ones, while maintaining their high efficiency.

However, there are minor differences between the two solutions. In case of the DC/DC stage in Figure 15 or Figure 16 GaN components may allow using hard switched PWM topologies in place of the resonant LLC converter. The resulting advantage is the absence of circulating power which present in the LLC implementation. With Si components this current is essential as it provides soft switching. At very light load, its contribution to the conduction losses is quite substantial. Therefore, GaN devices in a hard switched circuit will likely perform somewhat better at light load, at the cost of some efficiency loss at rated power.

One other point should be considered, as well. GaN devices are very new. Longtime reliability data is still missing as only very few GaN based power supplies are already on the marked. In addition, a proper design for reliable operation of the converter is much more difficult to achieve. The authors have gained experience with GaN since they are available. Based on this experience, a very careful printed circuit board layout is substantially more crucial than with Si MOSFETs. For those reasons, there is a certain degree of reluctance by some manufacturers to implement GaN into their new products.

6.4 Summary

The expected introduction of CoC, Tier 2 as mandatory limits will represent a substantial tightening over the currently applicable regulation, especially concerning the standby losses. Some areas have been identified, particularly in the very low power range, where these limits could even be more stringent, without causing major efforts. Irrespective of the technology, increasing the efficiency requirement about 1 to 2 % beyond CoC, Tier 2 appears possible, but requires clearly more efforts, and may jeopardize the reliability of the designs. With respect to the standby losses, lowering the limits would even be more difficult to accomplish. The stipulated values according to the CoC, Tier 2 appear already quite demanding.

It must be pointed out that these findings are based mainly on a theoretical analysis und should be verified by real circuit implementations, complemeted with field experience of GaN based devices.

The GaN technology is very young. The analysis carried out in this study is based on currently available components, including experience gained while implementing them in selected designs. It is reasonable to expect that the performance will quickly improve further. If we experience a similar progress as with Si MOSFETs the situation should be reevalueted again in not too distant future.

6.5 Further Considerations

The current (and future) mandatory limits in Europe and U.S. distinguish between basic voltage and low voltage devices, with a boundary between the two at 6 V. Many EPS operate at 5 V and another frequently occurring cluster lies around 18 V. The technically achievable efficiency at 18 V is clearly higher than at 6 V, irrespective of the implemented technology. Raising the distinction between the two voltage ranges to e.g. 11 V would allow higher limits for the large number of 18 V applications. The impact on energy savings would be considerable, as these are typically EPS with higher rated power. The devices in the 6 to 11 V range, which with this rule would fall under lower limits, are much less numerous and account for a clearly lower amount of energy.

The DOE level VI distinguishes between direct and indirect operation EPS, where the limits apply to the direct operation cases only. Direct operation means, the supplied device has no battery, or if it contains a battery, it can technically run without one, even if it cannot be removed physically. For indirect operation EPS the less stringent level V applies. Electronic equipment can be designed, such that they require the presence of a battery for the sole reason to avoid the tougher limits. It is questionable, whether this reflects the intention of the standardization body.

The definition of efficiency limits at very light load, e.g. at 10 % of rated power is crucial, as EPS frequently operate in a quasi-standby state. That means, the supplied equipment itself is in standby mode and consumes only a small percentage of its maximum power. For the EPS this is no longer standby mode, but very light load condition.

Another issue, not discussed here, are wireless charging systems. Today, they contribute only a small portion to the total number of EPS. It is foreseeable, however, that this will grow to a significant quantity. It is questionable, if at the considered power level below 250 W similar efficiencies and standby losses are feasible. This should be investigated separately.

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