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Final report

Precise Time Synchronization of Phasor Measurement Units with Broadband Power Line Communications

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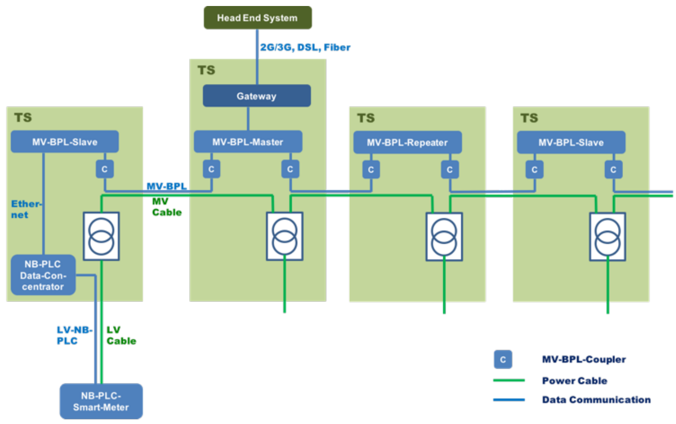
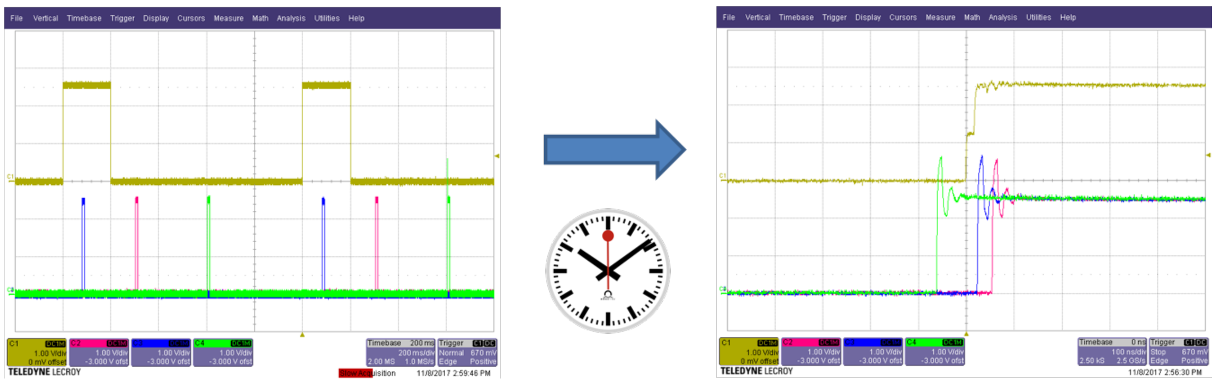
Precise Time Synchronization with Broadband Power Line Communications





Lucerne University of Applied Sciences and Arts

HOCHSCHULE LUZERN

Technik & Architektur

Date: 21 November 2017
Town**:** Horw

Publisher:
Swiss Federal Office of Energy SFOE
Research Programme «Grids»
CH-3003 Bern
www.bfe.admin.ch

Agent:
Lucerne University of Applied Sciences and Arts (HSLU)
Technikumstrasse 21, CH-6048 Horw
www.hslu.ch

Author:
Stephen Dominiak, Lucerne University of Applied Sciences and Arts, stephen.dominiak@hslu.ch
Ulrich Dersch, Lucerne University of Applied Sciences and Arts, ulrich.dersch@hslu.ch

SFOE head of domain:	Dr. Michael Moser, michael.moser@bfe.admin.ch
SFOE programme manager:	Dr. Michael Moser, michael.moser@bfe.admin.ch
SFOE contract number:	SI/501392-01

Swiss Federal Office of Energy SFOE
Mühlestrasse 4, CH-3063 Ittigen; postal address: CH-3003 Bern
Phone +41 58 462 56 11 · Fax +41 58 463 25 00 · contact@bfe.admin.ch · www.bfe.admin.ch

Zusammenfassung

Für dieses Projekt wurde ein komplettes Systemdesign für eine End-to-End Zeitsynchronisation (*Time Synchronization Protocol for PLUS PLUS-TimeSync*) zwischen im Verteilnetz verteilten Phasor Measurement Geräten (PMUs) über ein Breitband Power Line (BPL) Kommunikationsnetzwerk erforscht, konzipiert und realisiert. BPL-Modems sollen in Transformatorstationen des Verteilnetzes installiert und eine Kommunikation über das elektrische Verteilnetz ermöglichen. Dies als Teil der voranschreitenden Verteilnetzautomatisierung u.a. mit mission- und zeitkritischen Grid Monitoring und Automation (MTC-GMA) Applikationen. Anwendungsbeispiele mit PMUs sind die Netzzustandserkennung (State Estimation) sowie Fehlerlokalisierung (Fault Location), diese dienten als Referenzapplikation für dieses Projekt. In der ersten Phase des Projektes wurden die relevanten Applikationen erfasst und die resultierenden Anforderungen für eine BPL-Zeitsynchronisation abgeleitet. Dabei ist zu beachten, dass Applikationen unterschiedliche Anforderungen betr. der Kommunikation haben. Die strengste betrifft die Zeitsynchronisation, die über das gesamte BPL-Netz eine Genauigkeit von maximal ± 3.1 Mikrosekunden (µs) aufweisen muss. In der folgenden Entwurfsphase wurden sowohl die Anforderungen für die digitale Signalverarbeitung als auch für das Netzwerkprotokoll analysiert und entwickelt. Dazu kamen die Model-Based-Design Methode sowie Simulationen zur Anwendung. Das resultierende Systemdesign erlaubt nicht nur die Synchronisation aller Geräte einer BPL-Zelle untereinander, sondern auch die Synchronisation auf eine externe absolute Zeitreferenz ausserhalb der Zellen. Die Synchronisationslösung wurde auf der Basis einer an der Hochschule Luzern zuvor entwickelten Power Line data bUS (PLUS) BPL-Technologie als *Time Synchronization Protocol for PLUS (PLUS-TimeSync)* realisiert. Sie stellt eine standardisierte Schnittstelle zwischen den BPL-Modems und den Endgeräten zur Verfügung, welche auf einem ein Puls pro Sekunde Signal (1PPS) basiert. Die Tests wurden mittels realistischen Kanalbedingungen in Laborumgebung durchgeführt und zeigten, dass mit dieser Lösung eine Genauigkeit von ± 0.5 µs (also ca. Faktor 6 besser als die Anforderung) über zwei «Hops» in einem Netzwerk erreicht wird. In einem Folgeprojekt wird die Entwicklung eines MTC-GMA-BPL-Gesamtsystems konzipiert und realisiert.

Résumé

La conception d'un système de synchronisation des horloges au travers d'un réseau par courant porteur en ligne (BPL: Broadband Power Line) a été conçu afin de permettre la synchronisation entre des périphériques connectés de bout en bout, telle qu'une unité de mesure de vecteur de phase (PMU: Phasor Measurement Unit). Il est prévu que des modems utilisant la technologie BPL soit installés dans des stations de transformation afin d'établir une communication au travers du réseau électrique, laquelle fait partie d'un plus vaste système qui a pour but la surveillance et l'automatisation du réseau électrique et dans lequel la mission et le temps sont essentiels (MTC-GMA : Mission- and Time-Critical Grid Monitoring and Automation). L'estimation de l'état du réseau ou la localisation de pannes sont des exemples d'applications qui requièrent une PMU et elles sont considérées comme des applications de références pour ce projet. La première étape a été de définir les domaines d'application ainsi que les exigences d'une synchronisation des horloges sur un réseau BPL. Bien que chaque application a des exigences différentes, la plus stricte pour un tel système est la tolérance de synchronisation de bout en bout du réseau BPL qui est de ± 3.1 microsecondes. La seconde étape fut la phase de conception du protocole de communication requis pour la synchronisation d'horloges recourant à la méthode MBD (Model-Based Design) ainsi qu'à des simulations. Le système a été défini afin de permettre à chaque modem d'une cellule de se synchroniser entre eux mais également de se synchroniser sur une horloge de référence se situant en dehors de la cellule. La synchronisation de bout en bout du réseau utilise une interface standardisée entre le modems BPL et les périphériques, basée sur un signlal de une pulstion par seconde (1PPS). La méthode de synchronisation a été réalisée à l'aide de la technologie BPL PLUS (Power Line data bUS) développé à l'HSLU. Finalement, des tests ont été effectués en laboratoire sur un canal réaliste et une synchronisation avec une précision de l'ordre de ± 0.5 µs a pu être atteinte, au travers de deux modems connectés en cascade. Le développement du projet se poursuit afin d'obtenir un system de synchronisation d'horloges BPL MTC-GMA complet.

Summary

A complete system design for the end-to-end time synchronization between end devices of a Phasor Measurement Unit (PMU) application over a Broadband Power Line Communications (BPL) network has been conceived. It is foreseen that BPL modems will be installed within secondary substations enabling communications over the electric grid as part of a larger system for mission- and time-critical grid monitoring and automation (MTC-GMA) applications. State estimation and fault location are examples of such applications requiring a PMU and are considered as reference applications for this project. The first step in the process was to capture the relevant use-cases and the resulting application requirements for the BPL time synchronization. Although each application has different requirements, the strictest requirement is that the time-synchronization solution must provide an end-to-end accuracy over the BPL network of ± 3.1 microseconds. This was followed by a design phase in which both the necessary digital signal processing as well as network protocol required for the time-synchronization have been developed using model based design and simulations. A system design has been defined allowing each BPL cell to not only synchronize all devices within the cell, but also synchronize to the absolute time outside of the cell. End-to-end synchronization is realized by providing a standardized interface between the BPL modems and end devices based on a one pulse per second (1PPS) signal. The synchronization solution has been realized on top of HSLU's existing Power Line data bUS (PLUS) BPL technology. Tests have been carried out in a laboratory environment on realistic channel conditions and it has been shown that an accuracy in the range of ± 0.5 µs can be achieved over two "hops" in the network. Work continues in a follow-up project for developing a complete MTC-GMA BPL system.

Contents

1 Introduction

1.1 Overview

Worldwide, increasing pressure is being placed on the electric grids and in particular the Medium Voltage (MV) grids due to the steadily increasing introduction of Distributed Energy Resources (DER). The highly time-dynamic character of such power fed into the grid by a vast amount of spatially distributed sources combined with the decreasing ratio of stabilizing rotational mass leads to substantial challenges for the future grids to keep them robust enough for the requirements and expectations of the consumers. Grids must be able to accommodate new energy flow patterns in a considerably more dynamic environment.

Therefore, protection and automation systems are quickly gaining importance not only for the transmission grid but increasingly at the distribution grid level for the asset management programmes of Distribution System Operators (DSOs). This leads to the need not only for increasing the monitoring of the grid, but also to actively detect and mitigate the influence of potential faults in the grid. This requires critical applications such as voltage/congestion control and fault detection/location.

Phasor Measurement Units (PMU) measuring synchrophasors and Line Differential Protection (LDP) provide examples of such critical applications. They offer promising approaches for such high precision grid monitoring and automation. However, the communication requirements of such applications (high availability, low latency) provide a significant challenge to the communication infrastructure. Currently, there is no clear vision in the market on the exact communication technologies and network topologies which could fulfill these requirements. In any case there is a risk that the application of such applications – which are well installed in the transmission grid today - in the distribution grid might lead to unacceptable cost figures which might prevent or in the best case delay the acceptance of such applications by DSO customers.

Such applications call for a larger amount of control and automation technology, but requiring at the same time cost-effectiveness in order to be bearable for the customers. For example, due to the pressure induced by the highly dynamic generation of renewables, it is no longer enough to use local measurements (V, I phasors and P,Q values) within each Secondary Substation (SS) for automation and protection, but more advanced monitoring and protection applications which require the exchange of measurements data between SSs are required. Distributed measurements between SSs will also be adding value by allowing the application of synchrophasors to the distribution level, helping to achieve efficient control of bidirectional power flows due to the massive integration of renewable energy systems.

These types of functionalities present a real challenge as the complete chain is involved, from the sensors, protection relays and various electronic devices integrated in the cubicle to the communication infrastructure to exchange the data between the SSs. Such communication infrastructure has to fulfil very high requirements regarding availability and latency, as will be described later on, and can therefore be considered as a Mission- and Time-Critical (MTC) communications infrastructure.

Considering the state-of-the-art in the communication infrastructure, there has already been a substantial change, as not long ago the communication equipment installed in these installations communicated through serial protocols with dispatch centers, due to the fact that the communication requirements were not very high in the electrical sector. However, still today there are very few rollouts in which communications between SSs is provided.

Due to the large amount of SSs installed at the distribution level, the cost effectiveness of such applications including the communications system plays a critical role. Whereas Primary Substations (PS) at the transmission level are typically in an order of tens or few hundred, SSs are in an order of thousands or even tens of thousands for large utilities. A typical rule-of-thumb for DSOs is that the cost of equipment protecting the infrastructure should be less than 10% of the cost of the infrastructure to be protected. This further motivates a cost reduction of the protection equipment at the distribution level compared to the transport level.

Today's communication technologies do not completely fulfil the communication requirements for the above described applications with costs which are tolerable for a wide deployment in the distribution grid:

– Cellular networks (2G/3G/4G): latency too high, availability dependent upon the network operator

– Fiber Optic (FO) networks: fulfils the communication requirements but a full FO infrastructure is not bearable due to its significantly high costs

– MV Broadband Power Line Communications (MV-BPL): today's commercial technology does not support the reliability and latency requirements.

New solutions are therefore required.

1.2 MV-BPL Network

In this section an overview of the specific characteristics of a MV-BPL network will be provided which is partially necessary in order to understand the time-synchronization concepts presented later in this document. The MV distribution grid (i.e. 1 - 36 kV) comprises mainly underground cables, overhead lines and related infrastructure, including SSs. The MV grid mainly differs from the Low Voltage (LV) access and indoor grid in terms of the physical topology, cable/wire types and link distances. A broad range of SSs can be found depending upon the area (urban, suburban or rural) and consumption levels. Big utilities may operate hundreds of thousands of SSs. Such a heterogeneous set of SSs, however, presents a fundamental common infrastructure: MV lines which interconnect SSs among themselves and to PSs. The underlying topology of this interconnection can be considered as a meshed ring topology in which a certain amount of redundancy is provided between SSs and PSs. Links between SSs are usually very heterogeneous with several different cable types as well as a combination of overhead lines and underground cables being found in a single geographical area. While underground cables represent point-to-point links with relatively stable loads and impedances, overhead MV lines, on the contrary, may present taps in a tree-like topology.

One typical misconception regarding the use of BPL in MV grids is that link distances are too long to support any reliable communications. Attenuation is a very important factor and will increase with distance and frequency, and as a consequence, longer MV links have to use frequencies in lower bands to guarantee a minimum performance. While it is true that BPL cannot achieve 100% coverage of all links in a typical MV grid (especially in rural areas), measurements have shown that raw data rates of several 10's of Mbps are possible for links up to 500 m. A general rule-of-thumb is that older paper insulated lead covered and newer polyethylene insulated cables will support sufficient throughput on cables lengths up to 450 and 900 meters, respectively. Measurements have been performed on overhead wires in which it was determined that reliable communications can be supported on links up to at least 2 km. Analysis of actual MV grids in Spain and Switzerland have shown that MV-BPL can therefore cover 90%-95% of the overall grid.

As previously mentioned, the topology of a MV grid can be described as a ringed mesh topology in which SSs may have redundant paths to a single or multiple PSs. This means that SSs will have anywhere from one MV feeder (endpoint) to several feeders per station. For the case of multiple feeders, individual phases (3-phase system) are connected across a common bus bar. Feeder lines are switched within the electrical grid such that a connected tree structure without loops is achieved. Load management and fault isolation can lead to manual or automated switching being performed in the grid. In order to achieve independence from the underlying electrical grid topology, but also to provide increased reliability through redundancy (redundant paths) coupling is generally performed on the feeder side of the switch (opposite the bus bar). This ensures that the logical BPL network topology remains independent of the MV grid’s current switched state.

A critical aspect in the large-scale deployment and thereby the scalability of a MV-BPL network is defining a set of suitable guidelines for the cluster planning. In order to provide a scalable solution which can provide BPL coverage of a large MV grid, the network is typically divided into several clusters. As in cellular wireless networks, the communication nodes in a large-scale BPL network must be allocated to different clusters and channels must be assigned to these clusters. Each cluster consists of one master node which connects the cell to the backbone infrastructure, one or more repeaters used for extending the coverage and one or more slaves. Application endpoints may be attached to any BPL node within the network and the BPL network acts as a layer 2 switched Ethernet network. The master is the central node that controls and assigns resources to all the nodes in the network.

All nodes within a single cluster must be configured to operate on the same channel. As no dynamic channel allocation is supported, channels must be manually allocated to clusters such that neighbouring clusters operating on the same channel will not interfere with each other. Interference between neighboring clusters can be avoided by using a guard distance between the clusters which are using the same channels. Because of this guard distance, gaps or regions which cannot be covered by BPL may exist in the network (see example in Figure 2). To increase the amount of channel reuse within the network and minimize the gaps in coverage, multiple channels are used similar to the channel assignment problem known from mobile wireless networks.

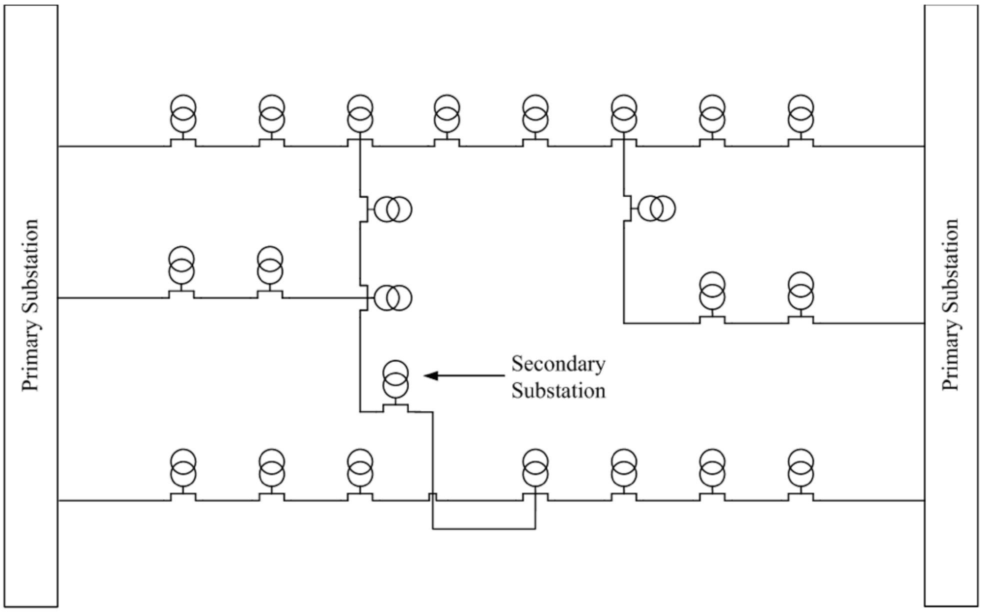


Figure 1: Simplified example of a ringed-mesh topology

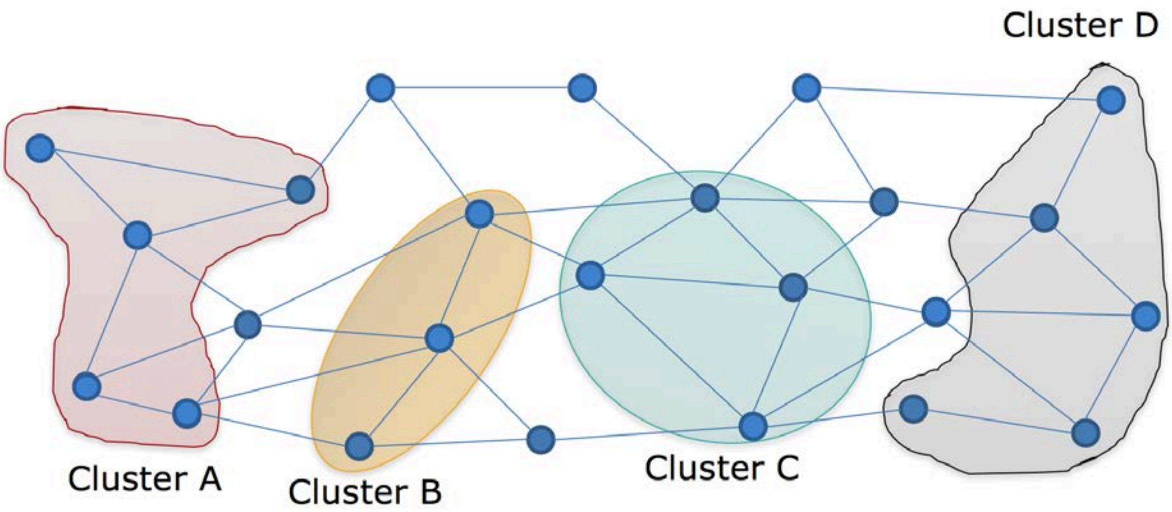


Figure 2: Example MV-BPL clusters in a MV electric grid

1.3 Motivation

The motivation behind this project is the development of a new Grid Monitoring & Automation (GMA) solution which takes advantage of the full potential of MV-BPL for enabling MTC-GMA applications in the MV grid. The main driver behind this idea is to provide increased observability and stability to the grid using functionalities previously only used in transmission grids, but for a much lower price that will enable a broad rollout of these functionalities into the distribution grid.

The state-of-the-art in MV automation developments over the last years has provided visibility to the MV grid all over the network, especially with the availability of accurate grid measurements. This visibility allows centralized advanced automatic functions to be realized. The future vision is to provide a synchronized exchange of GMA data from the installed equipment between neighbouring SSs which would provide much more value through optimized distributed monitoring, protection and automation functions (PMU, LDP).

The idea is to achieve this through a further development of the MV-BPL technology by enabling MTC-functionality with time synchronization, higher availability and low-latencies permitting the PMU and LDP functionality. The basis for this development is the Power Line data bUS (PLUS) BPL technology which has been developed at the Lucerne University of Applied Sciences and Arts (HSLU). The major advantage being the fact that HSLU has complete control over all aspects of the technology allowing the necessary features and optimizations for such vertical applications to be realized.

In order to achieve the overall goal, the neighboring SSs would be interconnected through this low-latency and high-availability MV-BPL network. The application devices could thus exchange synchronized phasor measurements creating a synchronized monitoring area. This would allow the instantaneous exchange of data and online system analysis of the area to be performed. Furthermore, the LDP application would provide automatic fault detection and mitigation thereby protecting the DSO’s important infrastructure and providing higher availability of the electric grid.

The major value of the proposed communication solution with MV-BPL is the low cost. For such functionality – today implemented on the transmission grid level only - a very expensive fiber optic communication would have been required. With the MTC-MV-BPL solution this could be avoided, as the MV lines between the SSs are re-used as the communications medium.

This would lead to a next step in the implementation of MV-BPL clusters. A MV-BPL cluster consists of a number of SSs which are connected together forming a MV-BPL network (see Figure 3 as an example). Within a cluster a single MV-BPL modem will simultaneously act as a the network master and serve as a gateway between the MV-BPL network and the Wide Area Network (WAN). The MV-BPL modems within other SSs serve as repeaters or as slaves. The potential for establishing multi-hop communications allows a single MV-BPL cluster to cover a large geographic area. Within this area only a single (typically expensive) connection to the WAN is required rather than a single connection per SS. This reduction in the number of expensive WAN connections provides a further cost advantage for MV-BPL.

Up to now such MV-BPL clusters have been implemented for Automated Metering Infrastructure (AMI). For this use-case, smart meter data is collected by the data concentrator using narrowband PLC technology for the connection between the SS and the meter. The data from the data concentrators in each SS is then further aggregated within the MV-BPL network and transmitted to the head end system through the gateway at the MV-BPL master. The largest current deployment of this solution is in Spain with the utility Iberdrola [3]. However, the network performance requirements for the AMI application are rather relaxed compared to the proposed GMA applications.

The proposed MTC-MV-BPL system would mean that such a cluster would behave as a real-time and reliable Local Area Network (LAN) rather than only as a channel to connect each SS to the head end system. Such a MTC-MV-BPL solution would also support PMU functionalities by synchronising the accurate phasor measurements provided by the automation solutions within an SS over the MV-BPL cluster.

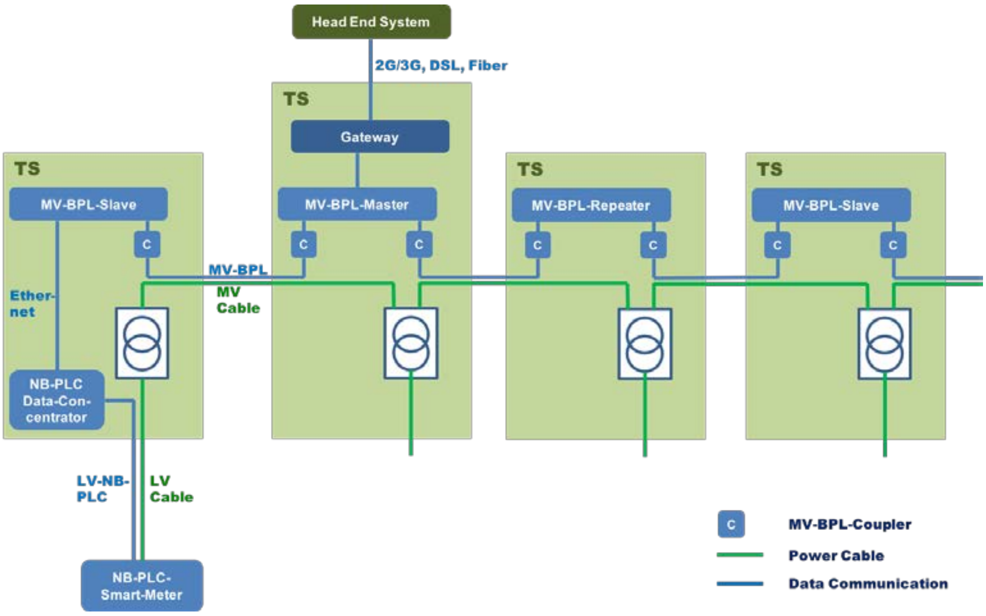


Figure 3: MV-BPL Cluster

2 Project Outline

2.1 Project Goal

The goal of this project is to develop a solution for a highly accurate time synchronization between PMU application devices on top of a MV-BPL network. The developed MV-BPL solution with time-synchronization will provide a cost-efficient alternative to existing PMU systems based on FO and Global Positioning System (GPS)-based time-synchronization. The developed solution will be integrated into a series of existing BPL prototypes and the performance will be verified within a representative laboratory environment.

2.2 Work Packages

The work within this project has been carried out within seven work packages and is described in detail below.

2.2.1 WP1 – Requirements Analysis

This first step within the project was to investigate and analyze the different potential GMA applications using a PMU. Applications have been identified through discussions with suppliers for the Spanish utility Iberdrola, discussions with the Swiss utility BKW as well as an analysis of other R&D projects.

The following projects were analysed in detail: GridBox (BFE), PMU EPFL/SIL, Commelec (EPFL), GridEye V2.0, GridEye V3 (CTI), SMILE.

Various Wide Area Monitoring Protection and Control (WAMPC) applications such as real-time state estimation and protection rely on synchronized monitoring information about the state of the grid. Most often this monitoring is performed by synchrophasor measurements from PMUs.

When applying PMU applications to the MV distribution grid we have multiple PMUs distributed at strategically significant locations throughout the grid in order to provide full network observability. The measured data from each PMU must be synchronized to an absolute time reference and is then transmitted to a Phasor Data Concentrator (PDC) which collects the data and provides an initial processing before providing the data to the relevant application devices. This architecture is shown in Figure 4.

The use of PMUs within the distribution grid opens the door for a wide variety of different use-cases which use the information in different ways:

- Automated system reconfiguration / system restoration with controlled islanding
- State estimation
- Fault location
- DER penetration planning
- DER control
- MV alarms/event detection
- Post mortem analysis

Based on the aforementioned use cases, a set of requirements was then defined. The requirements are summarized in Table 1 with the most critical requirements highlighted in red. Although each application has different requirements, the most strict requirement in terms of time synchronization performance comes from the PMU application in which an accuracy of ± 3.1 µs must be provided. This requirement comes from *IEEE C37.118.1-2011, IEEE Standard for Synchrophasor Measurements for Power Systems* [7]. In that standard a maximum allowable Total Error Vector (TVE) of 1% is defined. This corresponds to a time error of ± 31 µs for a 50 Hz system. A time source that provides accuracy at least 10 times better than ± 31 µs (i.e. ± 3.1 µs) is highly recommended. For less strict applications such as fault location a tolerance of ± 100 µs is acceptable.

In parallel to the use-case definition, the existing time-synchronization solutions were analysed in detail with especial detail given to the IEEE 1588 Precision Time Protocol (PTP) [5] and GPS-based solutions. A literature review was also performed in which performance details of these technologies from different field trials and tests were captured.

Assuming that the PMUs are located within SSs, providing an absolute time-reference in this distributed environment poses a significant challenge. GPS may be used to achieve this synchronization, however its widespread use at the SS level is not considered due to the difficulties in antenna/hardware installation as well as the security risk due to jamming and sabotage (SSs are not as well isolated from attacks as PSs). For this reason network-based synchronization methods such as the IEEE 1588 are more suitable. The use of IEEE 1588, however, requires a FO network between SSs which is a very expensive solution. For this reason there is a definite need to provide such high precision time-synchronization, but with a cost effective solution.

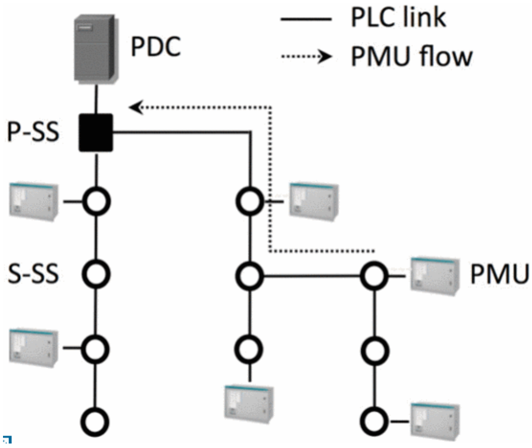


Figure 4: PMU architecture for the MV distribution network

Requirement	AMI	LDP	Synchrophasor
Transmission Frequency	Once per day	**Constant transmission of measurement values**	**Constant transmission of measurement values**
Bandwidth	**100kbps per SS**	10 kbps per SS	65kbps per SS
Latency	Not relevant (time-intolerant)	**< 5ms**	< 20ms
Bit error rate	No specific requirement	**10^{-6} or better**	No specific requirement
Availability	Network must be available for transmission of data only once per day	**99.99% availability**	High-availability if real-time state estimation is performed
Data Integrity	No specific requirements[1]	**100% data integrity[2]**	**100% data integrity[2]**
Time-synchronization Accuracy[3]	Not required	±100µs	**± 3.1µs**

Table 1: MV-BPL performance requirements

2.2.2 WP2 – Digital signal processing algorithm design

In WP2 the necessary adaptations of the digital signal processing algorithms were investigated. The basis for the BPL solution is the Power Line data bUS (PLUS) technology which HSLU has developed separately for avionics applications. PLUS has now been adapted in order to provide the necessary time synchronization over the BPL network. The physical layer of PLUS is based on the IEEE 1901 BPL standard [4]. A critical part in any network-based time-synchronization solution is providing a very accurate time-stamping at both the transmitter and the receiver. This time-stamping must be performed at a well-known place within the Tx and Rx chains, respectively. For reasons of accuracy it was decided to move the time-stamping down to the physical layer (similar to what is done with the IEEE 1588 protocol). However, the additional challenge with BPL is due to the signal distortion and resulting signal echoes due to the transmission channel. This means that multiple time-delayed

[1] Undetected errors will not lead to a large impact on operations.

[2] The typical definition is a probability of undetected error of 10^{-9} per operational hour.

[3] We assume here that time-synchronization is provided by the network so it's a requirement of the network.

versions of the transmitted signal will appear at the receiver. Within the MV grid with long transmission distances, these time-differences between echoes can be rather significant.

It was necessary to optimize the existing frame synchronization algorithm which detects the presence of the BPL signal based on the preamble (common signal known at the transmitter and receiver – see Figure 5). This optimization was necessary due to the fact that the Orthogonal Frequency Division Multiplexing (OFDM) modulation used within PLUS is highly tolerant to these echoes meaning that for the reception of the BPL frame a high precision of synchronization is not necessary. However, this precision was not sufficient when considering the requirements of time-synchronization. The design of this synchronization algorithm was performed using Model-Based-Design (MBD) within the existing PLUS physical layer simulation platform (PhySimPlatform). The PhySimPlatform is based on MATLAB / Simulink and provides a full transceiver model with realistic channel and noise models (see Figure 6). Simulation results have shown that a synchronization accuracy of a few hundred nanoseconds (ns) should be able to be achieved.

Another critical question which was also addressed within WP2 resulted from the necessity to synchronize two asynchronous clocks on the target hardware platform Xilinx Zynq. The Xilinx Zynq System-on-Chip (SoC) serves as the basis for the PLUS BPL prototypes. Two different options were available for timestamping: an implementation in the processing system (software controlled) or an implementation in the FPGA (hardware controlled). Unfortunately, the documentation did not define enough details on each option in order to determine the achievable accuracy. Therefore, it was necessary to implement a basic realization of each option in order to perform an evaluation of their accuracies. In the end the results led to the decision that a hardware-based timestamping is required in order to achieve the targeted accuracy.

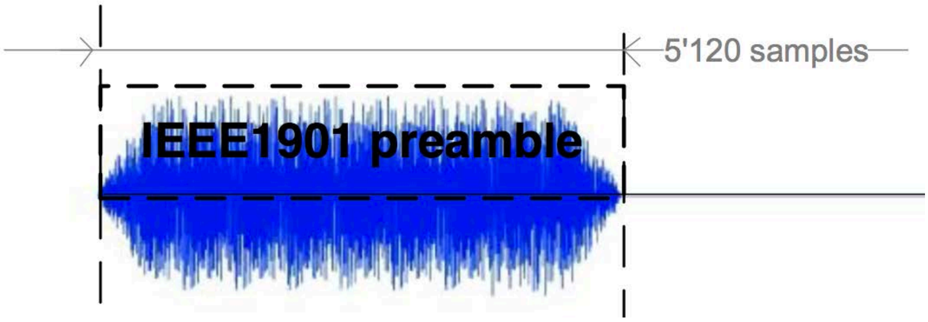


Figure 5: IEEE 1901 preamble signal

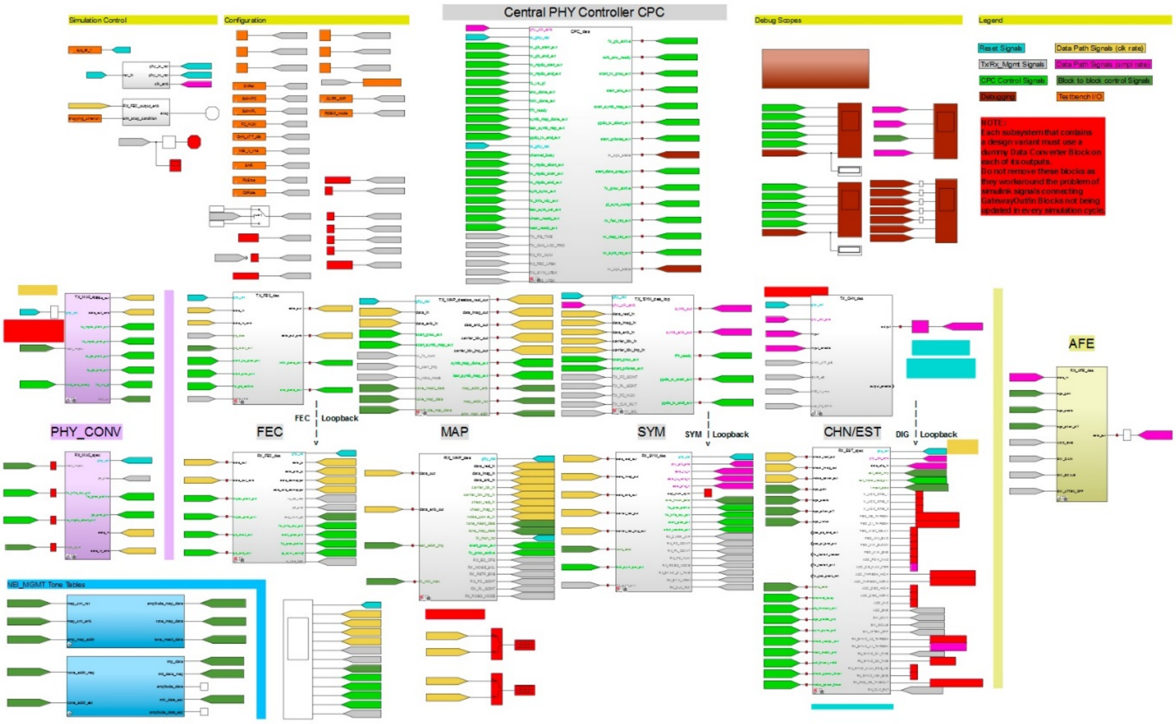


Figure 6: PhySimPlatform model of physical layer

2.2.3 WP3 – Protocol design

Within this WP the overall protocol design of the MV-BPL time-synchronization solution was performed. The developed protocol is known as *Time Synchronization Protocol for PLUS* (*PLUS-TimeSync*). The work started out with the definition of a suitable and scalable architecture. This was achieved by dividing the end-to-end synchronization into four different zones as is shown below in Figure 12. This hierarchical architecture was selected in order to provide a scalable solution in which an optimized solution is provided for the specific technical characteristics of each zone. This architecture also takes into consideration the cellular nature of a larger BPL network in which each cell is controlled by a MV-BPL master modem.

In addition to the theoretical analysis and design of the protocol within this work package, a simulation tool was developed based on the event-based simulation tool OMNeT++. Event-based simulation tools provide a very efficient way of simulating systems in which the state changes as a result of events such as is the case in packet based networks. The advantage of such simulation tools for time-based simulation is that the exact times of events can be captured such that no errors due to time scaling will occur. This allowed the time-sychronization accuracy within the BPL network to be evaluated using MBD. The influence of different communication channel characteristics such as packet loss and delay was evaluated. Protocol specific parameters such as the necessary update rate for achieving the targeted accuracy were also evaluated.

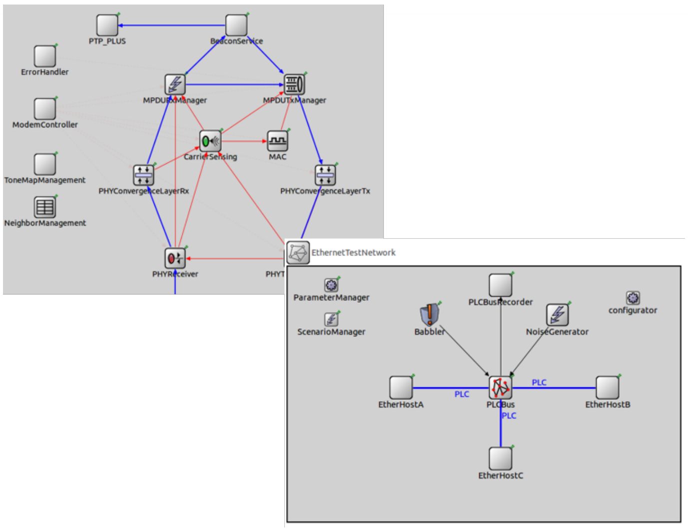


Figure 7: OMNeT++ simulation environment

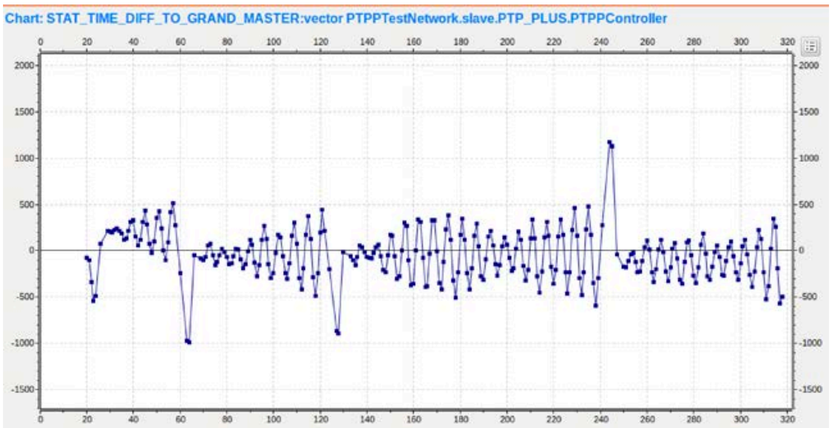


Figure 8: Example simulation results - time difference to grandmaster versus time

2.2.4 WP4/WP5 – Implementation of the Digital Signal Processing and Protocol

A design decision was reached within the project for implementing the time synchronization protocol completely within the Programmable Logic (PL) of the Xilinx Zynq chip in VHDL. WP4 and WP5 were orginally planned to be a hardware and software development WP, respectively. However, with the development being completely in hardware, they were combined into a single WP for implementing the Digital Signal Processing (DSP) and protocol required for PLUS-TimeSync. However, even in the development stage MBD also plays an important role. Critical parts of the realization were implemented using Xilinx System Generator which is a plugin for MATLAB Simulink. It allows a 1:1 model of the actual implementation to be realized which can be simulated as well as used to generating the resulting VHDL code. System Generator also provides an easy to understand graphical model of the realization. An example is shown in Figure 9 for the fraction counter which is later described in section 3.5. Cycle accurate simulations can be carried out in order to resolve complex timing issues at an early stage. An example of the output of such simulations is shown in Figure 10. The output of these WPs was the VHDL code for the PLUS-TimeSync DSP and protocol.

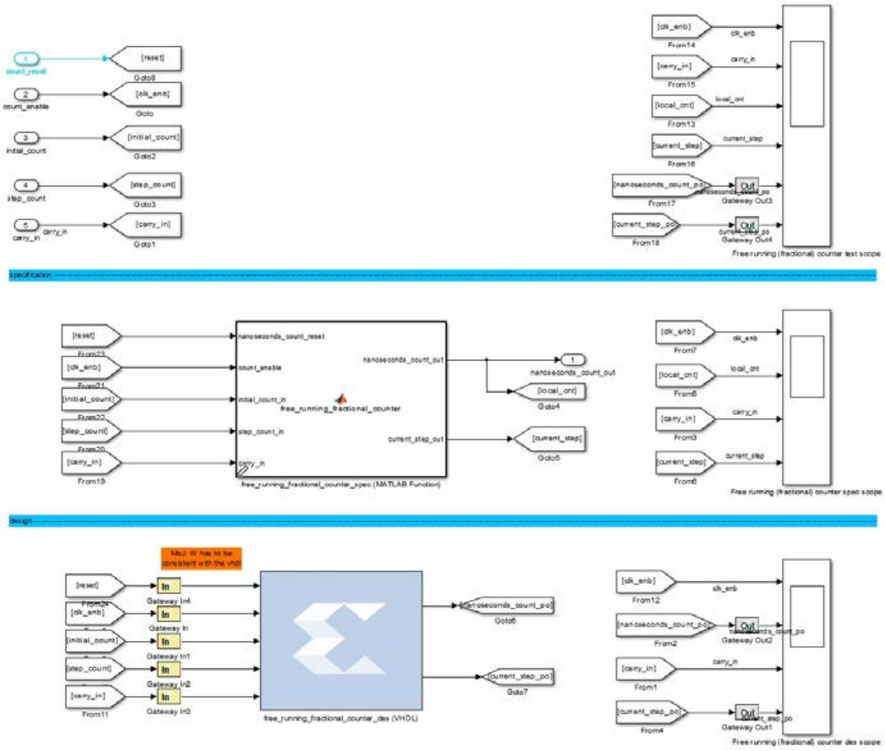


Figure 9: Example Xilinx System Generator model for the fractional counter

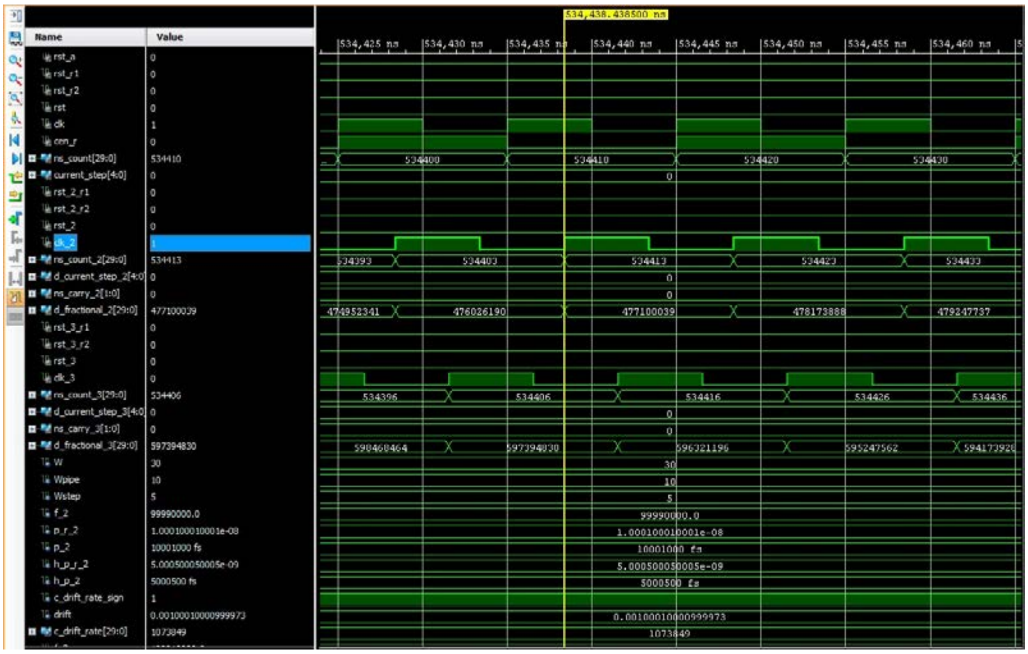


Figure 10: Xilinx System Generator signal simulation

2.2.5 WP6 – PLC Modem Integration

In this WP, the PLUS-TimeSync module developed previously was integrated with the other modules for PLUS. From this a bitstream was generated. This bitstream was deployed to the available PLUS prototypes. Functional testing was then performed. However, due to the complex nature of a digital hardware realization, several iterations were required before the integration was completed. Debugging of digital hardware proves to be extremely challenging. While the values of certain hardware registers can be read from the software console, if the problem cannot be identified in that form, then a logical analyzer must be integrated into the hardware design and various hardware signals must be observed in order to isolate the issue. However, the proper signals to include for debugging purposes must first be identified. An iteration round can easily cost a senior hardware engineer a day or more even if the resolution only requires a minor change to the VHDL code. The output of this WP was an integrated firmware on for the PLUS prototypes in which all functionality for PLUS-TimeSync had been verified.

2.2.6 WP7 – System Testing in a Laboratory Environment

In this final WP the PLUS-TimeSync firmware was deployed and tested on a number of PLUS prototypes. Due to the challenges in performing field trials on MV networks, laboratory testing was targeted for this initial project in the overall MTC-MV-BPL development. Several different performance tests were performed in order to verify that the PLUS-TimeSync solution can fulfill the necessary requirements. This testing in described in more detail in Chapter 4.

3 Time Synchronization Protocol

3.1 Summary of Time-Synchronization

Given the fact that the MV-BPL network architecture is based on a master-slave architecture, establishing time-synchronization also based on a master-slave architecture presented the optimal solution. In this way one does not have to deal with the inherent challenges of performing time-synchronization over the alternative peer-to-peer architecture.

The clocks on the MV-BPL modems can be considered as unreliable clocks. A clock consists of a stable oscillator driving a counter. In order to keep the cost of the modems at a tolerable price point, crystal oscillators (XTAL) are used as the source of the clock. A requirement provided by the standard upon which the MV-BPL solution is based, IEEE 1901, is that the XTAL must have an accuracy of ± 50 ppm. Any two clocks in the MV-BPL network can therefore be running at a maximum frequency difference of 100 ppm. As a 100 MHz clock source is used, this can lead to a maximum frequency difference of 10 kHz.

Synchronization of any two clocks will actually consist of two processes:

– Syntonization: Syntonization is actually a frequency synchronization in which it is ensured that the two clocks are running at the same rate, i.e. the oscillator sources driving the counter have the same relative values. With proper syntonization the clocks have no relative drift.
– Synchronization: With this process, it is ensured that the clocks agree on the time of day or have the same relative counter values at any given time instant. With proper synchronization, the clocks have no relative offset at any given point in time.

Both of these processes are essential for a clock synchronization algorithm. If, for example, syntonization would not be performed, the maximum frequency difference of 10 kHz previously mentioned would lead to a clock drift 100 µs/s. With this drift, even after one second this would put two clocks outside of the required time synchronization. Therefore, if highly precise synchronization under all conditions with unreliable clocks is desired, then both processes must be performed.

As MV-BPL is a packet-based network, clock synchronization must also be performed over a packet-based network. An important characteristic of performing time synchronization over a packet-based network is that the clock value of the master must be distributed to the slaves within packets. For this purpose a timestamp or snapshot of the clock is taken and sent within these packets. However, it is important to consider the delay from the time at which the timestamp was taken until the time when any correction would be applied at the slave. This delay must then be estimated and compensated (corrected) in order to provide a high degree of accuracy. One component of this end-to-end delay is the propagation delay across the actual communications channel which is based on the actual speed of the communications signal propagating within the cables between modems. A typical rule-of-thumb for copper wires is that this delay is around 5 ns/m. However, much larger components contributing to the end-to-end delay may come from the upper communications layers. Here there could be queing delays, bus access delays, processing delays, re-transmissions, etc. Delays can increase to the order of several hundred microseconds or even seconds. As the end-to-end delay between the time when timestamps are made at the transmitter and then receiver are the critical criteria, it becomes adventageous to perform timestamping on the lowest communications layer as possible in order to increase the accuracy. This is shown graphically in Figure 11. NTP performs timestamping at the application layer compared to PTP (IEEE 1588) which performs timestamping between the data link and physical layers. As will be shown later, in the developed solution timestamping is performed even within the physical layer which reduces the end-to-end latency to be measured down to only the propagation delay.

The following sections will provide a description of the protocol which has been developed for precision time synchronization over a MV-BPL network (PLUS-TimeSync).

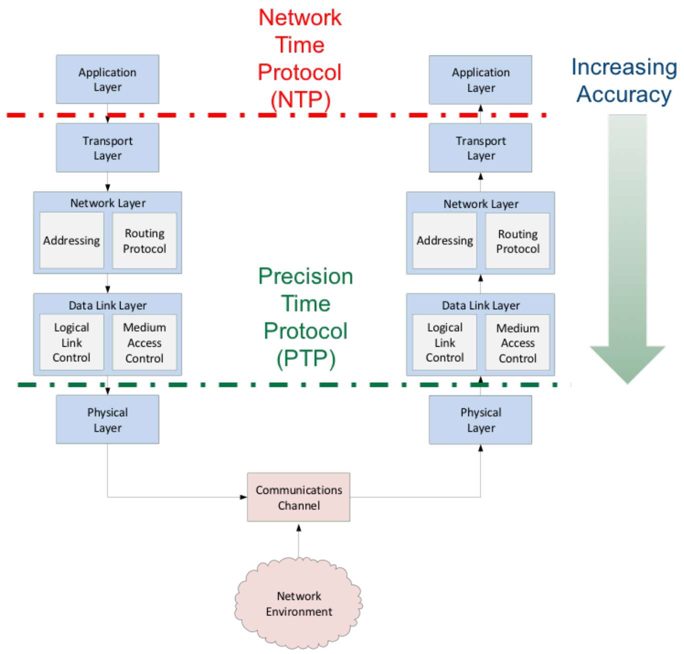


Figure 11: Timestamp accuracy

3.2 System Overview

The Time Synchronization Protocol for PLUS (PLUS-TimeSync), defines a solution for a highly accurate time synchronization between PMU application devices on top of a MV-BPL network. The developed BPL solution with time-synchronization will provide a cost-efficient alternative to existing PMU systems based on fiber optic communications and GPS-based time-synchronization. A system design has been defined allowing each BPL cell to not only synchronize all devices within the cell, but also synchronize to the absolute time outside of the cell.

The end-to-end synchronization has been divided into four different zones as is shown in Figure 12. This hierarchical architecture was selected in order to provide a scalable solution in which an optimized solution is provided for the specific technical characteristics of each zone. This architecture also takes into consideration the cellular nature of a larger BPL network in which each cell is controlled by a MV-BPL master modem. This also allows any loss of synchronization to error conditions to be partially contained within a single zone meaning that the impact will not have a direct impact on the complete system.

The different zones are summarized here and described in more detail in the following sections (refer to Figure 12 for the location of the zone in the architecture):

Zone A: Synchronization of the grand master clock at the BPL master with the absolute time. This synchronization takes into consideration providing not only a highly accurate solution, but also a solution that is robust against potential security attacks. For that a combination of different technologies are used allowing a sanity check to be made against the obtained time-synchronization and also providing a fallback solution should one of the synchronization sources be lost.

Zone B: Synchronization across the MV-BPL network. The MV-BPL master acts as the time synchronization grandmaster. In order to ensure a standardized BPL solution can be provided this network based synchronization was defined within the framework of the IEEE 1901 BPL standard. Although the standard does not directly allow for a synchronization with the required accuracy the necessary modifications were identified and defined. The required message exchange, however, makes use of management messages which are defined by IEEE 1901 using vendor specific extension fields.

Zone C: Synchronization within the BPL modem between the clocks for zone A and zone C. The synchronization in zone A and zone C is, in principle, running asynchronously. However, in order to provide very high accuracy these two clocks must be synchronized. The developed design takes into consideration the specifics of the target hardware platform which is the Xilinx Zynq System-on-chip.

Zone D: Synchronization to end devices using a standard one pulse per second (1PPS) interface. This provides the most accurate and simple means to synchronize to an end device. Along with the 1PPS signal the absolute time is output as a NMEA sentence. Therefore, the BPL modem always acts as the time master and the attached device is the time slave. This allows the developed solution to interface to existing application devices (even beyond that of the PMU application) without requiring modifications to the devices. This interface is very similar to the absolute time input interface used in Zone A.

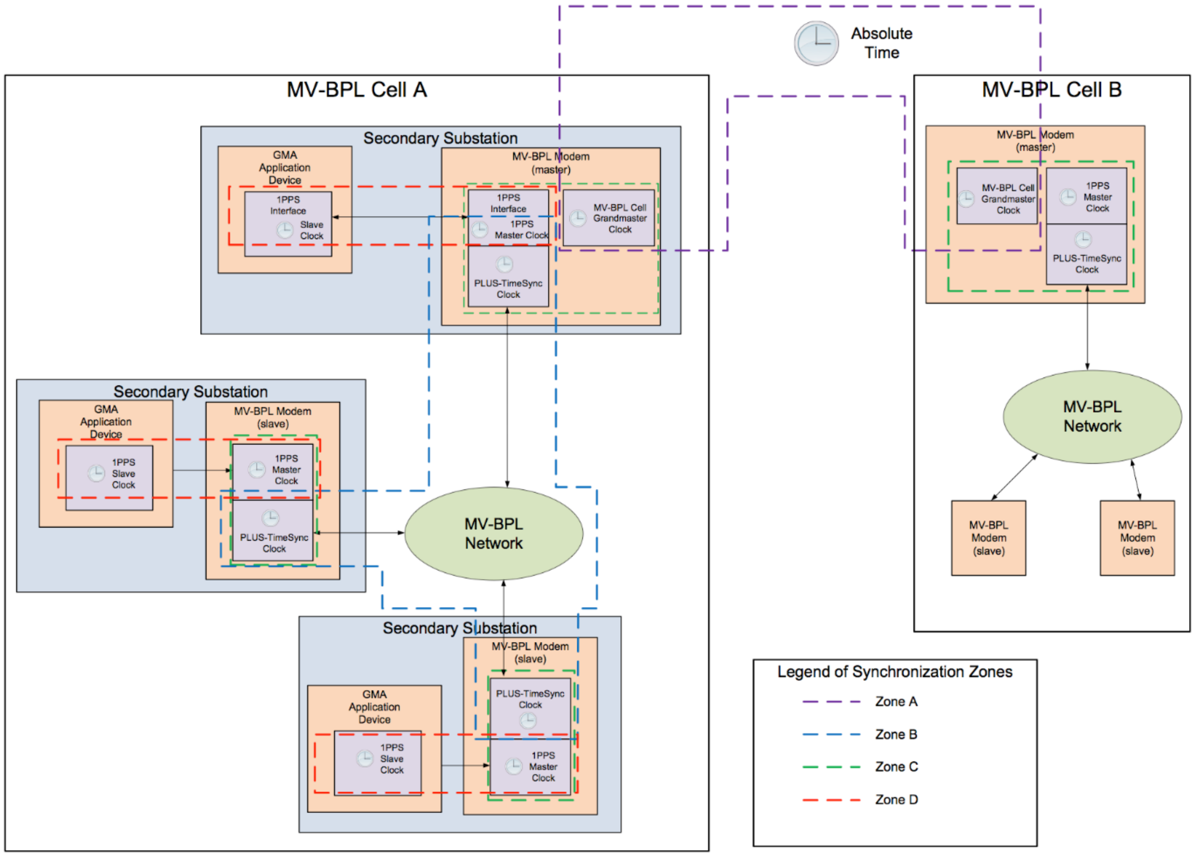


Figure 12: PLUS-TimeSync System Architecture

3.3 Zone A: Absolute Time Synchronization

As previously described a MV-BPL network will consist of a number of clusters. Each cluster operates independently and is controlled by a MV-BPL master. According to the overall system requirements application devices belonging to different MV-BPL clusters must still be synchronized relative to each other. This means that each MV-BPL cluster must be synchronized to each other. In order to achieve this each MV-BPL cluster will synchronize independently to the absolute time through the MV-BPL cluster master modem. This builds upon the scalable solution provided by the MV-BPL network meaning that a failure in the time-synchronization of one MV-BPL cluster will not have an influence on the time-synchronization of any other MV-BPL clusters. As each MV-BPL cluster contains one or more master MV-BPL modem that controls that cluster, the SS containing these master modems becomes a natural place for the installation of a reliable absolute time source. It should be noted that in the previous generation of MV-BPL technology the loss of a master led to the complete communications loss of all the modems in the network. The overall MTC-MV-BPL solution that is being developed will not have this limitation. Cluster-wide communications will still be possible, even if the master is lost.

Practically two different absolute time sources exist which could be used for this system: GPS and/or an atomic clock. GPS has the disadvantage that it requires the installation of a GPS antenna which could be susceptible to either a physical attack or jamming. While the price of Rubidium-based atomic clocks have come down significantly, it is still more expensive than a GPS-based solution.

The MV-BPL master will thus synchronize to the absolute time using either GPS or an atomic clock. The problem with this solution is that it does provide a potential single point of failure in the system. In order to provide an added layer of reliability (should that be required by the application requirements) two potential solutions are available:

– The MV-BPL solution provides a redundant master concept. This means that another MV-BPL modem in the network can potentially take over the role of the master if it should detect that the master has failed. In this case the redundant master could also be provided with a GPS and/or atomic clock. The existence of the absolute time source at the master is then introduced into the algorithm for assessing the availability of the primary master modem. Should it be detected that the absolute time source at the primary master has failed or is not available for any reason, then the backup master would take over the role of master for the MV-BPL cluster including the role of time grandmaster for that cluster.
– Another alternative is providing two absolute time sources at the MV-BPL master, i.e. GPS and atomic clock. The master modem could monitor both of these time sources and fall back to one or the other should one of them fail. This would not provide as high a reliability as the previous mentioned solution as a complete failure of the master modem would lead to a cluster-wide loss of the absolute time synchronization.

For the synchronization to the absolute time it will also be necessary to perform synchronization and syntonization. In the actual implementation of PLUS-TimeSync, the same resources used for performing synchronization and syntonization over the MV-BPL network (as described in the next section) are used for performing those processes with the absolute time source. Typically GPS or atomic clock devices will provide two interfaces for providing their time-base. On one interface the absolute time will be providing in the form of a standardized time base, e.g. UTC. Typically this is provided on a serial interface and can be used by the mater modem to set the clock counter. A translation will be required between the time-base used by the absolute time device and the PLUS-TimeSync time-base. Also here computational delay in the conversion and application of this time-base must be compensated. On the other interface a so-called 1PPS (one pulse per second) signal is provided which provides a reference for performing syntonization. The MV-BPL master modem must adjust its clock frequency to match that of the absolute time device.

3.4 Zone B: MV-BPL Time Synchronization

3.4.1 Time Synchronization Protocol for PLUS

Time synchronization within the MV-BPL network follows some of the basic principles of other network time synchronization protocols such as NTP or IEEE 1588. The basic protocol and algorithm can be broken down into the following functionality which will be described in the following sub-sections:

1. Timestamping of time synchronization packets at the transmitter and receiver
2. Reliable exchange of timestamps between network nodes
3. Estimation of the mean path delay
4. Synchronization and syntonization
5. Clock correction

3.4.2 Timestamping

One of the main features provided by highly precise network synchronization protocols such as IEEE 1588 is the use of timestamping of transmitted and received frames at the interface between the PHY and upper layers. The variance in the resulting timestamp is then dependent upon the accuracy of detecting a certain characteristic of the physical signal, e.g. start of frame or end-of-frame. In a dedicated data network this is not such a problem. However, in a BPL network this poses a more significant problem because of the signal distortion and signal echoes resulting from the transmission channel. This means that multiple time-delayed versions of the transmitted signal will appear at the receiver. Within the medium-voltage network with long transmission distances, these time-difference between echoes can be rather significant. The relatively high level and time-variant noise conditions on the BPL channel also make this difficult.

Therefore, an algorithm has been developed which can:

- Accurately detect a specific location in the received BPL frame even in the presence of significant impulsive noise.
- Differentiate between the direct received signals and the received signal echoes.

On the transmit side the detection of the end of the preamble is rather trivial. The frame synchronization algorithm within the existing PLUS solution provides a good basis for the accurate detection of the end of the preamble at the receiver. The actual point at which the timestamp should be made within the PHY Protocol Data Unit (PPDU) is shown in Figure 13. Frame synchronization uses the repetative synchronization mini-symbols within the preamble in order to accurately detect the exact point in time between the preamble and the Frame Control (FC) OFDM symbol. It is also very robust to differentiating between different echoes resulting from the channel.

It is important to note that due to the encoding performed by the MV-BPL transceiver for both error correction and error detection, it is infeasible to include the timestamp of the PPDU being transmitted within that PPDU. The time required for encoding would not be sufficient to include that information in real-time. Therefore, as will be described below the timestamp of the actual transmitted PPDU is always included in a follow-up PPDU.

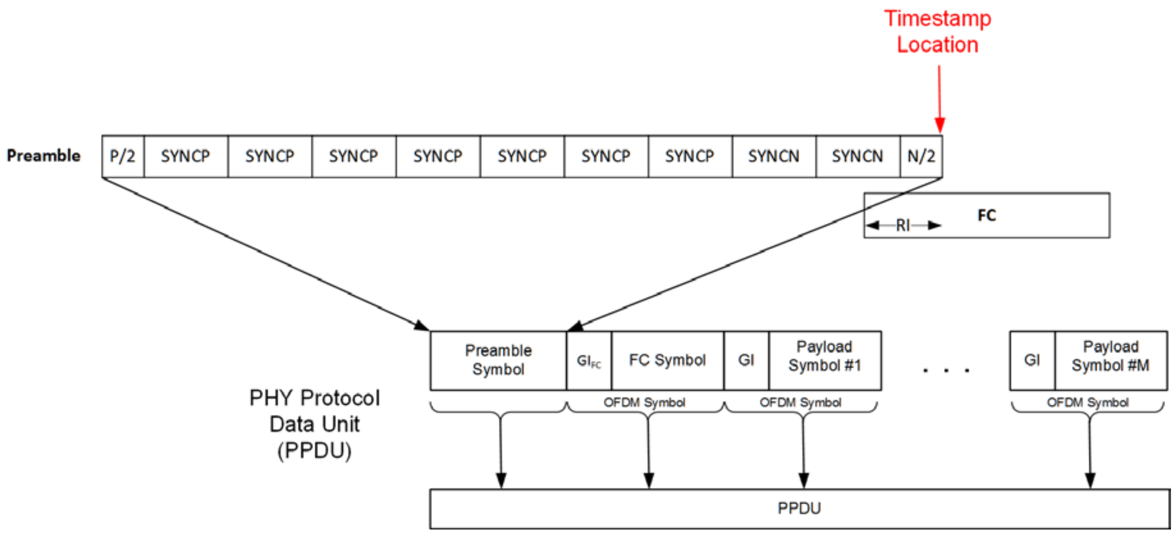


Figure 13: Timestamp location within the PPDU

3.4.3 Reliable Exchange of Timestamps

3.4.3.1 PLUS-TimeSync Time Synchronization Topology

Time synchronization within a MV-BPL cluster with PLUS-TimeSync follows a basic master-slave architecture. Within a MV-BPL cluster each node will form a multi-hop connection to the cluster master by selecting the best relay node along a path towards the master. In this way a tree topology is formed between all nodes in the cluster and the master acting as the root of the tree. Each node therefore connects either directly to the cluster master node or to a relay node along a branch to the master.

For time synchronization with PLUS-TimeSync the logical topology formed within a MV-BPL cluster is used in order to determine the master-slave relationship for time-synchronization. Therefore, the time synchronization master selection is not performed explicitly within the PLUS-TimeSync protocol, but is rather a function of the overlying MV-BPL protocol which is based on the IEEE 1901 standard. The MV-BPL cluster master acts as the time "grandmaster" for that cluster. It will synchronize its time to the absolute time as previously described in the description of Zone A. MV-BPL modems with a direct logical connection to the MV-BPL master can be considered to be 1-hop removed from the grandmaster (MV-BPL cluster master). However, these 1-hop MV-BPL modems can simultaneously serve as time-synchronization masters for other modems which are 2-hops away from the grandmaster. Those modems can then serve as time-synchronization masters for other modems which are 3-hops away and so forth. Thus each modem in the cluster can potentially serve as a time synchronization slave (connecting to a modem acting as a master further up the tree towards the root) and as a time synchronization master (connecting to modems acting as their master further down the tree away from the root).

However, the time synchronization itself is always only performed between master and slave(s). The direct message exchange also only occurs between master and slave(s). This architecture provides a more reliable (error resiliant) and scalable solution. If a modem should ever lose the connection to its time-synchronization master it will still maintain synchronization in "free-running" mode. Therefore, modems further down the tree would still remain synchronized. Once the connection to the master would be resumed then a re-synchronization would occur. In this way all the modems within the network which still maintain connectivity to each other, can synchronize even if problems within a specific area of the network would occur. This is also true for the MV-BPL master and the synchronization to the absolute time. If that synchronization would be lost, then the MV-BPL master would be in free running mode, but still be able to provide synchronization for the remaining modems.

3.4.3.2 Time Epoch

As mentioned in the previous section, a single modem can thus participate in two time-synchronization domains. One acting as a slave where the master dictates the time and one acting as a master where the modem dictates the time to its slaves. A synchronization is required between those two domains. The synchronization is guaranteed in that only a single clock is used for both domains. This, however, leads to the problem that a change in time due to a new synchronization to the master leads to an invalidation of any timestamps within the other domain. Otherwise synchronization and syntonization calculations with timestamps from two different time references would lead to incorrect results.

In order to ensure this synchronization the concept of an epoch has been introduced. The meaning of epoch here is taken as a particular time interval in which a modem is synchronized to its master or in which a synchronization remains valid. Applying a new time offset as a result of a new synchronization leads to a new epoch. Epochs are counted through the use of an epoch counter which is distributed with all timestamps. Therefore, all slaves know the epoch of their master and can easily determine when that epoch has been changed. A change in the epoch will lead to the invalidation of any existing/stored timestamps. This ensures that any time changes performed as a result of synchronization within the MV-BPL cluster do not lead to a cascade effect in terms of a loss of synchronization.

3.4.3.3 PLUS-TimeSync Messaging

In order to perform synchronization it is necessary to distribute timestamps between modems in the network. This requires a message exchange. The required messages are described within this section. An example sequence for a message exchange between the grandmaster and a slave is shown in Figure 14. The basic message exchange consists of the following messages and fields:

- SYNC Message: The SYNC message is sent periodically (with a typical interval being 1 second) from all modems. It always includes the timestamp from the previous SYNC message (see above in the timestamp section for the reasoning behind this).
    - SYNC_SEQ_NUM: The sequence number field. The value of this field simply counts up for every SYNC message transmitted. This field allows the receiver to determine the exact message with which the SYNC_PREV_TS field is associated. It is necessary as the harsh MV-BPL channel can lead to messages being lost.
    - SYNC_PREV_TS_VALID_FLAG: This field indicates if the SYNC_PREV_TS field contains a valid timestamp or not. Under certain conditions a timestamp would not be included in the SYNC message, e.g. during initialization.
    - SYNC_PREV_TS: The previous timestamp field. This contains the timestamp which was made during the transmission of the previous SYNC message.
    - REQ_SYNC_RESP: With this field, a SYNC_RESP message to be generated by the receiver can be requested.
- SYNC_RESP Message: The SYNC_RESP message is used in order to send the timestamp recorded during the reception of a SYNC message back to the transmitter of that SYNC message. It is requested during a new synchronization or during periodic updating of the mean path delay.
    - RESP_SEQ_NUM: The sequence number of the SYNC message for which the timestamp in RESP_TS was generated.
    - RESP_TS: The timestamp which was recorded during the reception of the most recent SYNC message of the modem requesting the SYNC_RESP.
- ANNOUNCE: In addition, an ANNOUNCE message has been defined which is periodically sent by all modems, but at a longer interval than the SYNC message. The ANNOUNCE message is used for the modems to exchange information such as the supported protocol version, whether or not they have an attached absolute time source, the accuracy of that time source, etc. The exact fields of this message are not described here.

Of course the transmission of these messages between MV-BPL modems leads to overhead in the network which reduces the available bandwidth for the actual application traffic. Although, without this overhead traffic, the important time synchronization feature could not be provided. As with many networking protocols there is an important tradeoff between functionality, the protocol overhead and performance. The design of the PLUS-TimeSync protocol has taken into consideration that an IEEE 1901 network requires that all modems in the network periodically send so-called beacon messages.

Although the period of such messages is not explicitly defined in the standard, a typical value is that beacon messages are sent every second. Therefore, PLUS-TimeSync messages have been designed to be sent within these beacon messages and the protocol has been designed such that a sufficient performance can be achieved even when sending messags at most once per second. The messages are integrated into beacon entry (BENTRY) messages. Each beacon can include multiple BENTRY messages. As a beacon must typically include at least 512 bytes of information, the additional information required for the PLUS-TimeSync messages can be integrated without leading to additional network overhead.

3.4.3.4 Synchronization

For performing synchronization an estimation of the mean path delay must be performed. For this estimation four different timestamps are required. In the example message sequence shown in Figure 14 TS1, TS2, TS3 and TS4 would be required at the slave modem. Note that TS1 is actually provided in the SYNC message sent at TS5. Furthermore, TS3 is provided in the SYNC_RESP message sent at TS5. Therefore, it is not until TS8 that the slave modem can compute the time offset. Until that time TS2 and TS4 must be stored and then associated correctly with TS1 and TS3 based on the sequence numbers once they are received.

Once all the information is available synchronization can be performed by calculating the time offset according to the formulas provided here.

First, the mean path delay must be calculated. Here we make the assumption that the delay is symmetric. This assumption is valid due to the fact that the timestamping is performed within the physical layer. This means that the main contributor to the path delay will be the propagation delay which will be symmetric due to the physics of signal propagation. The calculation of the first expression may not be apparent as it results in the difference of timestamps made on two different unsynchronized clocks. However, rearranging that expression leads to two differences with timestamp values in the same clock domain. Dividing by 2 takes the average of the forward and reverse delay as the mean delay as the delays can be considered to be symmetric.

$$meanPathDelay = \frac{(TS4 - TS1) + (TS3 - TS2)}{2} = \frac{(TS4 - TS2) + (TS3 - TS1)}{2}$$

The time offset can then be calculated as the difference between the grandmaster time and the slave time while taking into consideration the path delay value previously calculated.

$$timeOffset = TS1 - TS4 + meanPathDelay$$

This time offset should then be applied to the clock which will generate a new epoch.

3.4.3.5 Syntonization

Syntonization is somewhat easier to calculate as it only requires knowledge of the ratio of the clock difference over unit time between the grandmaster and the slave. Therefore, the slave requires no feedback of the reception timstamp of its SYNC messages from the grandmaster, i.e. SYNC_RESP messages are not required for syntonization. Given the message sequence shown in Figure 14, the frequency correction that must be applied to the clock at the slave in order to syntonize to the master can be calculated according to the following formula:

$$driftRateCorrection = \frac{(TS8 - TS4)}{(TS5 - TS1)}$$

This drift rate correction would then need to apply to the clock oscillator. However, extensive simulation has shown that applying this value directly leads to system instability. Therefore, the new drift rate correction factor is applied to the clock based on a weighted average filter between the new value and the old correction value.

3.4.3.6 Further Notes

Here are some further notes to the operation of the PLUS-TimeSync protocol

– It has been found that synchronization should be applied before syntonization. After this time, fine tuning of syntonization can be performed with every newly received SYNC message.

– A periodic check of synchronization (including an evaluation of the mean path delay) is performed in order to determine if the time difference has gone over a configurable threshold. If this is the case, then a new synchronization is triggered. Otherwise only syntonization will be performed as long as the time difference is within the threshold. This allows a larger network wide stability as the modems will remain within the same epoch for a longer period of time.

– When a slave detects that its master has changed epochs, then all stored timestamps are cleared and a new synchronization is triggered. This ensures that potential large jumps in timestamp values coming from the master will lead to strange behaviour.

– During a new synchronization, the previous drift rate offset is still applied to the clock. This has been shown to provide more stable behaviour.

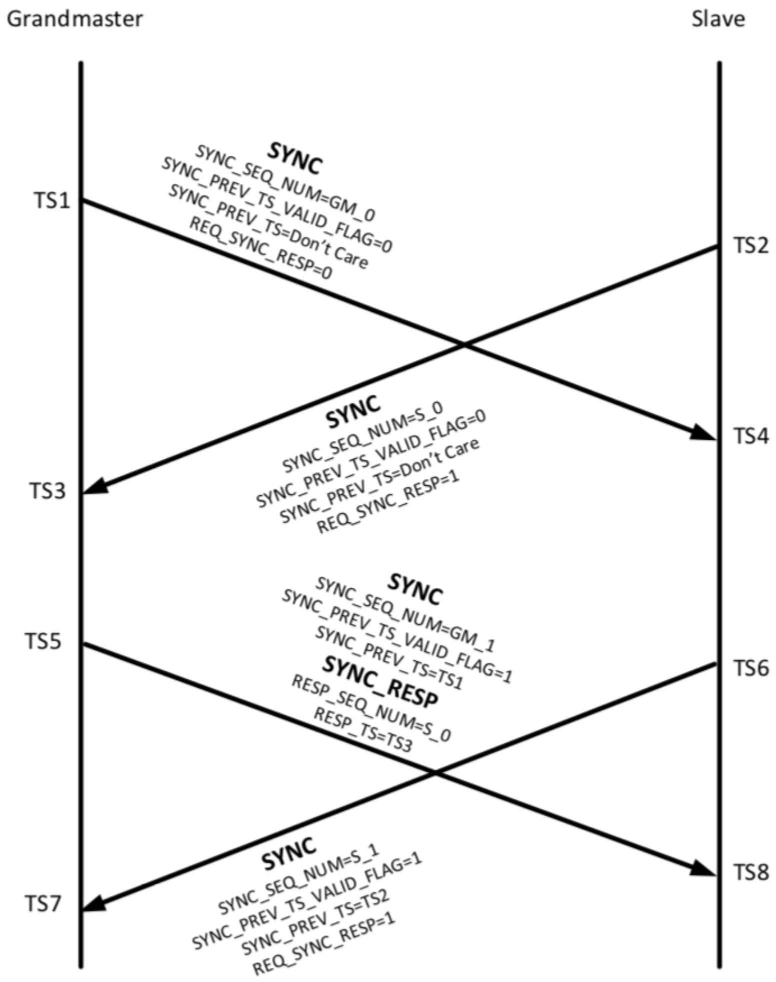


Figure 14: PLUS-TimeSync example message exchange

3.5 Zone C: Internal Clock Synchronization

In addition to a remote time synchronization with PLUS-TimeSync, each MV-BPL modem has a number of different time domains locally which must be synchronized:

1. Synchronization to the absolute time with GPS and/or atomic clock (only at the grandmaster/MV-BPL master)
2. “Upstream” synchronization over PLUS-TimeSync to another master (not present at the grandmaster/MV-BPL master)
3. “Downstream” synchronization over PLUS-TimeSync to one or more slaves
4. Synchronization to end devices attached to the modem through a 1PPS serial interface

It is only for processes 1 and 2 that re-synchronization or a change in the time will occur as those are the cases for which a modem will synchronize to another source. For processes 3 and 4 the modem acts as the source providing the time to other devices. Furthermore, only one of either process 1 or 2 will be active on any single modem at a given time. This is due to the fact that process 1 is only active on the MV-BPL cluster master while process 2 is inactive. For all other modems process 1 will be inactive and process 2 will be active. Therefore, this design limits competing processes which would change the time to only a single source.

However, we are still left with the challenge of maintaining synchronization between the different time domains associated with those processes. This is achieved by having each modem maintain a single clock which is then shared by all processes. In this manner, a perfect synchronization can be achieved.

One potential solution for implementing the clock would be to use a controllable oscillator such as a voltage controlled oscillator and a simple counter. The oscillator frequency could then be adjusted as part of syntonization. This solution has the disadvantage that its accuracy is dependent upon the underlying hardware and the precision can also be influenced by environmental conditions. For this reason an alternative approach has been followed in which the complete clock is implemented in digital hardware.

The general architecture of the single clock is shown in Figure 15. The clock is driven by a 100 MHz XTAL. The clock counter actually consists of two counters. An 80-bit free running nanosecond counter and a 30-bit fractional nanoseconds counter. For synchronization, the time offset is applied to a signed 80-bit offset register which is added to the free running nanoseconds counter. The time offset can be calculated as mentioned in the previous section. As the offset is calculated directly in nanoseconds no further conversion is required. For syntonization, a 30-bit signed drift rate correction factor is summed with the fractional nanoseconds counter. Negative or positive overflows/underflows are then added to the free running counter. In other words at each clock cycle of the 100 MHz oscillator a nominal value of 10 ns will be added to the free running nanosecond counter. With the drift rate correction factor the value added may be 9 or 10 ns at periodic intervals based on the drift rate. This allows a very accurate adjustment of the nanosecond counter with fractional nanosecond values at a very high resolution. A correction with a resolution of 9.31E-5 ppm is possible. However, a conversion from the drift rate correction which will be a fractional number between -1 and +1 must be converted to the correspoding drift rate correction factor to be applied.

The overall synchronized time is thus always present in an 80-bit nanosecond format. This format is then converted as required to several different formats as timestamps are made from the clock:

– PLUS-TimeSync timestamp with 48-bit seconds and 30-bit nanoseconds fields

– 1 pulse per second signal

– UTC time and data fields

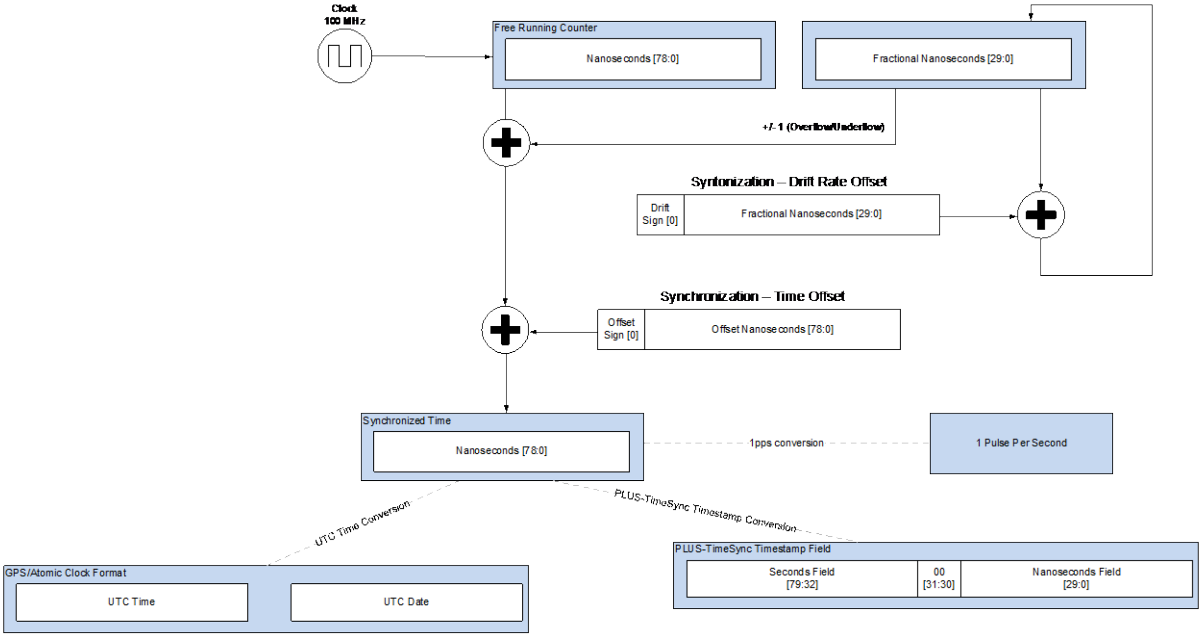


Figure 15: Fractional counter and timestamp format conversion

3.6 Zone D: Synchronization with End Devices

As the goal is to provide time synchronization to the application end devices, it is not enough to provide an accurate time synchronization within the MV-BPL modems as has been described until this point. That time synchronization must be extended to the end devices. Two potential solutions have been investigated in this project:

– **IEEE 1588** [5]: IEEE 1588 can potentially provide the necessary accuracy. This would mean that end devices would be attached to the MV-BPL modem over an Ethernet LAN and the IEEE 1588 Precision Time Protocol (PTP) would be used to synchronize the time. The MV-BPL modem will always act as the IEEE 1588 master for all attached application devices which act as IEEE 1588 slaves.

– **1PPS Interface**: Here, the absolute time is provided over a serial interface together with a 1PPS signal for accurate synchronization and syntonization.

Regarding the first solution, a key component in providing high accuracy with IEEE 1588 is hardware supported time stamping. Fortunately, this feature is supported directly by Xilinx Zynq which is the target platform for the PLUS BPL technology. The architecture of the current MV-BPL modem implementation based on PLUS is shown in Figure 16. Xilinx Zynq consists of a Processing System (PS) which contains the dual core ARM processor as well as a number of communications interface controllers. One of these controllers is the Gigabit Ethernet Controller (GEM). The typical use-case is that the Timestamp Unit (TSU) in the GEM manages the timestamping for IEEE 1588 and is controlled by the Ethernet driver running under Linux. The Zynq reference manual references potential inaccuracies with performing timestamping in PS due to the non-deterministic delay in software controlled timestamping [2]. This has been also reported in other references [1]. An alternative is to implement the TSU in Programmable Logic (PL) in VHDL. The necessary signals for generating timestamps can be re-rerouted to PL through the EMIO interface. Timestamps are generated and stored in PL until they can be read by the Ethernet driver. The signaling over EMIO is direct and therefore suffers from very little delay and, more importantly variation in the delay (jitter). The reading of the timestamps is a non-real time operation so any delays or jitter is non-critical. An investigation was performed in this project in which the accuracy of a software controlled timestamping process with the TSU in the GEM was compared to the realization of a TSU in PL. It was found that a TSU in PL is the only means to provide a true sub-microsecond accuracy for this timestamping. The MV-BPL modem architecture with the TSU in PL is shown in Figure 16. The IEEE 1588 software driver running under Linux is provided by the The Linux PTP Project. Unfortunately, the adaptations to the Linux driver in order to support the TSU in PL proved very challenging to implement. Changes were required not only within the IEEE 1588 driver, but also within the Ethernet driver as well. Furthermore, debugging problems with the adaptations proved difficult as enabling log output led to timing problems which influenced the functionality of the driver.

In the end, an implemention using IEEE 1588 as the interface to end devices has several disadvantages:

– The IEEE 1588 protocol requires a full network protocol stack and IEEE 1588 hardware and software driver support. In other words, there is a significant overhead and complexity required not only within the MV-BPL modem, but also within the end devices.

– The accuracy of the solution is dependent upon the characteristics of the LAN within the secondary substation. If switches would be used between the MV-BPL modem and end devices, then these switches would also need to support IEEE 1588.

– The developed solution with timestamping performed in PL and the necessary driver adaptations would mean that it would only work on the Xilinx Zynq platform with the selected driver. If future MV-BPL modem products would use a different platform, then significant adaptations to the concept would be required.

The alternative approach which has been implemented is to provide the time synchronization with a 1PPS signal. A similar approach is provided by GPS receivers. As this solution is supported by most GPS receivers it can almost be considered as a de-facto standard and is supported by most end devices. With the 1PPS interface a pulse is generated every second for providing accurate synchronization and syntonization. Furthermore the absolute time is transferred serially using a standardized format such as a NMEA sentence. This solution has been selected as has been implemented as shown in Figure 16. The challenge here was to convert the running *Fractional Counter* to the necessary format for generating the 1PPS signal. This was achieved within the *1PPS Generator* block. Any delays within the conversion and generation of this signal has also been compensated in order to ensure that the 1PPS signal reflects the time of the *Fractional Counter*.

In the end the difficulties with the IEEE 1588 driver led to the fact that the IEEE 1588-based solution could not provide the necessary accuracy. Those issues combined with the disadvantages previously mentioned led to the fact that the 1PPS interface is the preferred interface to any end devices. The 1PPS interface has therefore been selected for the final PLUS-TimeSync solution.

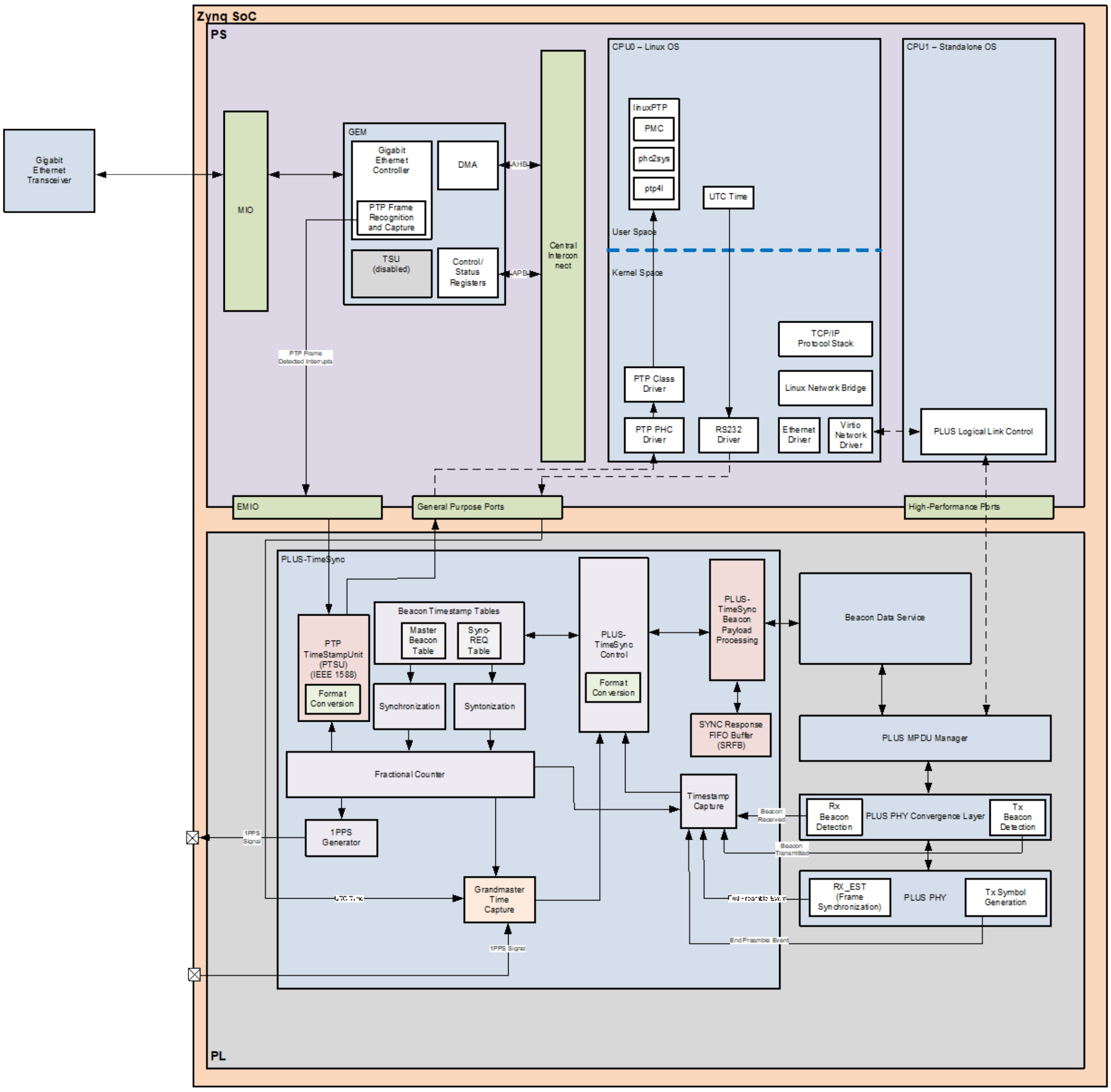


Figure 16: PLUS-TimeSync modem hardware architecture

3.7 PLUS-TimeSync Prototypes

The PLUS-TimeSync solution has been realized on a series of three PLUS prototypes. The prototypes are the first generation prototypes in which the hardware is based on development kits provided by Xilinx and other vendors. For this reason the prototypes are rather large, however the full functionality is provided. Figure 17 shows an image of one of the prototypes. As the focus of this project was on the development of digital hardware as well as some software, only modifications to the firmware running on the prototypes were made. No modifications to the prototype hardware were necessary.

Figure 17: PLUS BPL prototype

4 Laboratory Testing

4.1 Test Setup

Field testing of MV-BPL solutions is rather expensive due to the high costs of equipment installation within the SSs. Safety requlations usually require that the MV-BPL coupler be installed when no voltage is present on the MV line. Therefore, there is a significant planning effort required in order to ensure that no network outages occur. Installation must also be performed by trained professionals. For this reason the testing of the PLUS-TimeSync solution has occured within a laboratory environment within this project. The overall MTC-MV-BPL solution to be developed in the follow-on project will be tested within a real MV environment.

Nevertheless, HSLU posseses a BPL test environment which can be highly representative of the true MV environment. Extensive models for the transmission channel both on underground cables as well as overhead wires have been developed in previous Swiss CTI projects based on measurements in real MV environments [6]. These models are not only reproduced in the simulation environments previously described, but can also be reproduced to a certain extent in the laboratory environment using channel emulators.

The test setup used for testing the PLUS-TimeSync solution is shown in Figure 18. It consists of a cluster of three MV-BPL modems. PLC Modem A acts as the cluster master. PLC Modem B connects directly to the cluster master, i.e. PLC Modem A. PLC Modem C connects to PLC Modem B. Therefore, PLC Modem B acts as a relay modem between A and C. In other words, a connection over two hops in the network can be tested. The BPL channel emulator is able to reproduce attenuation and noise conditions which are representative of a MV-BPL network. Each modem is connected over an Ethernet LAN to a test laptop which is responsible for reading out status information from the modems in order to verify the BPL functionality and performance.

In the indoor lab environment, a reliable GPS signal is not available. Therefore, the GPS clock or the absolute time is emulated by a simple function generator which is used to output a 1PPS signal. This signal is split and additionally input to the oscilloscope for comparing the time at the modems to the absolute time.

Finally, the end-to-end synchronization to the application devices must be tested. For time synchronization performance, it is critical that the resulting time for all available devices is measured relative to each other with a single reference time. The output reference time from each modem provided to the end devices through the 1PPS signal is used for measurement purposes. Within the test setup this time reference from all three modems is input to an oscilloscope such that any differences can be accurately measured.

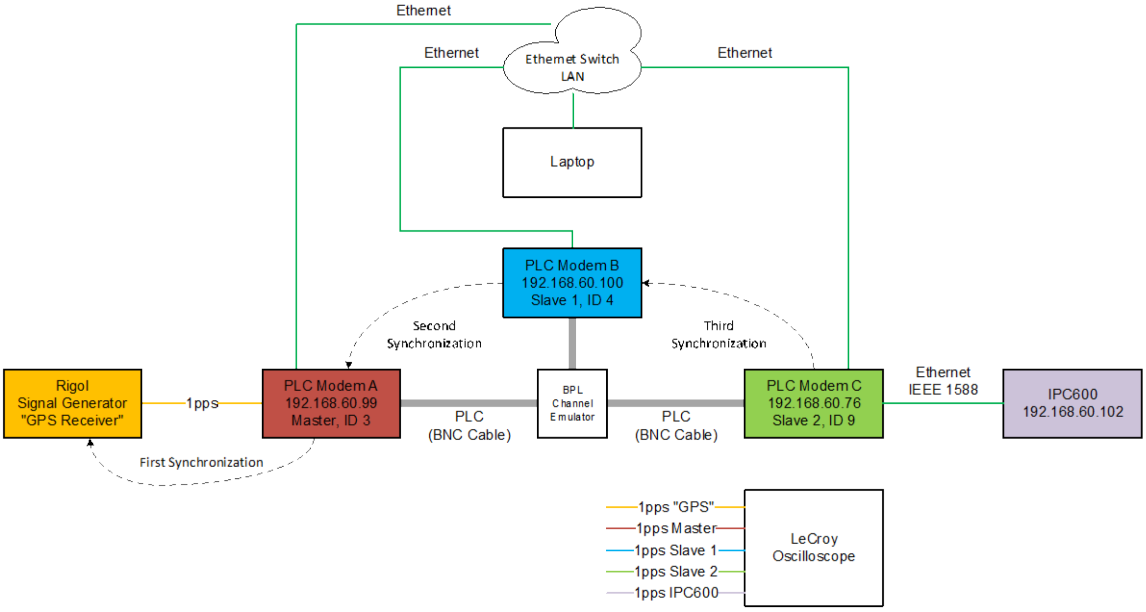


Figure 18: PLUS-TimeSync laboratory test setup architecture

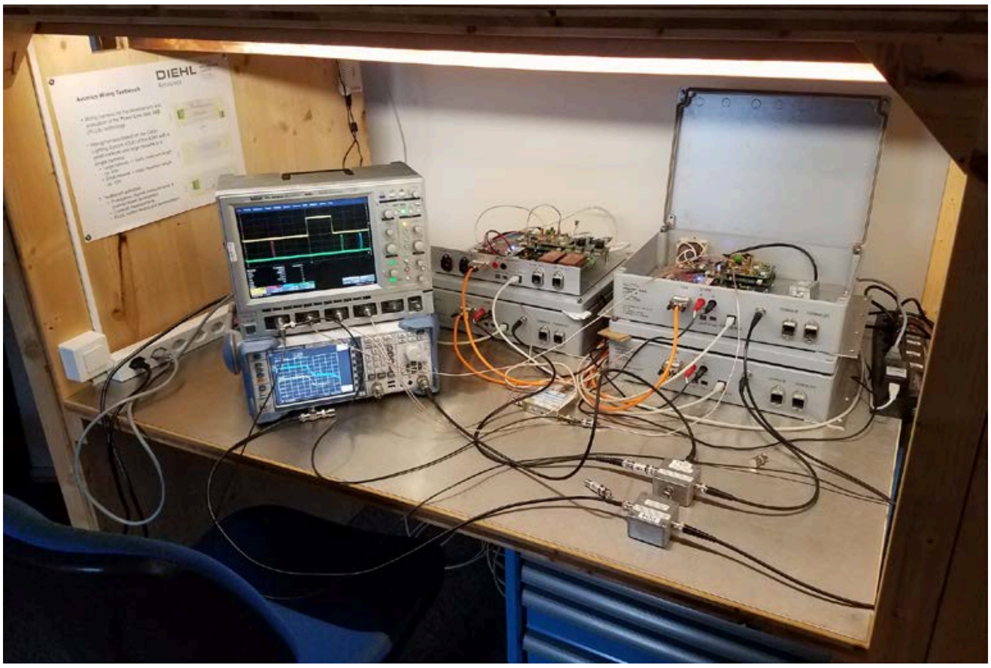


Figure 19: PLUS-TimeSync laboratory test setup

4.2 Test Results

A test procedure has been defined for verifying the synchronization using the test setup described in the previous section. Note that this only verifies the synchronization to all modems. The synchronization to the end-device is verified in the next section.

The following images show one execution of the test procedure and the measured results. The signals within the following imsages are:

- Yellow: 1PPS signal from "external GPS-receiver", emulated by function generator which will be used as the reference time.
- Red: 1PPS signal from master-modem, PLC Modem A.
- Blue: 1PPS signal from 1st slave modem, PLC Modem B, which synchronizes to master modem.
- Green: 1PPS signal from 2nd slave modem, PLC Modem C, which synchronizes to 1st slave modem.

The test procedure is the following:

1) Figure 20: All modems are started, however the PLUS-TimeSync protocol is disabled so that no time synchronization is being performed. This case is used to show that the 1PPS signal generated by all modems in not synchronized to the reference time (yellow). In the normal case the PLUS-TimeSync protocol would be enabled upon power-up of the modems so that synchronization would begin immediately.
2) Figure 21: The PLUS-TimeSync protocol of the master modem, PLC Modem A, is enabled. The master modem, red line, therefore synchronizes to the reference time signal (yellow line).

3) Figure 22: The PLUS-TimeSync protocol of the 1st slave modem, PLC Modem B, has been enabled. The 1st slave modem (blue line) therefore synchronizes to the master modem.
4) Figure 23: The PLUS-TimeSync protocol of the 2nd slave modem, PLC Modem C, has been enabled. The 2nd slave modem (green line) therefore synchronizes to the 2nd slave modem. Now all modems are synchronized.
5) Figure 24: This is a zoomed in view of the result of the previous step. Here the x-axis shows a time resolution of 200ns/division. As can be seen all the modems are within ± 200ns of the reference time.

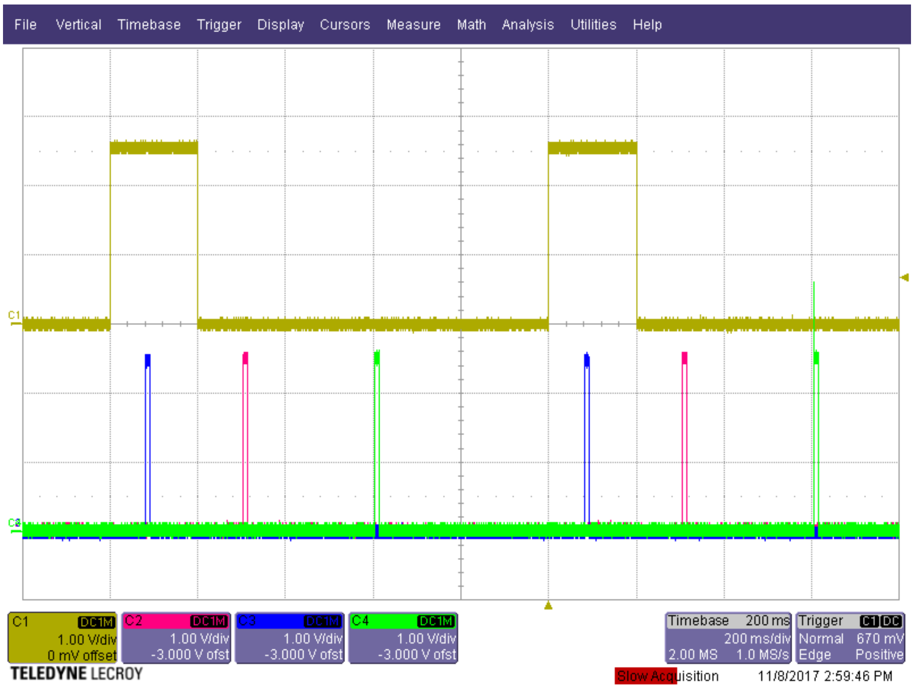


Figure 20

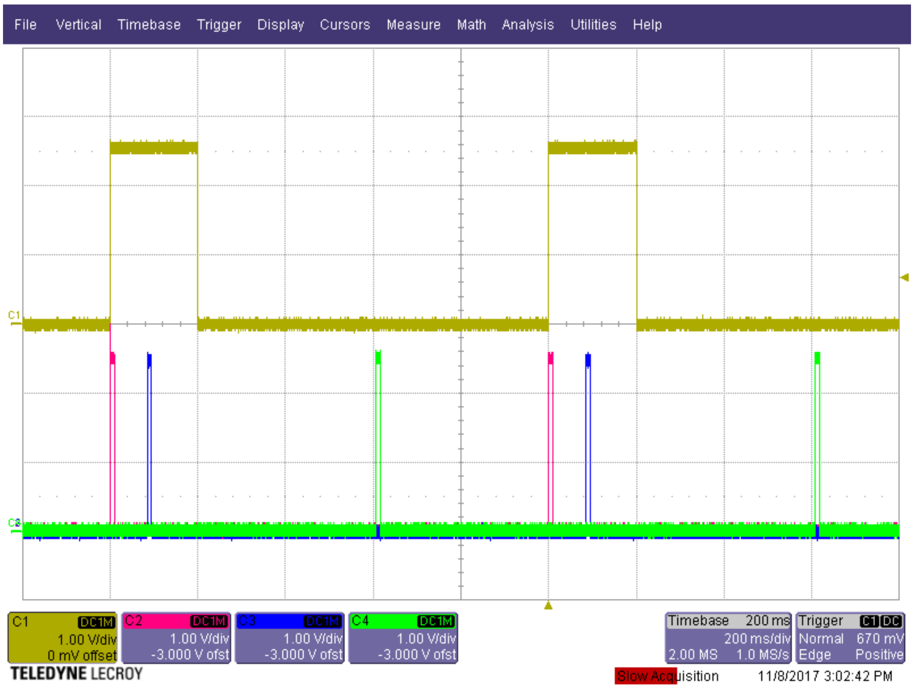


Figure 21

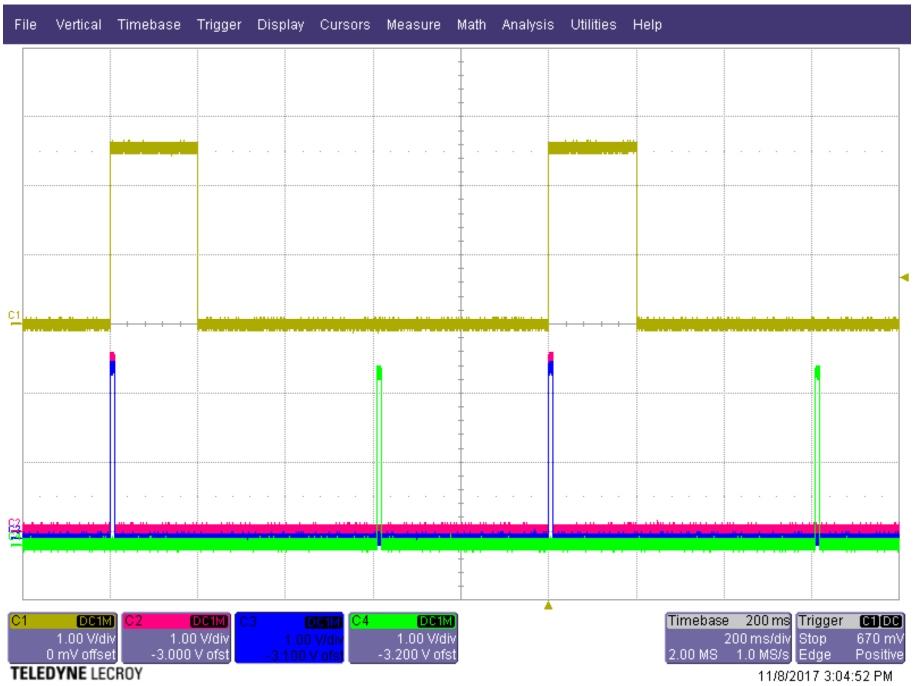


Figure 22

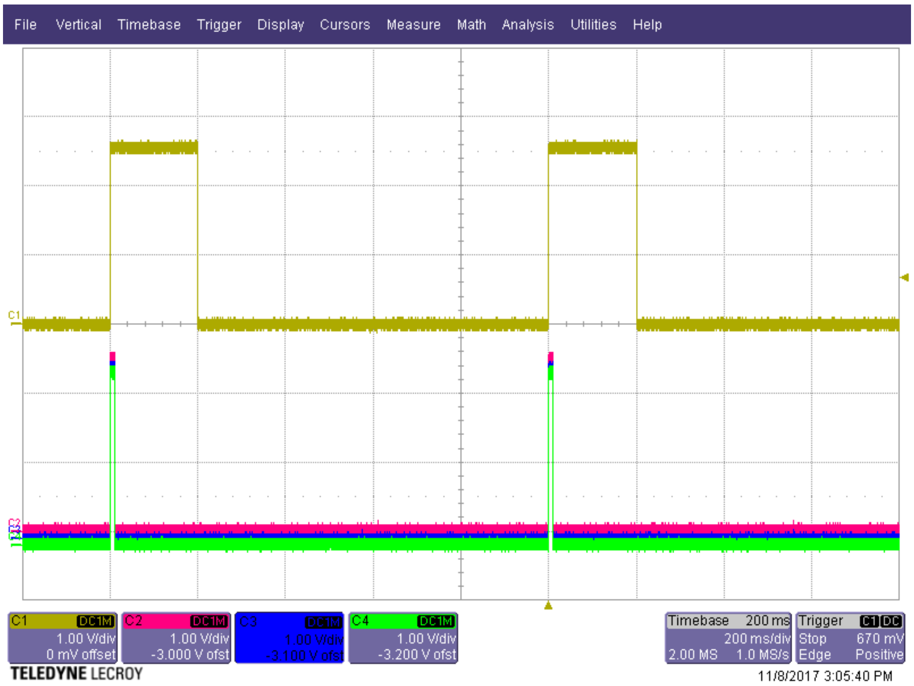


Figure 23

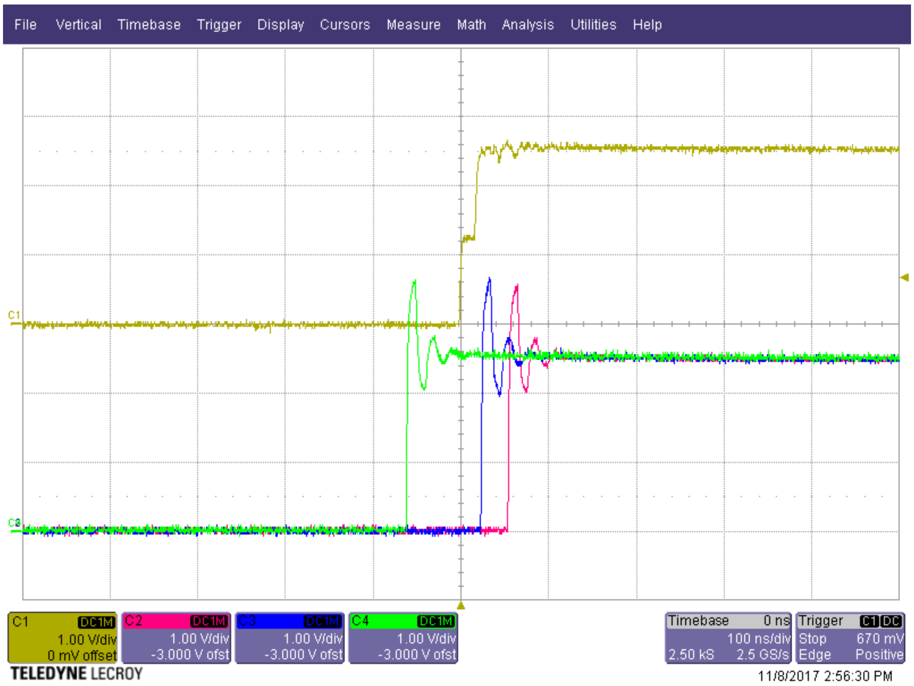


Figure 24

Of course the previously described test case was just a single test run of the functionality and performance of the PLUS-TimeSync protocol. For all tests the time synchronization was verified with the 1PPS signals at the oscilliscope. The persistance feature on the oscilliscope was enabled such that the worst case differences over a long period of time could be measured. With this type of measurement a the 1PPS output signal from the 2nd slave remains on the display. An example of such a measurement is shown in Figure 25. All of the dark green plots show the 1PPS output from the 2nd slave over a long measurement duration.

Several different test cases were performed as described here:

– Time to synchronization: It is known that in order to achieve initial synchronization a slave must receive at least two SYNC messages from its master where the second message includes the SYNC_RESP, i.e. after the slave begins requesting a SYNC_RESP. After this time, the syntonization will begin for which a further two SYNC messages are required. Therefore, in the best case the complete synchronization will require four message intervals, however depending upon the timing of the masters SYNC message transmissions compared to the slaves timing could require 8 message intervals in the worst case. Therefore, the time to synchronization scales linearly with the configured transmission interval. This has been verified through tests with different transmission intervals and measuring the time between enabling the PLUS-TimeSync and the first synchronization was achieved.

– Different channel conditions: several different channel conditions have been evaluated in the test setup. The overall result has shown that the packet loss is the main influencing factor on the performance of the time synchronization. This is due to the fact that the timestamping is dependent upon the frame synchronization algorithm. If frame synchronization is found, then a timestamp will be made and then typically the packet can be successfully decoded. If frame synchronization is not found, then no timestamp will be made and also the packet cannot be successfully decoded. Therefore, if very little packet loss is occurring (<3%) then it has been observed that synchronization can be maintained. If high packet loss is occurring, then the maintained synchronization depends upon the stability or drift rate of the local oscillator as the clock will drift until synchronization can be resumed. However, with BPL due to the turbo coding algorithms, it is known that the channel condition range between a low packet loss rate and no possible communications is very small. Therefore, the conclusion from these tests is that the time synchronization can remain stable as long as the channel conditions are such that communications is possible with a relatively low loss rate (<3%).

– Environmental variations and its influence on the performance has also been tested. This was done by spraying the XTAL on the modems with a coolant spray. This served the purpose of creating a dramatic change in the XTAL frequency. It was verified that for all cases the synchronization was able to be maintained even with these drastic changes. In the extreme cases a new syntonization could not stabilize the overall synchronization. However, the synchronization monitoring was able to detect this and a new synchronization corrected the problem.

Overall with a high confidence level we can say that an accuracy of ± 0.5 μs can be achieved over a network with two-hops in a laboratory environment, but with realistic MV channel conditions.

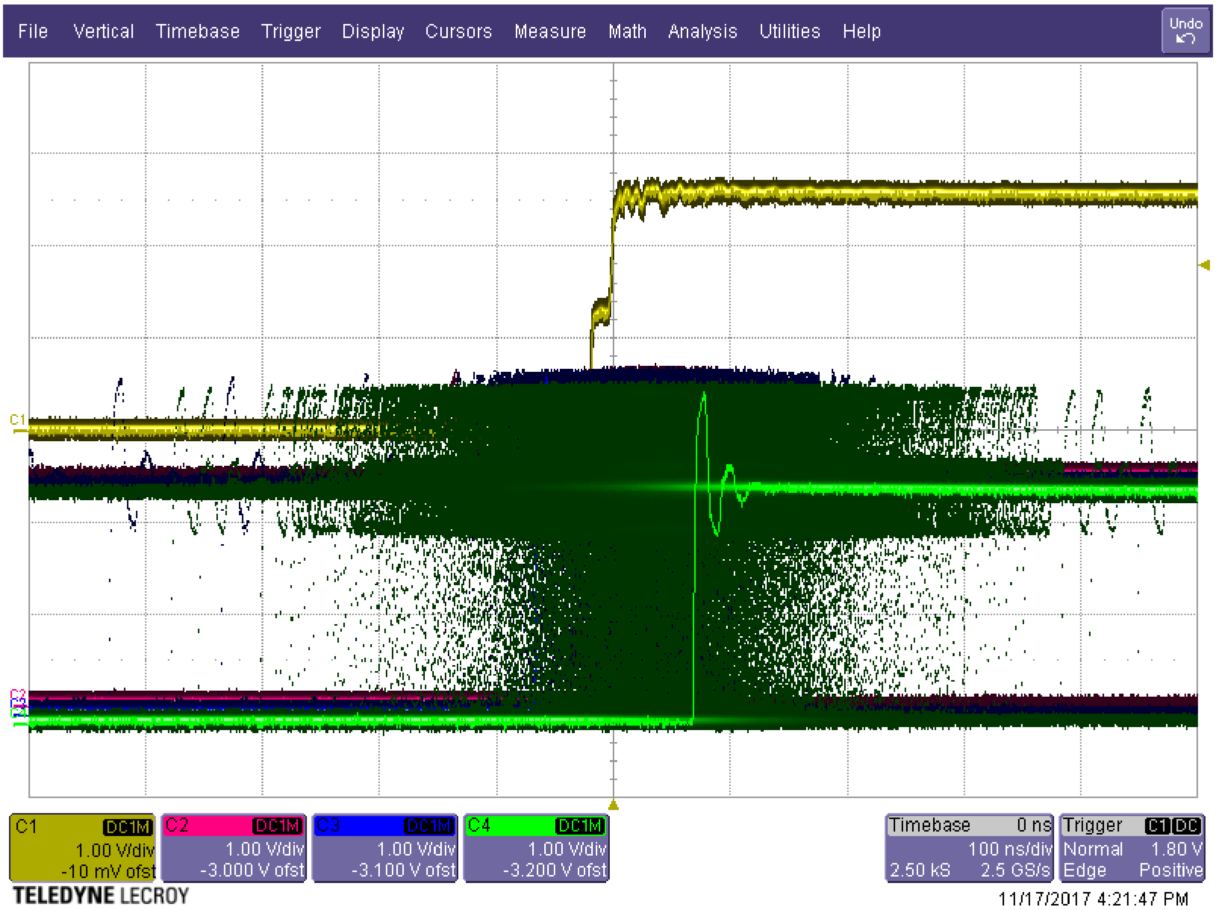


Figure 25: Long term measurement of the time synchronization performance

5 Conclusion and Next Steps

Worldwide increasing pressure is being placed on the electric grids and in particular the MV grids due to the steadily increasing distributed energy resources ratio. The highly time-dynamic character of such power fed into the grid by a vast amount of spatially distributed sources combined with the decreasing ratio of stabilizing rotational mass leads to substantial challenges for the future grids to keep them robust enough for the requirements and expectations of the consumers. Grids must be able to accommodate new energy flow patterns in a considerably more dynamic environment. Therefore, protection and automation systems are quickly gaining importance not only for the transmission grid but increasingly also for the distribution grid levels. The deployment of powerful concepts in the distribution grids like phasor measurement units measuring synchrophasors and line differential protection appears as a promising approach to this problem. However, the communication requirements of such applications (high availability, low latency) raise a significant challenge to the communication infrastructure as a cost efficient solution must be provided. The use of the MV-BPL technology provides an interesting approach as it provides a cost efficient solution in which the existing electrical grid infrastructure is used also as the communications medium.

Within a larger umbrella project of which this project is part, a dedicated MV-BPL solution for mission- and time-critical applications is being developed. The first step in this development which has been covered within this project is to provide a robust and highly precise network time synchronization protocol over the MV-BPL network. An analysis of the application showed that it is necessary to provide a synchronization with an accuracy of ± 3.1μs in order to fullfill the most strict PMU requirements.

The basis of this development is the existing Power Line data bUS (PLUS) technology provided by HSLU. This technology has been extended to support network time synchronization. The TimeSynchronization for PLUS (PLUS-TimeSync) protocol has been developed. In a first step the protocol concept was developed using model based design and an event-based simulation platform. The feasibility of this concept has therefore been verified at an early stage in the development. In the next step the protocol was implemented with the majority of the implementation has been done in VHDL. The implementation has been integrated to the firmware within existing PLUS prototypes on the Xilinx Zynq SoC. Finally, extensive testing has been performed in a laboratory environment in order to verify the functionality and performance of the PLUS-TimeSync protocol. The test results have shown that the achieved performance well exceed the requirements. **A time synchronization accuracy of ± 0.5 μs over two-hops in a network could be achieved under wide-ranging test conditions.**

With these promising results this part of the umbrella project is now successfully completed. However, work now continues in a follow-on project also funded by BFE. In this follow-on project the full communications solution for a mission and time critical MV-BPL solution will be developed. The main focus of this work will be in developing a communications solution which meets the strict reliability and latency requirements. This complete solution will then be tested through field trials in a real MV environment.

References

[1] Moreira, Naiara, et al. "Nanosecond accuracy using SoC platforms." Precision Clock Synchronization for Measurement, Control, and Communication (ISPCS), 2014 IEEE International Symposium on. IEEE, 2014.

[2] Xilinx, "Zynq-7000 All Programmable SoC Technical Reference Manual", UG585 (v1.10) February 23, 2015.

[3] Sendin, Alberto, et al. "PLC deployment and architecture for Smart Grid applications in Iberdrola." *Power Line Communications and its Applications (ISPLC), 2014 18th IEEE International Symposium on*. IEEE, 2014.

[4] IEEE Standard for Broadband over Power Line Networks: Medium Access Control and Physical Layer Specifications," in IEEE Std 1901-2010 , vol., no., pp.1-1586, Dec. 30 2010.

[5] IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems," in IEEE Std 1588-2008 (Revision of IEEE Std 1588-2002) , vol., no., pp.1-300, July 24 2008.

[6] Marri, Vamsi Krishna, Stephen Dominiak, and Mikko Maurer. "Channel Modelling and Channel Selection for Broadband PLC on Medium Voltage Overhead and Underground Lines."

[7] Power System Relaying Committee. "IEEE Standards for Synchrophasor Measurements for Power Systems-IEEE Std C37. 118.1-2011." New York, USA (2011).

Abbreviations

Abbreviation	Meaning
1PPS	One Pulse Per Second
AMI	Automated Metering Infrastructure
BPL	Broadband Power Line Communications
DC	Data Concentrator
DER	Distributed Energy Resource
DSO	Distribution System Operators
FC	Frame Control
FO	Fiber Optic
FPGA	Field Programmable Gate Array
GEM	Gigabit Ethernet Controller (on Xilinx Zynq)
GI	Guard Interval
GMA	Grid Monitoring and Automation
GPS	Global Positioning System
HSLU	Lucerne University of Applied Sciences and Arts
HV	High Voltage
LAN	Local Area Network
LDP	Line Differential Protection
LV	Low Voltage
MBD	Model Based Design
MPDU	MAC (layer) Protocol Data Unit
MTC	Mission- and Time-Critical
MV	Medium Voltage
MV-BPL	BPL solution for use in MV electric grids
NB-PLC	Narrowband Power Line Communications
NTP	Network Time Protocol
OFDM	Orthogonal Frequency Division Multiplexing
PDC	Phasor Data Concentrator
PL	Programmable Logic
PLC	Power Line Communications
PLUS	Power Line data bUS
PLUS-TimeSync	Time Synchronization Protocol for PLUS
PMU	Phasor Measurement Unit
PPDU	Physical (layer) Protocol Data Unit
PPS	Pulse Per Second

PS	Primary Substation (HV/MV transformer station)
PTP	Precision Time Protocol (IEEE 1588)
SoC	System-on-Chip
SS	Secondary Substation (MV/LV transformer
TSU	Timestamp Unit
UTC	Universal Coordinated Time
VHDL	VHSIC Hardware Description Language
WAMPC	Wide Area Monitoring Protection and Control
WAN	Wide Area Network
WP	Work Package
XTAL	Crystal Oscillator