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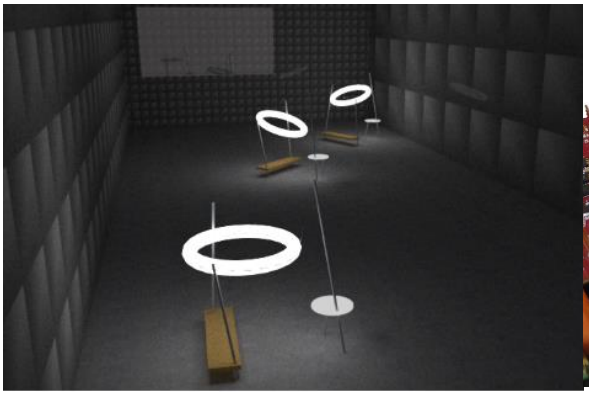
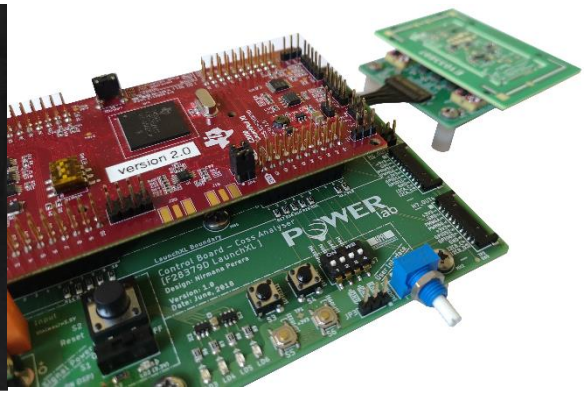
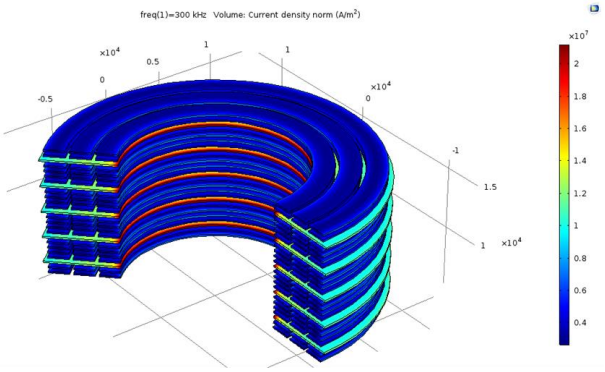
Energy Research

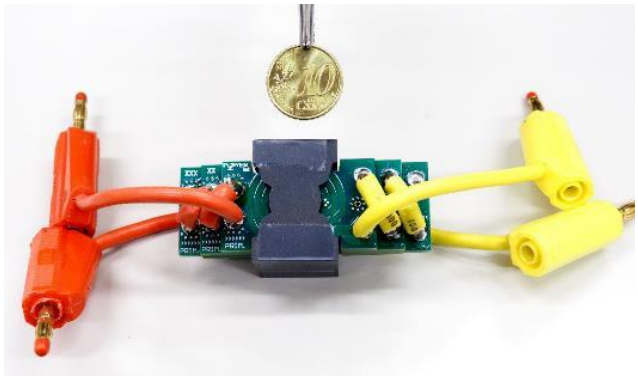
Final report 2019

GaN-based Power Electronics for Energy Efficiency Applications









Date: 30 March 2019

Place: Bern

Publisher:
Swiss Federal Office of Energy SFOE
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SFOE contract number:	SI/501266-01

Contents

Summary

The mission of this project was to investigate the increase in system efficiency in power conversion by utilizing the benefits of GaN semiconductor technology. The superior material properties of GaN such as high breakdown strength, high saturation velocity and high mobility (especially due to the presence of two-dimensional electron gas (2DEG) in its structure) allows to increase the efficiency and power density of power electronic converters compared to existing technologies. The first part of this project was dedicated to identify applications that offer large energy-saving potential by using GaN-technology, which were: autonomous LED street lighting and micro-inverters for photovoltaic applications. In addition to their large energy-savings potential, these applications serve as a platform to understand the full potential of GaN technologies for energy-efficiency.

Technical aspects of the project covered research all the way from the device-level to the converter-level, up to the system-level. In a device level, we propose a new method to analyze the intrinsic characteristics of Gallium Nitride power devices from a circuit designer's perspective to improve the design of integrated power electronics for high efficiency applications. Based on preliminary results, we found that, in order to best utilize GaN devices for integration and high efficiency, a much better understanding of their switching behavior is required. Moreover, we have identified the key device-level characteristics of GaN transistors to obtain the lowest losses at high frequency operation. This is extremely important as this directly affects the power density and integration capabilities of the converters. In the system level, various converter architectures were evaluated for harvesting maximum energy from PVs. Converter-level optimizations were performed on power circuits used in micro-converters and LED driver systems with the goal to achieve high efficiencies and power densities. We have identified what could be optimized from the device technology side and what needs to be improved from passive components. For example, the magnetic components at high frequencies are extremely complicated to design, which is leading to an extensive research in this area, as this plays a key role in system integration. Our results clearly show that GaN devices are capable of faster and higher speed operation compared to existing technologies, allowing much higher efficiency converters.

Résumé

La mission de ce projet était d'étudier l'augmentation de l'efficacité des systèmes de conversion d'énergie en utilisant les avantages de la technologie des semi-conducteurs GaN. Les propriétés supérieures du GaN, telles qu'une haute tension de blockage, une vitesse de saturation élevée et une grande mobilité (notamment grâce à la présence de gaz électronique bidimensionnel (2DEG) dans sa structure), permettent d'augmenter le rendement et la densité de puissance des convertisseurs électroniques de puissance par rapport aux technologies existantes. La première partie de ce projet a été consacrée à l'identification des applications qui offrent un grand potentiel d'économie d'énergie en utilisant la technologie GaN, à savoir : l'éclairage public autonome à LED et les micro-inverseurs pour applications photovoltaïques. En plus, ces applications servent de plate-forme pour comprendre tout le potentiel des technologies au GaN en matière d'efficacité énergétique.

Les aspects techniques du projet couvraient la recherche depuis le niveau du composant jusqu'au niveau du convertisseur, ainsi que le niveau du système. Au niveau des composants, nous proposons une nouvelle méthode d'analyse des caractéristiques intrinsèques des dispositifs de puissance au nitrure de gallium du point de vue du concepteur de circuits afin d'améliorer la conception de l'électronique de puissance intégrée pour les applications à haute efficacité. Sur la base des résultats préliminaires, nous avons constaté que, afin d'utiliser au mieux les dispositifs GaN pour l'intégration et la haute efficacité, une bien meilleure compréhension de leur comportement de commutation est nécessaire. De plus, nous avons identifié les principales caractéristiques des transistors GaN au niveau de l'appareil afin d'obtenir les pertes les plus faibles en fonctionnement haute fréquence. Ceci est extrêmement important car cela affecte directement la densité de puissance et les capacités d'intégration des convertisseurs. Au niveau du système, diverses architectures de convertisseurs ont été évaluées pour obtenir l'énergie maximale des PV. Des optimisations au niveau du convertisseur ont été effectuées sur les circuits de puissance utilisés dans les microconvertisseurs et les drivers pour les lampes à LEDs dans le but d'obtenir des rendements et des densités de puissance élevés. Nous avons identifié ce qui pourrait être optimisé du point de vue de la technologie des dispositifs et ce qui doit être amélioré à partir des composants passifs. Par exemple, les composants magnétiques à hautes fréquences sont extrêmement complexes à concevoir, ce qui conduit à des recherches approfondies dans ce domaine, car ils jouent un rôle clé dans l'intégration des systèmes. Nos résultats montrent clairement que les dispositifs GaN sont capables d'un fonctionnement plus rapide et plus rapide que les technologies existantes, ce qui permet des convertisseurs beaucoup plus efficaces.

1. Project Goals

This project investigated the impact of GaN power electronic devices in energy efficiency applications such as drivers for LED light bulbs, micro-inverters for PV panels, power converters, etc. A study of the impact of such technology on these applications was performed and circuit demonstrators for the most promising applications were designed and built. The project guided for improvement of intrinsic device characteristics and benchmark the devices fabricated in our laboratory.

As concluded by the Swiss Federal Office of Energy (SFOE), the reduction of energy consumption by increasing energy efficiency would allow a significant proportion of Switzerland's energy requirements to be met through the use of renewable forms of energy in the future.

The outstanding electronic properties of Gallium Nitride (GaN) semiconductors (such as large breakdown voltage, high critical electric field, high electron mobility and saturation velocity, high frequency switching, high temperature operation) yield a much larger figure-of-merit (Baliga's figure-of-merit) compared to SiC and Silicon, making them an ideal material for power switches and converters. This will enable several applications for energy efficiency, such as drivers for LED light bulbs, inverters for photovoltaic panels, embedded power converters for computers and data centers, drivers for electric and hybrid automobiles, trains, ships, etc.

The final goals of this project were divided in the following way:

1. Investigate the following main questions
    - What applications would benefit the most from GaN technology?
    - What is the national and global energy-savings potential of GaN technology deployed in these different applications?
    - What are the intrinsic requirements for power devices and systems to address these applications?

2. Design and fabricate power devices in our laboratory that satisfy the requirements determined in the first part of the project. This step will be done in parallel to the design of circuit demonstrators to test and compare the devices fabricated in our laboratory to the current commercial state of the art devices (based on Silicon, SiC and also GaN). These circuits will serve as experimental platforms to benchmark the state of the art devices fabricated in our laboratory in terms of performance and energy savings. In this part of the project, we will:
    - Design and fabricate GaN-based power devices suiting the requirements determined previously.
    - Design and build circuit demonstrators to test and compare the devices fabricated in our laboratory to the commercially available devices.

These circuit demonstrators will yield insights on intrinsic characteristics of the devices that need to be better designed to yield circuit-level improved performance. Looking towards the future, we believe that in the long-term these devices and circuits could be the basic building blocks of efficient power electronic systems that will compose a future sustainable energy infrastructure in Switzerland.

2. Project Overview and Outcomes National Cooperation

There are two applications we have identified, which offer large energy-saving potential of GaN-technology: autonomous LED street lighting and micro-inverters for photovoltaic applications. In addition to their large energy-savings potential, these applications serve as a platform to understand the full potential of GaN technologies for energy-efficiency. In future phases, as follow ups for this project, we will expand our focus to other areas of high potential impact in energy-savings.

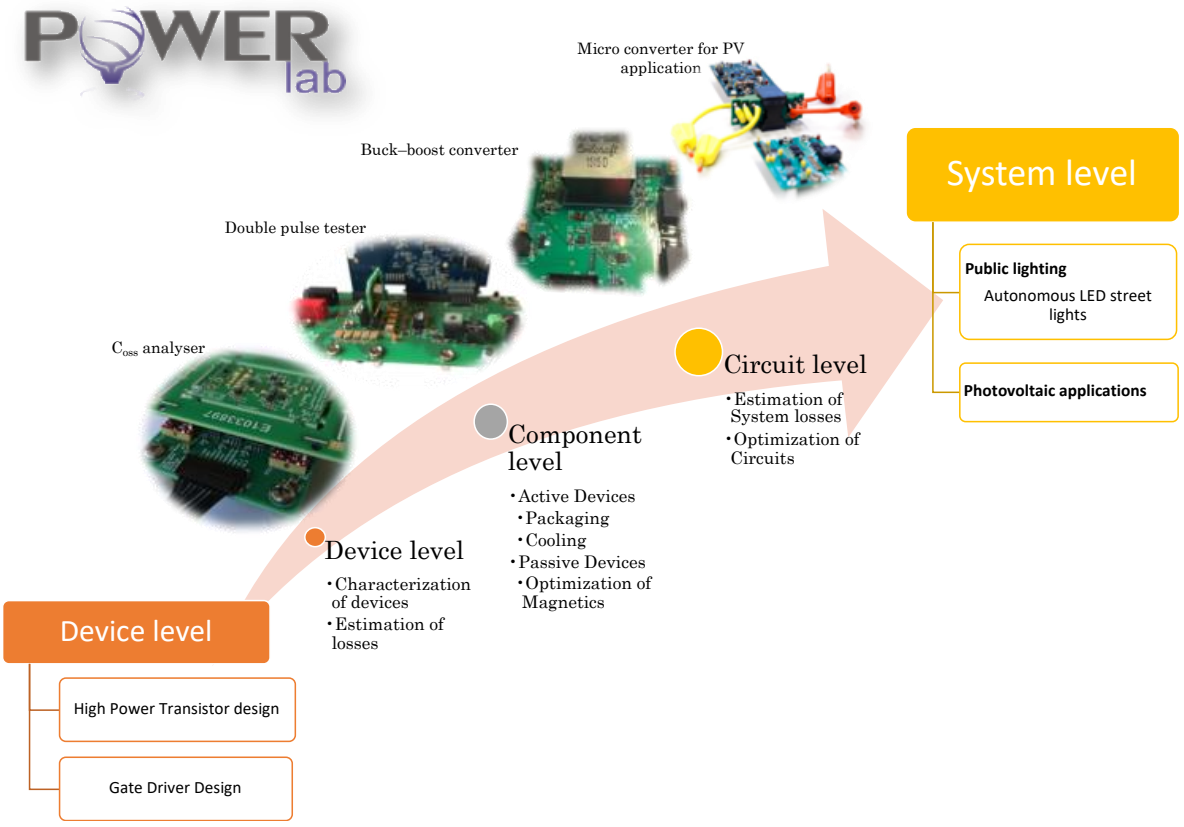


Figure 1: Our multi-disciplinary approach to achieve GaN-based high efficient power converters.

During the entire period of this project, the following team members have contributed to the work presented here:

Post-doctoral fellows:
Dr. Georgios Kampitsis, joined in September 2017
Dr. Martel Tsirinomeny, from Jan. 2016 to Jan. 2017

Ph.D. students:
Mr. Armin Jafari, joined in January 2017
Mr. Nirmana Perera, joined in March 2017

Master students:
Mr. Christian Westmark Sønnichsen, from Oct. 2017 until Jan. 2018

Bachelor students:
Mr. Simon Strobl, from Feb. 2018 until Jun. 2018
Mr. Enea Figini, from Feb. 2018 until Jun. 2018
Mr. Firmin Manoury, from Feb. 2016 until Jul. 2016

One of the challenges in a university environment is that some team members can only contribute to projects during a limited amount of time (typically Master and bachelor students), which sometimes interrupts the continuity of the projects. Despite these events, we managed to have advanced with this project in an exceptionally good pace. Below we describe a summary of the work performed during this project:

Device Level

Among the activities of our laboratory is the research on the device level (Section 6): this is the most basic level in our multi-disciplinary approach to demonstrate high efficient power converters, as shown in

Figure 1. We propose a new method to analyze the intrinsic characteristics of Gallium Nitride power devices from a circuit designer's perspective to improve the design of integrated power electronics for high efficiency applications. Based on preliminary results, we found that, in order to best utilize GaN devices for integration and high efficiency, a much better understanding of their switching behavior is required.

Component Level

This is the second approach we used to optimize our devices and circuits towards efficiency maximization and is presented in **Section 6.3**. We developed new test platforms in which we can utilize our PowerLab devices and evaluate their performance, **for the first time, in real circuits**:

1. We developed a new double pulse tester that can give us insight on the static and dynamic performance of our devices. It is accompanied by a front-end DC/DC converter and a clamping circuit for accurate measurements and fully autonomous operation (no manual actions are needed). The customized test platform is able to perform the following measurements:
    - **Dynamic resistance**: Our circuit is equipped with the required hardware and software to measure the voltage drop of GaN transistors under real operating conditions with varying quiescent voltage and duty cycle.
    - **Forward/reverse recovery**: the circuit should be flexible to measure diode characteristics as well.
2. We also demonstrated novel tri-gate GaN-an-Si Schottky barrier diodes (SBDs) with exceptional dynamic performance due to the low reverse charge. We tested our new diodes in a fully functional rectifier circuits up to 5 MHz.
3. In general, the GaN devices developed in PowerLab exhibit remarkable static characteristics (high breakdown voltage, large gate voltage swing capability, low on-resistance, low diode forward voltage, etc.). The knowledge gained by applying our transistors in real-life circuits (DPT and diode rectifier) is proven to be essential for understanding their dynamic performance and addressing the fabrication obstacles we face.

Circuit Level

The last step of our multi-disciplinary approach was to utilize GaN technology in high-efficiency compact converters. We aimed for applications that potentially have a large impact on our society and the way the energy is produced and distributed. We investigated, and still pursue, the potential of the new GaN technology in the field of renewable energy sources. We selected two very important applications in renewable energy as our first converter demonstrators.

1. The fully autonomous LED lighting system was the first project we undertook (see **Section 6.3.1**) because it can effectively address one of the major energy demanding requirements in

both urban cities and remote areas. With no grid connection requirements, minimum installation cost and long-life expectancy, this could be the ultimate lighting solution. During this period, we established collaboration with the architecture department of EPFL (ENAC) to propose a new structural design of the LED lighting system that makes it more functional, cost effective, reliable and visually appealing. As we progressed through the project in the fast few years, we developed more efficient and reliable converters and new battery management systems for a safe and long-lasting energy storage system. This initial system was key to establish new collaborations with lighting companies, such as A&B étude d'éclairage that will be working with us for the final product.

2. **Section 6.5** provides the design aspects and measurement results of a PV micro-converter. This work addresses the partial shading problem in PV systems, which is a necessity for next generation DC microgrids. Not only the converter is efficient, but also the method of local power extraction helps for harvesting the maximum available energy. In a summary, the power converter has the following characteristics:
    - Power capability of 400 W
    - High voltage step-up (Almost 12 times)
    - No external cooling requirements (neither heatsink nor forced air cooling)
    - Compact size and high efficiency (93%)
    - Galvanic isolation
    - Ability to be integrated in PV panels, due to the compact size
    - Based on wide band gap semiconductors (GaN and SiC)

As the continuation of the work, and to migrate toward higher power levels, the concept of a converter with two active bridges was used. This is an effort to evaluate the capability of GaN and high-frequency power transformers for achieving higher power levels and efficiency. The concept is scalable and could be used for applications such as electric vehicle charging, dealing with power levels of up to 10 kW.

3. National Cooperation

To execute this project, we have established collaborations in the national level with the following companies and laboratories:

- **Schrèder**
- ***CSEM (Neuchatel)***
- **A&B étude d'éclairage**: collaboration in designing public lighting system prototypes.

4. International Cooperation

During this period, in addition to the previous collaborations, we have also submitted a new collaboration project to a European Union funded project in the international level with Infineon technologies to investigate the potential of developing the technologies of our laboratory for commercial manufacturing.

5. Work undertaken in this project

The work that has been undertaken is summarized in **Table 1: Work undertaken and findings obtained** The following sections provide a thorough description of the project.

Table 1: Work undertaken and findings obtained

Milestones	2015	2016	2017	2018	2019
Assembly of first commercial circuit demonstrators					
Investigation of impact of GaN technology					
Growth of GaN materials and fabrication of power devices Starting with low power and going progressively to high power devices					
Design of circuit demonstrators Starting with low power and going progressively to high power applications					
Implementation of low power circuit demonstrators Starting with low power and going progressively to high power applications					
Using commercial state-of-the-art devices					
Using devices from our laboratory					
Implementation of higher power circuit demonstrators Starting with low power and going progressively to high power applications					
Using commercial state-of-the-art devices					
Using devices from our laboratory					
Feedback to our devices and circuit re-design					
Final circuit demonstration					
Final report					

6. Project details from device level

6.1 Introduction

Since the beginning of the project, we have achieved a significant design and fabrication improvement on the GaN transistors developed in the PowerLab ranging from low power GHz transistors to high current rating HEMTs with their gate drivers monolithically integrated on the same chip. We have also demonstrated novel tri-gate Schottky barrier diodes (SBDs) and developed high power PiN diodes. Still, various static and dynamic measurements and tests need to be performed before applying the newly developed devices in real-life circuits.
The double pulse tester (DPT) is a generalized platform that can give insight to the dynamic performance of our devices [1],[2]. It is a simple, yet effective test setup that is adopted by all transistor manufacturers. However, there is no such off-the-shelf setup. So one of the goals of this project was to develop a customized DPT circuit, able to perform the following measurements:

- **Dynamic resistance**: With the term dynamic resistance we refer to a known problem of GaN devices, their varying on-state voltage drop with the quiescent voltage level and the duty cycle of the applied gate pulse. Our circuit should be equipped with the required hardware and software to perform such complicated measurements.
- **Forward/reverse recovery**: the circuit should be flexible to measure diode characteristics as well.

6.2 Double Pulse Tester for dynamic performance characterization

6.2.1 Design Considerations

The basic topology of a DPT consists of the device under test (DUT) connected in series with an inductive load and a freewheeling diode, across a DC-bus. We decided to enrich this basic topology with a low-power DC/DC converter, as the front-end voltage regulator, shown in Figure 2(a), to develop a fully-autonomous test platform. The purpose of the input regulator is to automatically charge the decoupling capacitor, C_{DC}, to the required voltage reference, avoiding any manual operations. Once the DC-link is fully charged the device under test is switched with a double pulse, according to the waveforms in Figure 2(b). The turn off characteristic is recorded at t_1 and the turn on characteristic at t_2. The developed circuit board is depicted in Figure 2(c). Minimization of the parasitic elements of the circuit (e.g. parasitic inductances) was a crucial part of the design process, [3]–[5]. The bare GaN die is wire-bonded on the interface board and, subsequently, connected to the main DPT board as a regular TO-220 package.

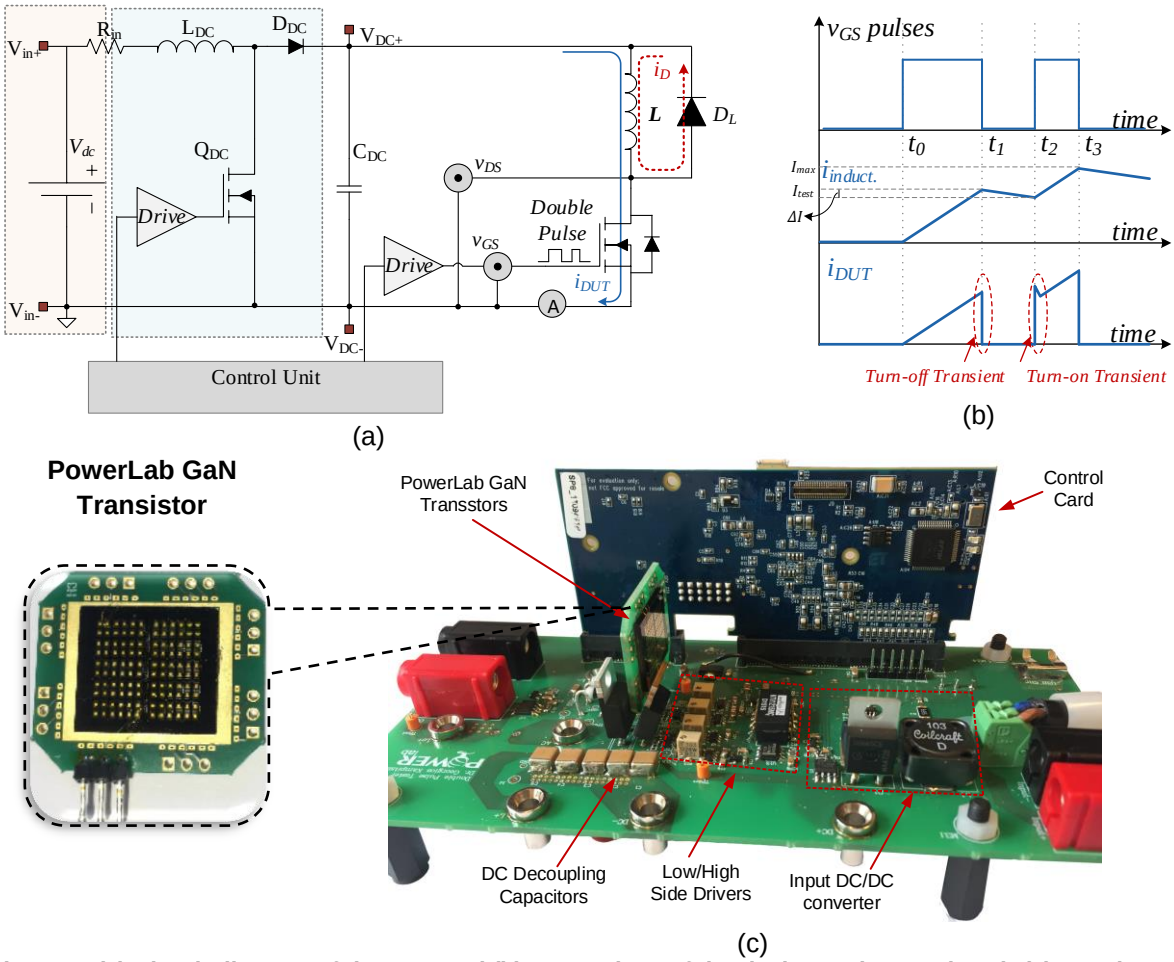


Figure 2: (a) Circuit diagram of the DPT and (b) gate pulses of the device under test (DUT). (c) Developed DPT circuit board featuring a PowerLab's GaN transistor.

6.2.2 Calibration and experimental Results

The DPT was first calibrated by measuring the switching losses of a commercial GaN device, TPH3212PS. The experimental results under 400V and 12A load current are presented in Figure 3 in normalized form. The extremely low switching losses, 65uJ during turn-on and 6uJ during turn-off, highlight the incredible potential of GaN technology. As a complementary test, we vary the gate resistance from 5Ohms to 20Ohms and record the switching losses. The results are shown in Figure 4.

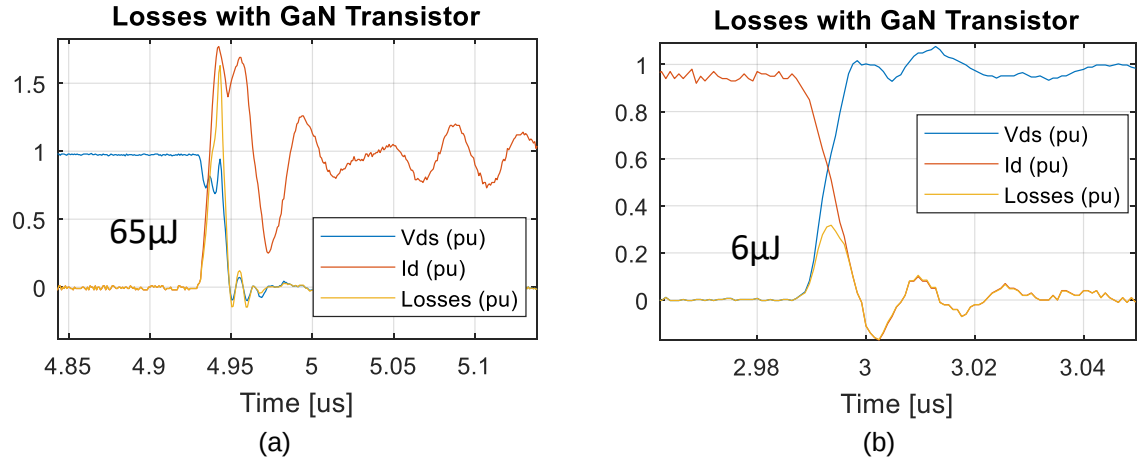


Figure 3: (a) Turn-on and (b) turn-off transients of the commercial device TPH3212PS, for calibrating the DPT.

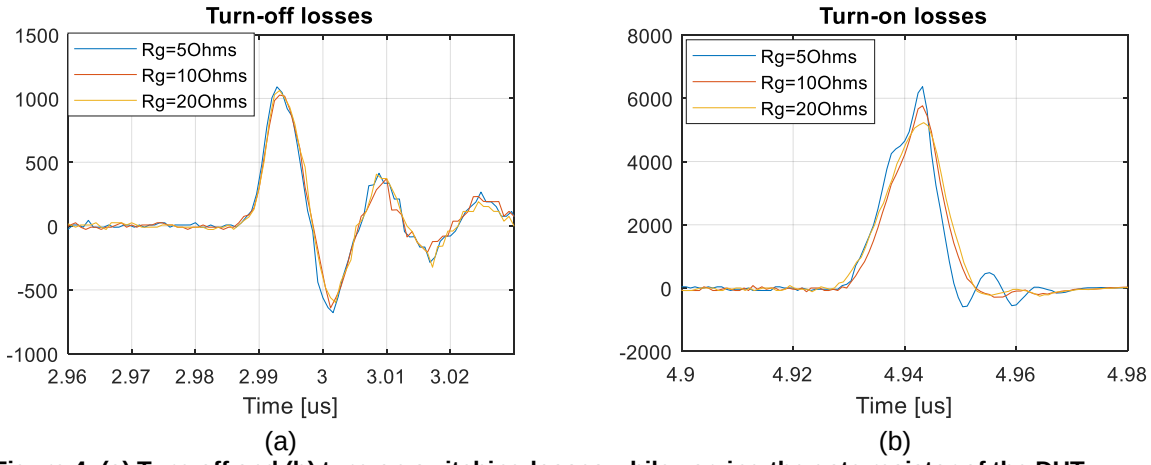


Figure 4: (a) Turn-off and (b) turn-on switching losses while varying the gate resistor of the DUT.

Having calibrated the DPT, we then proceeded on verifying the operation of the voltage clamping circuit for measuring the dynamic resistance $dR_{DS(on)}$ of our GaN devices. This phenomenon can be captured by a clamping circuit that allows an accurate measurement of $V_{DS(on)}$ when the power transistor is conduction, but clamps the DC-link potential to a low/fixed value when the device is in the off-state. A detailed comparative analysis of the different clamping alternatives is performed in [6] and [7]. Our circuit is based on a current mirror that provide constant current, manually regulated by an external resistor, and a set of well-matched clamping diodes, as shown in Figure 5. Instead of measuring directly the $V_{DS(on)}$, we now measure V_{AB}:

- In conduction mode $V_{AB} = V_{DS(on)}+V_{DA}-V_{DB} = V_{DS(on)}$, and
- In the off state V_{AB} is equal to the voltage drop of the series diodes D_1-D_4.

The methodology for capturing the $dR_{DS(on)}$ is based on charging the DC-Link capacitors at around 10V, through the front-end DC/DC boost converter and discharge them by turning-on the DUT with successive pulses of 1% duty cycle. While the device is ON we record V_{DS}-I_D characteristics as illustrated in Figure 6(a). As a first experiment we tested a commercially available power MOSFET and compared the performance of the developed circuit against a *power semiconductor parametric analysis tool* from AMCAD. The extracted curves with and without the use of the clamping circuit are

presented in Figure 6(b). This experiment proves the excellent performance of the clamping circuit and allows us to test for the first time our transistors, developed in PowerLab, in a real circuit.

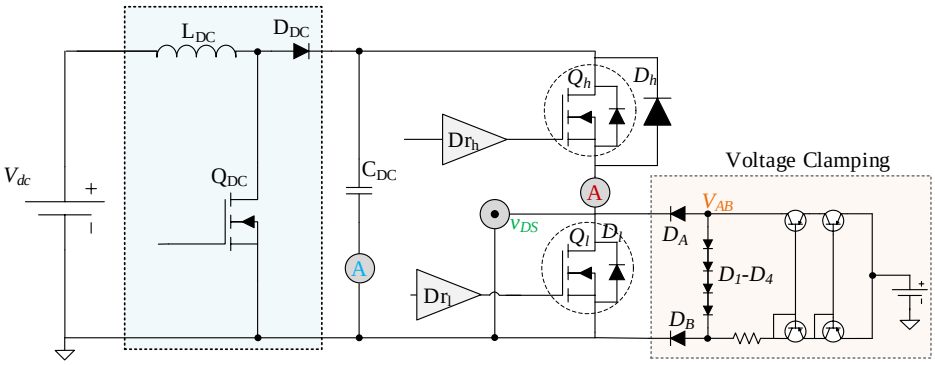
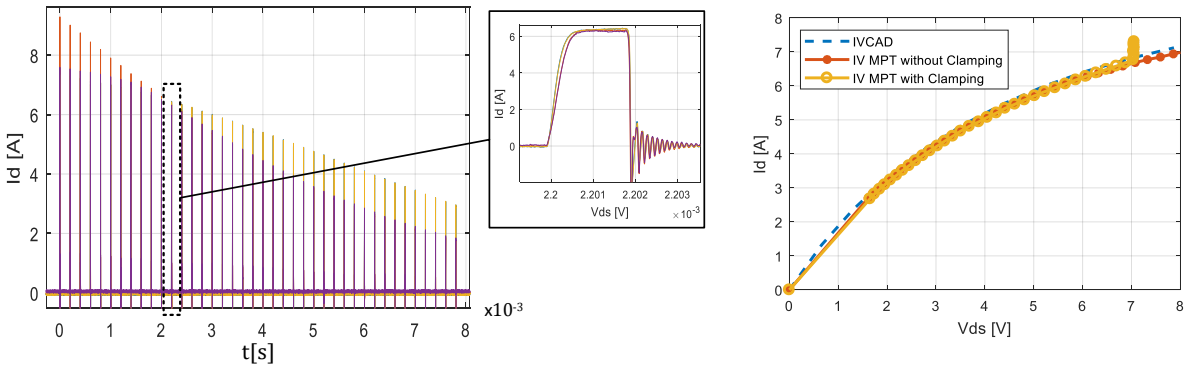


Figure 5: Voltage clamping circuit for measuring the dynamic $dR_{DS(on)}$.



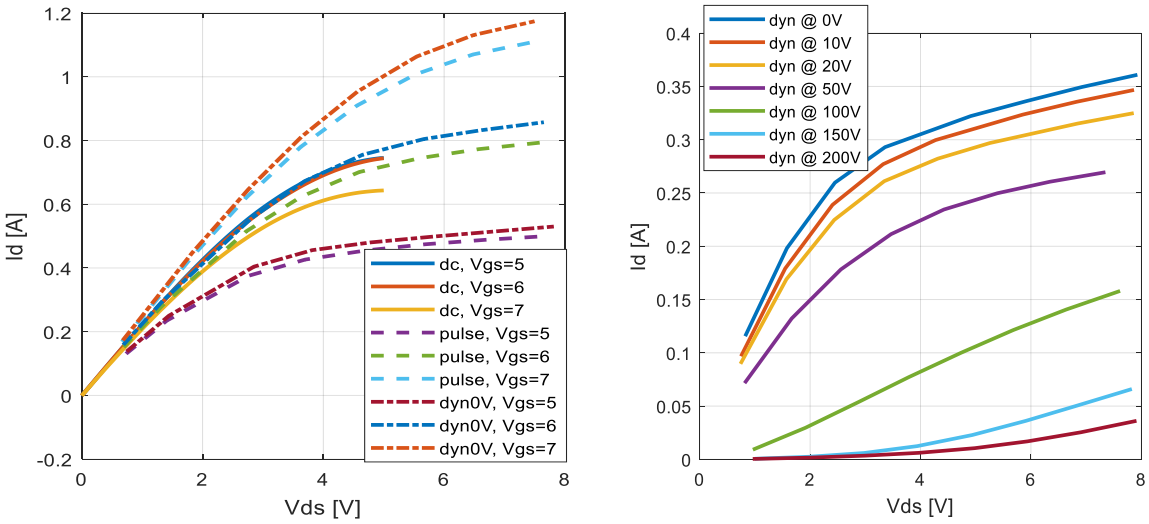
(a) (b)

Figure 6: Methodology for measuring the dynamic $R_{DS(on)}$. (a) Drain current in time domain during successive pulses of 1% duty cycle. (b) Dynamic I_D-V_{DS} characteristic with/without clamping circuit compared to the AMCAD system results.

Figure 7(a) shows the VI characteristics of the PowerLab GaN HEMTs under the same DC-link voltage and various V_{GS} voltage levels. More specifically, this figure contains three sets of graphs for comparison purposes:

- Static DC characteristics (named “dc” in legend and marked with solid lines). This is the most reliable method to extract the static characteristic of a transistor. However, if the pulse duration is long, the device may show low saturation levels due to self-heat-up.
- Quasi-DC characteristic. This means that the VI characteristic is extracted in segments with multiple pulses, while the quiescent voltage remains at 0V. This set of graphs is named “*dyn0V*” and marked with dashed-dotted lines. The curves appear to be above the static dc curves due to the shorter pulse duration and, ultimately, the lower heat-up.
- Dynamic VI characteristic (named “pulse” in legend and marked with dashed lines). These are the typical dynamic curves, which, as expected, are lower than the Quasi-DC characteristics, due to the trapped carriers under the 2-dimensional electron gas (2DEG) during off state.

The same PowerLab transistor is then subjected to dynamic IV measurements under the same VGS voltage and various quiescent voltage levels, ranging from 0V to 200V. The experimental results, shown in Figure 7(b), reveal a significant increase of the $dR_{DS(on)}$ with higher DC-link voltage. This is attributed to the large number of unwanted traps in the gate and buffer layer. It is a known behavior that can be addressed with a proper passivation technique.



(a) (b)

Figure 7: Measurement of the dynamic $R_{DS(on)}$ of the transistors develop in PowerLab. (a) Constant DC-link voltage and variable VGS. (b) constant VGS and variable DC-link voltage.

6.2.3 Switching Performance of our GaN Schottky Diodes

We also focused on expanding our product range by developing new high-performance lateral GaN power Schottky barrier diodes (SBDs) based on tri-gate architecture, [8]–[14]. With this architecture we achieved a significant reduction in ON resistance (R_{ON}) of 50%, down to 7.2 ± 0.4 Ω·mm, and much smaller forward voltage (VF) of 1.57 ± 0.06 V. We used a tri-anode structure to form Schottky contact, leading to a small turn-ON voltage (V_{ON}) of 0.67 ± 0.04V. Our approach resulted in an ultra-low leakage current (IR) of ~3 nA/mm at -650 V and a high breakdown voltage (VBR) of -900 V.

Most importantly, the devices presented promising switching performance, due to the small product of R_{ON} and reverse charge (Q), thanks to the optimized tri-gate geometry, and the high effective mobility (μ) of 2063 ± 123 cm2·V-1s-1 despite the small fin width (w) of 50 nm. The switching performance of the tri-gate SBDs was investigated using a rectification circuit with minimized parasitic elements through an optimized printed circuit board PCB layout and short interconnections (Figure 9). The device was directly bonded onto the PCB and connected directly to the oscilloscope and its internal function generator. The internal 50 Ω termination resistor of the oscilloscope was used as the load.

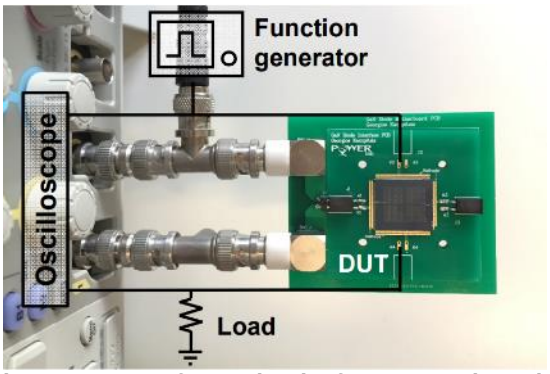


Figure 8: Interface circuit for measuring the switching characteristics of the developed SBD.

At a frequency of 1 MHz, the forward-recovery time of the tri-gate SBDs was as small as 13.8 ns (Figure 9(a)), along with a very short reverse-recovery time of 8.2 ns (Figure 9(b)), which did not change from 10 kHz to 10 MHz. Figure 9(c) shows rectification characteristics of the tri-gate SBDs, revealing an efficient rectification up to 5 MHz. The small phase shift between the input (V_{in}) and output (V_{out}) was likely caused by remaining parasitic elements in the circuit. The effectiveness of the rectifier can also be observed from the Lissajous plots of the I-V characteristics of the tri-gate SBDs in Figure 9(d).

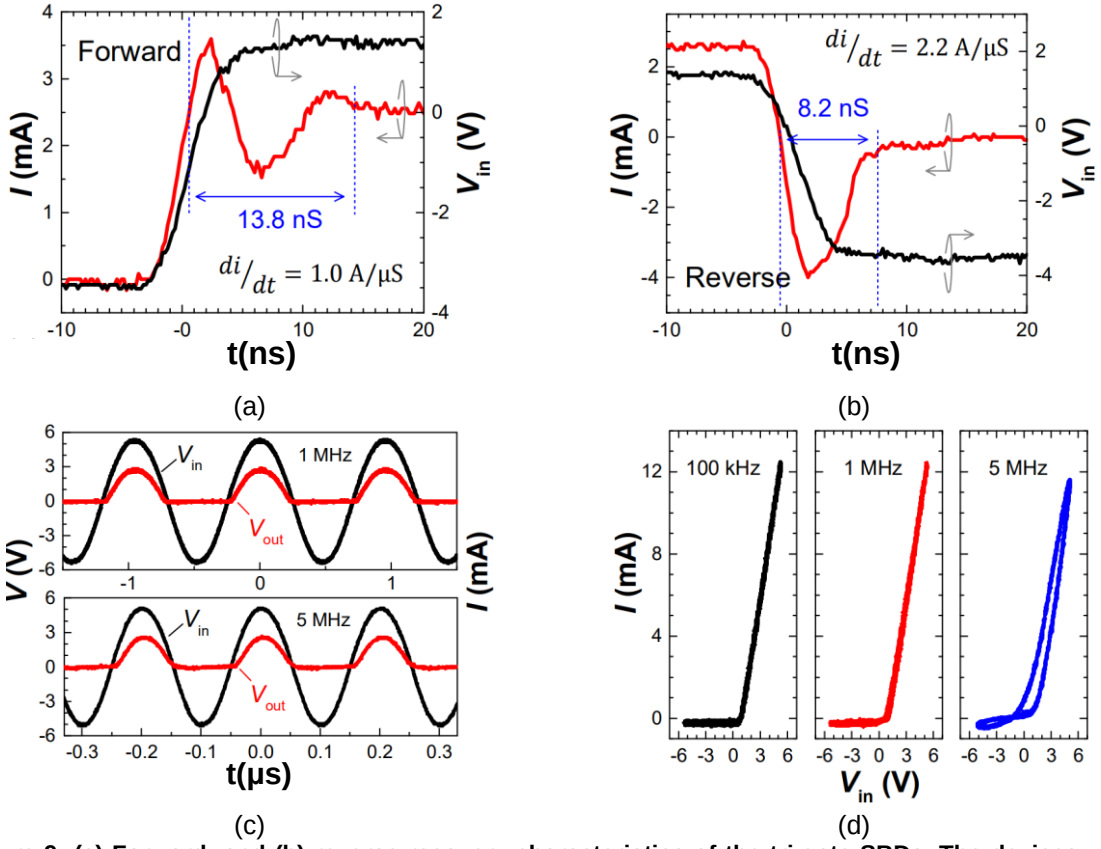


Figure 9: (a) Forward- and (b) reverse-recovery characteristics of the tri-gate SBDs. The devices were switched between 1.5 V to -3.5 V at 1 MHz. (c) Rectification characteristics and (d) Lissajous plot of the I-V characteristics of the tri-gate SBDs at different frequencies, using an external function generator.

6.2.4 Summary and future steps

In general, the GaN devices developed in PowerLab exhibit remarkable static characteristics (high breakdown voltage, large gate voltage swing capability, low on-resistance, low diode forward voltage, etc.). Our approach to combine in a unique way the excellent electrostatic control of the tri-gate structure with a high conductivity architectures, offers a promising platform for future advances in GaN power devices.

Our GaN Schottky diodes also show exceptional dynamic performance due to the low reverse charge. We are glad to announce that our devices work efficiently and reliably in real rectifier circuits up to 5Mhz. Our next goal is to use the developed technology to fabricate and demonstrate power SBDs.

For our GaN lateral HEMTs, further investigation is needed to improve the dynamic performance. The knowledge gained by applying our transistors in real-life circuits (DPT) is proven to be essential in order to understand and address the fabrication obstacles we faced. In particular, we aim to study and try different passivation methods in order to eliminate the traps and, ultimately, optimize the dynamic performance of our devices. In parallel we are working towards monolithic integration of the power device and the gate driver, a challenging subject that will allow ultra-compact and reliable converter design (due to the elimination of parasitic elements), even development of on-chip power converters.

6.3 Project details from circuit level

6.3.1 Energy savings potential

According to the report from *suisse énergie "l'éclairage efficace des rues avec des LEDs",* public illumination in Switzerland consumes about 410 million KWh of electrical energy, which corresponds to an annual expense of CHF 150 millions in public illumination. Studies from the Basel Agency for Sustainable energy conclude that upgrading the Swiss street lighting to a more efficient technology presents a huge energy saving opportunity of 130 GWh of electricity per year. The annual energy consumption of the commonly used high-pressure sodium lamps per illumination point is 500 kWh which could be reduced to 220 kWh by using LED light bulbs.

This project aims to maximize the energy saving potential of LED technologies by demonstrating autonomous LED-based street lighting, where the LED light bulb is connected to solar panels and batteries to use the energy stored during the day for night illumination, which will lead to a completely autonomous system. In addition to being a more efficient source of illumination, which can by itself save about 50% of the electricity consumption, LED street lighting can be dimmed automatically when there is less need for light. For example, in the middle of the night, the LED light intensity will be dimmed to 10%, which can significantly and reduce the needs in terms of solar panel area and number of batteries. *This solution could save the entire consumption of electricity in street lighting.*

In this project, we focused on developing and demonstrating small and highly efficient converters based on GaN devices to control the energy flow between the solar panel, batteries and LED light bulb. The converter will have sensors to detect the presence of people and determine the intensity of lighting. This will reduce the need for energy storage, thus reducing the size of panels and the number of batteries required. During the first year of the project, the practical aspects of lighting systems and PV-based energy storage were explored to well establish the scope of the project and its deliverables. The details are summarised in the next sections for the completeness of the report.

6.4 Autonomous LED Street-Light Project

In this part of the project, innovative solutions have been proposed and implemented to address one of the major energy demanding requirements in both urban cities and remote areas. Our goal was to demonstrate a fully autonomous LED-based lightning system. With no grid connection requirements, minimum installation cost and long-life expectancy this could be a groundbreaking lighting solution.

6.4.1 Introduction

This project has advanced remarkably during the past year. New architecture designs of the LED lighting system have been proposed that make it more functional, cost effective, reliable and appealing. We developed more efficient and reliable converters for harvesting the solar power. Specifically, we replaced the old modular system (with multiple flyback DC/DC converters) with a single generalized buck-boost converter. We thus increased the efficiency from around 85% to more than 96%.

An important part of this year's work was the development of the battery management system (BMS) for safe and long-lasting energy storage system. We included battery balancing and many safety features that increase dramatically the lifetime of our battery pack. We also developed a reliable communication between the different parts of the autonomous system based on the CAN protocol.

The outstanding work of all of our group members has resulted in a fully functional prototype of the autonomous lighting system. This year's results have brought our system closer to a final product driven by our society's requirements and needs, which is currently under prototyping phase under collaboration with the swiss design company A&B Etude d'éclairage.

The complete block diagram of the developed autonomous LED lighting system is depicted in Figure 10. The boost converter transfers the solar power to the energy storage system, while the LED driver sets the reference for the LEDs and regulates the load current. The presentation of each part will follow a bottom up approach, starting with the LED architecture and concluding with the PV generator selection, since the load determines the entire system.

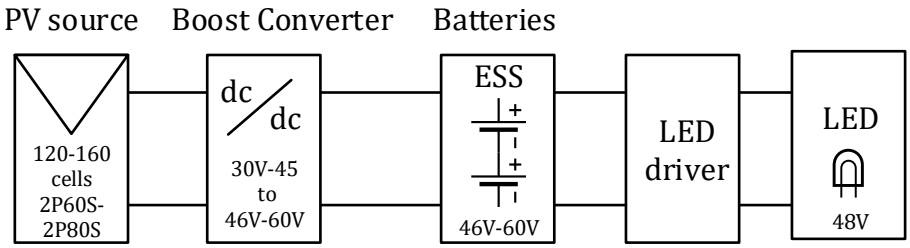


Figure 10: Block diagram of the developed autonomous LED lighting prototype.

6.4.1.1 Preliminary Study in Solar Power Utilization

The most important aspect to take under consideration in solar power sources is the variable PV power production during the day (clouds, rain, sun angle, etc.), and of course, the fact that there is no power production during the night. Also, the total PV energy production varies significantly during the year, as the sun radiance varies with season. A typical variation of the produced energy by a 1 kWc (watt-crete) PV system within one year is illustrated in Figure 11: Typical electricity production by 1 kWc.

Considering the constraints imposed by the design specifications within this project, the power rating of the PV generator is selected by calculating the mean value of the power produced over one year, which means that it will be undersized for cold months and oversized for summer months. A detailed review on arriving at the strategy for solar power accumulation is presented in the following sub sections.

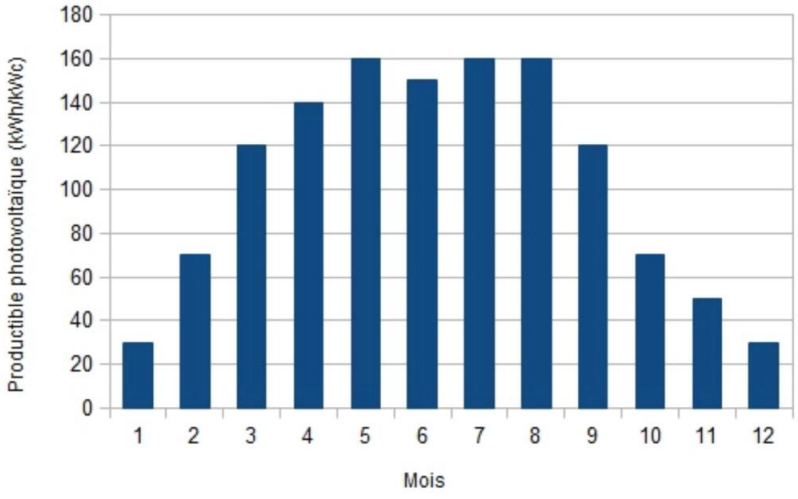


Figure 11: Typical electricity production by 1 kWc

6.4.1.2 Definitions and Regulations to Consider

The following is a quick summary of important terminology in solar power technology to establish grounds for the study presented next.

- *Luminous flux*: sum of radiation emitted by a light source evaluated by the human eye, measured in lumens [*lm*].
- *Luminous intensity*: power emitted by a light source in a given direction, measured in Candelas [*cd*]. Note that a light source doesn't generally radiate in every direction with the same intensity.
- *Luminance*: measure of the luminous intensity per unit area of light, emitted or reflected, travelling in a given direction measured in candelas per square meter [cd / m^2].
- *Illuminance*: total luminous flux incident on a surface per unit area, measured in lux [*lx*]

We can also define the ratio *R*: where $R = Illuminance/Luminance$. This ratio R depends on the reflectivity of the surfacing and is usually included in the range 13 to 15 for the case of a standard road.

The unit of interest in the domain of street lighting is the luminance, in cd / m^2. This is what is closer to the abstract concept of brightness sensation for the eye. It depends on many parameters, such as the luminous flux emitted by the light, its distribution in the space, the surfacing of the road, etc. It is then not straightforward to select the correct power of light for a given application knowing that the manufacturers usually provide the luminous flux and its direction, and therefore, has to be selected with proper knowledge. All the light installed on the outskirts of roads has to follow pre-determined rules. It is important to take notes of these norms early in the development process as it imposes several inflexible constraints that could question seriously the design developed.

The quality of lighting has a huge influence in terms of security and comfort on the road but also in terms of criminality. The light intensity as well as homogeneity are examples of parameters to think about when designing street lighting systems.

In Switzerland as well as in Europe, the street lighting is regulated by the norm *EN 13201*. As proof that the street lighting is in mutation, these norms have been recently updated from 2015 to 2016 to be compatible with today and future technologies.

The norm EN 13201 contains 5 documents describing the following:

1. Method for lighting class definition according to the traffic line.
2. Set minimum and maximum luminance and uniformity for each class.
3. Photometric performance computation rules.
4. Static and dynamic measurement methods.
5. Energetic efficiency computation taking into account a dynamic adaptation of the luminous flux.

A complete study of these norms is beyond the scope of this project, and therefore, will not be analysed in detail. We will, however, remember their existence for the time being and utilize them in the final stages of the project. For the first stage of this project, we will underline only the minimum luminance needed for our application and the limitations imposed when designing a dynamic adaptation of the luminous flux. As these norms are not available freely, the information has been found in application and recommendation guides of the norms [15,16]. We can underline the fact that the adaptation lighting can cause a discomfort for the residents close to the installation. Indeed, if the adaptation of the luminous flux is too fast, the blinking effect could be annoying for the residents. It has to be slow enough and then reduce the potential energy savings.

The other point of interest is the minimum luminance acceptable for an installation of the device on the EPFL campus. For the first prototype stage (in early work in 2016-2017), we made a choice has been made based on recommendations from Schreder, the manufacturer of the light chosen. The minimum luminance is then set to 0.5 cd/m^2 for the case of a residential street, which corresponds to a 38 W LED light model they are producing, the *Ampera MINI*.

6.4.1.3 Solar Radiation

The study of the annual solar radiation in the point of the installation is essential for a correct sizing of the components. The analysis has been done using the Photovoltaic Geographical Information System (PVGIS) online tool developed and provided by the Institute for Environment and Sustainability of the European Commission. This tool allows to compute the daily and monthly radiation for given coordinates, to analyse the performance of grid-connected PV and also to estimate the operating of a stand-alone PV installation couples with loads and batteries, with data coming from a choice of radiation databases.

Figure 12 provided by CM SAF, the Satellite Application Facility on Climate Monitoring, gives a first idea of the solar radiation in Switzerland. We can observe that the region of Lausanne is quite sunny compared to the rest of the country. A yearly sum of global irradiation around 1650 kWh/m^2 can be expected for optimally inclined photovoltaic modules. The sizing for this region may not be adapted for the rest of the country.

We will now evaluate the monthly radiation in Ecublens using the radiation database Climate-SAF PVGIS. This data is based on measurements from satellite images performed by CM SAF. The database represents a total of 12 years of data, from 1998 to 2005 and June 2006 to December 2011.

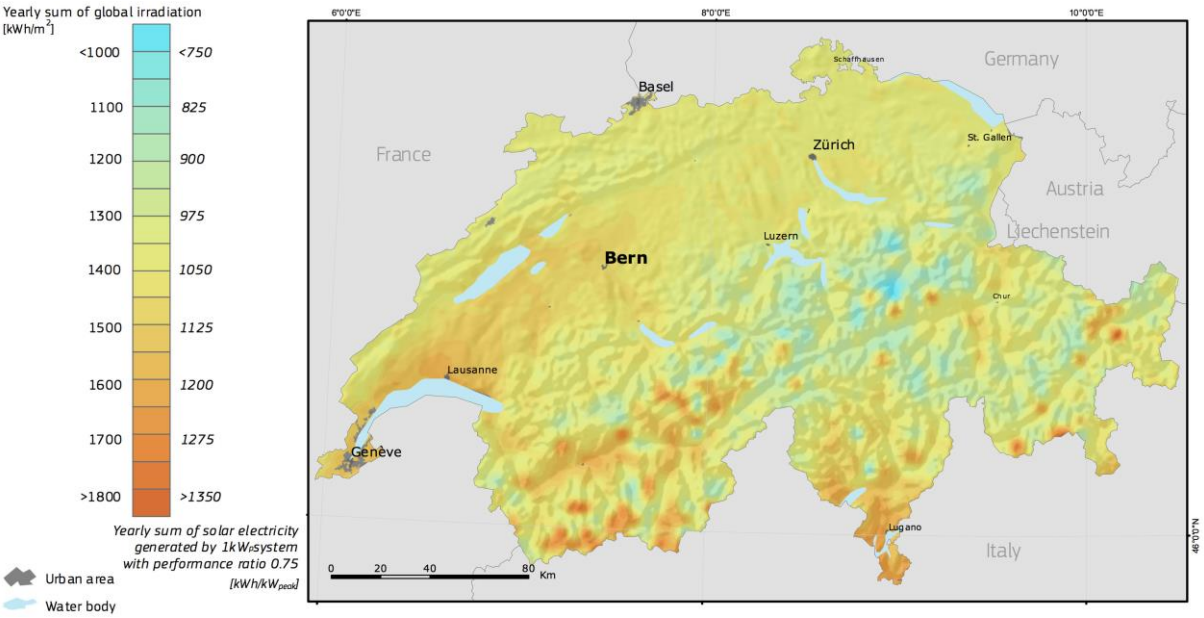


Figure 12: Irradiation and solar electricity potential for optimally inclined photovoltaic modules in Switzerland.

Month	H_h [Wh / m^2/ day]	H_{opt} [Wh / m^2/ day]	H(66) [Wh / m^2/ day]	I_{opt} [°]
Jan	1200	1980	2170	64
Feb	2220	3460	3660	59
Mar	3810	5050	4910	48
Apr	5040	5730	5010	33
May	5830	5870	4690	19
Jun	6570	6290	4800	13
Jul	6480	6370	4930	17
Aug	5510	6000	5030	28
Sep	4250	5380	5050	43
Oct	2650	3810	3890	54
Nov	1450	2380	2590	63
Dec	1000	1700	1900	66
Total	**3840**	**4510**	**4050**	**37**

where,

H_h : Irradiation on horizontal plane.
H_{opt} : Irradiation on optimally inclined plane over the whole year (37°).
H(66) : Irradiation on plane at angle 66°, optimal inclination in December.
I_{opt} : Optimal inclination.

Table 2: Average monthly incident global irradiation in Ecublens

In Table 3 are presented the average monthly incident global irradiation in Ecublens for different angles of inclination of the panel south-facing. We are then able to compare the incident global irradiation on a horizontal plane, on an optimally inclined plane over the whole year and on a plane at angle 66° as well as the optimal monthly inclination.

First of all, we can observe that the worst month in terms of irradiation is in December. As the objective of the system is not to maximize the annual energy production but to have a system always operational minimizing the size of its components, the inclination of the panel will be set in order to be optimal in
December, at 66°, and not at the annual optimal angle of 37°. This way, we will maximize the minimum incident global irradiation.

We can see in Table 2 that the average monthly minimum energy available will be of 900 Wh / m^2/ day for an angle of the panel of 66°. If the angle was set to 37°, the average energy available in December will be only 1700 Wh / m^2/ day. By having a horizontal plane, this energy falls to 1000 Wh / m^2/ day. This underlines the importance of the inclination angle in the process of optimization of the system.

For later consideration in the sizing process, the average monthly minimum energy available will then be set to E_{rad} = 1900 Wh / m^2/ day. For the rest of the year, the amount of energy received is large enough and the system will necessarily be oversized.

Another important parameter to take into account for the sizing of the system is the length of the day, or more specifically, the length of the night during which the light will be turned on. For this purpose, we use the tool *Suntag* [18]. Suntag computes the theoretical number of hours of sunshine in every location in Switzerland taking into account the topography of the location as well as the trajectory of the sun. Table 3 presents the monthly average duration of daytime and time of sunrise and sunset in Ecublens.

Month	Daytime	Shade begins	Sunrise	Sunset	Shade ends
Jan	8h29	8h14	8h34	17h03	17h11
Feb	9h48	7h38	7h57	17h57	17h57
Mar	11h19	6h47	7h05	18h38	18h38
Apr	12h56	5h47	6h04	19h20	19h20
May	14h11	5h00	5h22	19h59	19h59
Jun	14h57	4h41	5h05	20h27	20h27
Jul	14h38	4h56	5h18	20h23	20h23
Aug	13h30	5h32	5h51	19h44	19h44
Sep	12h01	6h11	6h28	18h46	18h46
Oct	10h25	6h50	7h08	17h48	17h48
Nov	8h52	7h35	7h55	17h00	17h00
Dec	**8h05**	**8h11**	**8h34**	**16h45**	**16h45**

Table 3 Monthly average duration of daytime in Ecublens

As expected, December is the month with the shortest daytime, and thus, the longest nighttime. The street light should then be operational between the sunset at 16h39, until the sunrise at 8h34, this means a theoretical duration of 15h55. Obviously, the street light will not be at 100% during the whole time; therefore, the energetic strategy will come into play to reduce the energy consumption.

6.4.1.4 Energetic Strategy in Accumulating Solar Energy

To evaluate the average daily solar energy needed, it was necessary to build a model to estimate the energetic strategy of the system. As describe earlier, one of the challenges is to develop an energetic strategy that will minimize the energy consumption by regulating the luminous flux of the light based on luminosity and motion sensors.

Information about the traffic density provided by the general transport management of Geneva [19] has been used to evaluate when the light will be turned on at 100%. As an example, Figure 13 presents the standard daily distribution of the traffic on a highway in Geneva for both directions based on data from 2010.

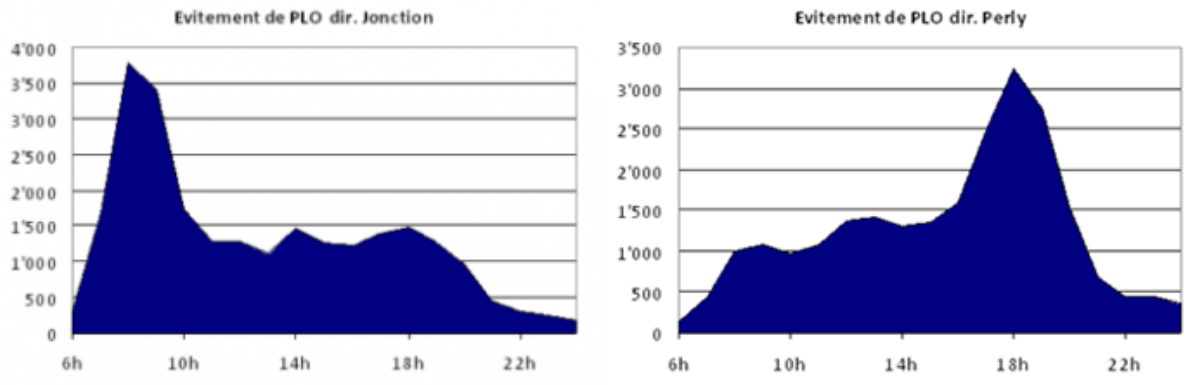


Figure 13: Standard daily distribution of the traffic on a highway in Geneva

It allows us to have an estimation of the peak times during which the light will be turned on. We can estimate the morning one between 7h to 9h and the evening one between 17h to 20h. This permits to set that the night reduction of the flux can begin around 20h and finished at 7h. As before, the worst case of December will be taken into account. Given the sunrise and sunset time presented previously, the street light should be operating at high power between 16h39 to 20h and between 7h to 8h34, at least. During the rest of the time, the intensity of the luminous flux will be controlled by the sensors.

Two different estimators have been developed, one with a weak attenuation and the other one with a stronger attenuation of the flux. Figure 14 represents the estimated average hourly power of the light in percent of the rating power of both estimators.

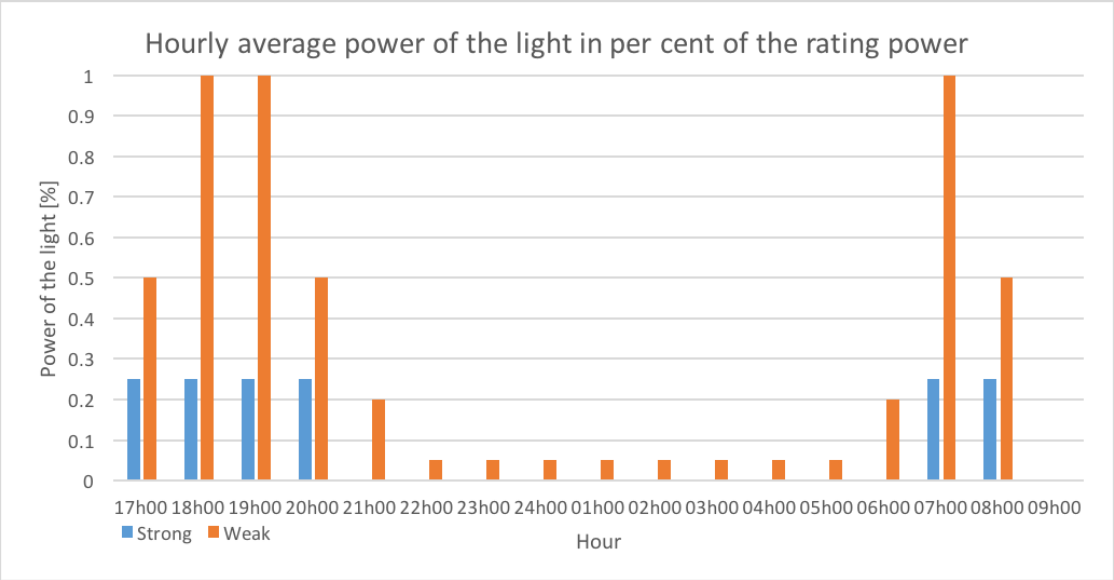


Figure 14: Estimated average hourly power of the light in per cent of the rating power.

The weak strategy (in orange colour) follows the schedule defined above and reduces the power of the light to 5% during the night. Moreover, 1 hour at full power is added to the daily consumption to take into account the motion sensor that will increase the flux to its maximum when a user is passing through. This corresponds to 180 detections for a boosting of the light for 20 seconds.

The strong strategy, in blue, is way more restrictive with a power reduced to 25% during the peak time and then completely switched off. 1 hour at full power is also added to account for the sensor. This situation corresponds a really low usage of the street light on an uncrowded road.

These two estimators give a range of usage duration for the rest of the sizing, presented in Table 4.

Strategy	Strong	Weak
Regular time [h]	1.5	5.3
Sensor time [h]	1	1
Total time [h]	2.5	6.3

Table 4 Estimated usage duration at 100% for both strategies

The content of this section is an estimation of the energetic strategy estimated for the sake of sizing. The strategy itself is open to future development, the idea being the development of a strategy based on the time of the day and on measurements provided by a luminosity and movement sensor in fuzzy logic. The luminous flux is then adapted by the strategy depending on the time of the day and the ambient luminosity, as well as the actual usage of the road where the street light is installed. Fuzzy logic can be easily implemented in embedded microcontroller.

The discussion carried so far emphasizes the importance of the efficiency of the system as the solar power production is of variable nature, especially during the winter periods. Therefore, it is essential

that the power converters of the system can extract all the power it can from the PV without wasting large losses for their own operation. And more importantly, the stored solar power in the energy storage unit should be transferred to the LED lights with highest efficiency to save energy.

6.4.2 The Converter Stages: First stage results of the work

To make a coherent case of the converter design we will describe the decisions made in the first stage of the project and follow up with the necessary modifications made in the final part of the project.

6.4.2.1 Preliminary design of the converter stages: Design approach

Let us consider a single LED street light equipped with an integrated PV solar panel on the top and batteries inside the pole. In this scenario, the system is fully isolated from the grid, which makes it possible to be installed in remote areas. The PV panel charges the battery during the day, while during the night, the stored energy is transferred to the LED light. The solar panel never feeds the LED light directly. The challenges arise when the solar irradiance is limited, due to bad weather conditions, resulting in low power production during the day, considering, at the same time, the small size of the PV panel. Since no connection to the grid is considered, an energy-saving strategy should be adopted, to significantly reduce the consumption during the night. It should be emphasized that a very highly efficient converter stage translates to “Increased ON time” for the LEDs.

In this project, both circuits controlling the energy flow, the one from the PV panel to the batteries (*converter stage 1*), and the other from the batteries to the LEDs (*converter stage 2*), are based on GaN devices. This allows the miniaturization of the circuit, since it switches at much higher frequencies: the size of the passive components (i.e., capacitors and magnetic components) in the circuit is reduced and the requirement for large heat sinks is eliminated. The extra area allows for intelligence features to be introduced, for optimum usage of the energy stored in the batteries and overall system efficiency increase.

The LED light should be bright enough for safety and comfort reasons, yet small enough to be fed by a small battery. The choice GaN-based LED lighting is due to their higher efficiency and dimmable property, which allows us to efficiently control its illumination based on inputs from external signals, with some optimized intelligent features. A second converter stage, responsible for charging the batteries from solar power also needs to be simple and efficient. However, since the solar power is source of variant nature a conclusive study was carried out to identify the viability of the solar power source throughout a year.

The converter power stages are the heart of the system. In the first two years of the project, we investigated several topologies and tested hardware prototypes to obtain efficiency trends. The second version of *converter stage 2* (batteries to LEDs) exhibited very high values of efficiency up to **96%**.

A close investigation of the power converter stages revealed that the converter should be small enough to be ideally integrated into the global system, which would also reduce its cost, while being very efficient, to reduce the requirements on the solar panel and batteries while increasing the system lifetime. The large speed of GaN technology allows the switching frequency to be increased without huge switching losses. And since the value of the passive components (L, C) is proportional to the switching frequency, their size can be significantly reduced. However, smaller magnetic components result in higher magnetic losses, thus reducing the system efficiency, as explained in detail in Appendix 6.5. Design of magnetic components is, indeed, another field that we are investigating, both from scientific and practical perspective, to allow the full exploitation of our technologies, since some of the components required cannot be found commercially.

The firstly imagined overall block diagram of the Autonomous LED Street-Light system is illustrated in Figure 15.

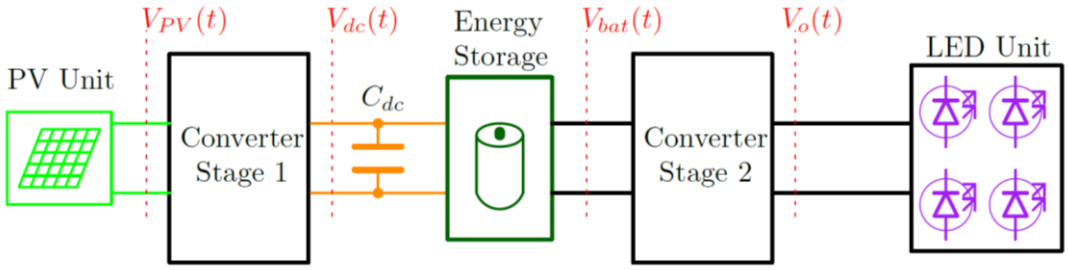


Figure 15 Block Diagram of LED Street-Light System

The PV panel captures the solar energy during the day-time and the *converter stage 1* is used to efficiently transfer this captured power to the battery-based energy storage unit. The primary role of the *converter stage 1* is to track real time the maximum available power of the PV panel and to charge the batteries accordingly, taking into consideration the all safety limits. Then during the night time, converter stage 2- transfers the stored power within the batteries; the primary role of the *converter stage 2* is to regulate the power fed to the LED light according to different lighting requirements. The overall system requires a set of global control rules to establish a standalone intelligent system. It is also important to select a proper battery charging circuit: the charging method affects both the battery life and charging time. However, ensuring maximum efficiency of the *converter stage 2* is most critical to achieve optimum power management during the night. Therefore, we have put substantial effort to explore better topologies and control strategies for this.

In other words, we need to minimize the losses in the converter stages. First, we need to determine which is the most energy consuming part of the conversion process. To reduce the effect of switching losses in conventional Si-based solutions, soft-switching is often required. However, we believe that a thorough investigation should be performed to determine whether this is the best solution when dealing with fast GaN devices. This is because soft-switching complicates the system by introducing additional circuitry and, sometimes, daunting control tasks. With these points in mind, we are initially considering simple and cost-effective converter topologies that serve our purpose.

6.4.2.2 Preliminary design of the converter stages: Summary of the first development (year 2016)

One of the goals of the first version of this project was to identify the technical strategies and limitations in incorporating GaN devices into known topologies. We, firstly, used commercial GaN Field Effect Transistors (FETs) EPC8010 from Efficient Power Conversion (EPC) to implement and test our converter circuit. The circuit board was designed with Altium Designer and the final PCB is shown in Figure 16 (a). Figure 16 (b) reveals the very small size of the GaN transistors and the absence of heat sinks, which makes the circuit size much smaller compared to other technologies. Figure 16 (c) shows the measured efficiency against the output power of this first version of the circuit, with a maximum of 87%, a relatively good value, especially considering that this was the first version of the circuit with some un-optimized components.

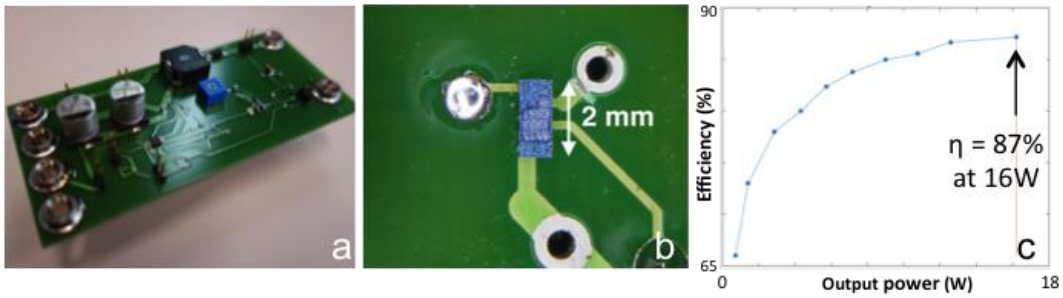


Figure 16 (a) PCB designed with Altium. (b) GaN transistor. (c) Efficiency versus output power.

6.4.2.3 Preliminary design of the converter stages: Second development (Year 2017)

With the gained knowledge and experience from the first stage in year 2016, we worked on the optimization of the efficiency of *converter stage 2*. In this version, we used commercial GaN devices as well, to evaluate the operation and the control of our medium-to-high power converters. In future work, we will use the power devices and gate drivers developed in our laboratory that will be designed for this specific application in order to optimize the final system.

For this prototype, our focus was placed on the correct operation and control of the system, rather than the size of the circuit. In fact, one major aspect that determines the size is the ease of measurements during testing. Once were satisfied with the full operation of the system and the control, we moved to the final design (year 2018) that minimize the size of the system to achieve maximum efficiency.

Analysis and design
The LED unit selected is the commercial AMPERA MINI (004A7) from our partner Schreder, which consists of 24 individual LEDs and has 38 W output power. The unit is shown in Figure 17. The nominal input voltage of the LED unit is 76 V and the nominal input current is 500 mA.

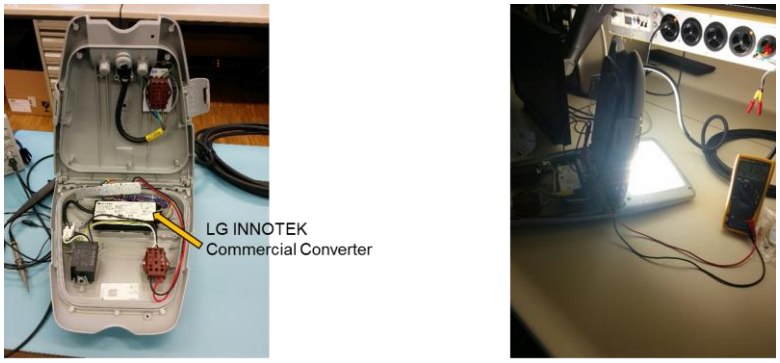


Figure 17 Commercial LED unit from Schreder: (a) inside of the unit showing the commercial converter, (b) Unit turned-on with 3-phase input supply

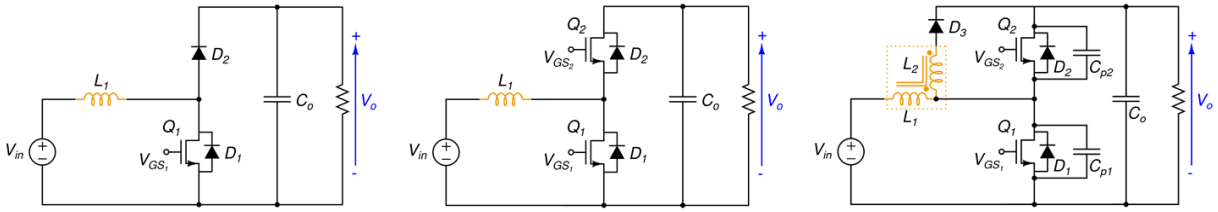
We considered the following important points in selecting the topology for the *converter stage 2*:

1. High efficiency (low losses) to save the battery energy and reduce the requirements on the solar panel surface.
    a. We need to have minimum constant losses (on the auxiliary system). Simple control circuits draw less power, and low number of switches minimizes the gate drive losses.
    b. We need to minimize the switching and conduction losses. Again, lower number of switches would minimize losses even with hard switching.

6.4.2.4 Minimum number of passive components would minimize their own losses as well.

2. No isolation requirements (as no grid connection is considered)
    a. A non-isolated dc-dc converter is the most cost effective solution that would also give a high power density

Since there are no high-gain requirements and the nominal power is just 38 W, complex topologies were not necessary. Based on these requirements, we selected three different converter variations, shown in Figure 18. Our goal is to use a single PCB for all tests, including efficiency comparison, which allows us to understand more about the losses of different components and their contribution in high-frequency GaN-based circuits.



(a) Topology T1 (b) Topology T2 (c) Topology T3

Figure 18 The three variations of the topologies selected for converter stage 2: (a) T1, standard boost converter with hard switching; (b) T2, synchronous boost converter; (c) T3, soft switching boost converter with coupled inductors

A general illustration of the occurrence of conduction and switching losses (of the power devices) for the three topologies is presented in Figure 19: the device notation is in accordance to Figure 18. To understand the operation of the circuits, the device turned-ON periods for two switching cycles are shown: T_{sw} is the switching period, d is the duty, and T_d is the dead time (exaggerated to show the duration). The corresponding losses of all the power semiconductor devices are illustrated to predict the loss performances that could expect from the practical circuits. Also, note that magnetic and control unit losses are not included here.

It can be seen that transistor Q_1 conduction losses are common to all three topologies. The major difference between topologies T1 and T2 is the conduction loss of the diode D_2. This loss is eliminated in T2 and can be practically represented as a switching loss during the dead time as shown. The conduction loss of the diode is a major contributor to overall losses and depends upon the output current (I_{out}) rating. This can be approximated as, $P_{D2}(conduction) = V_f I_{out}$ for its ON-time; here V_f is the diode forward voltage drop.

By moving to topology T3, apart from the benefits from T2, additional loss savings come from the minimized switching losses achieved by introducing a soft-switching mechanism. The corresponding loss diagrams are shown in Figure 19. However, it is important to note that, this new mechanism requires an additional diode D_3, an inductor L_2, and two snubber capacitances C_{P1} and C_{P2} as shown in Figure 18. The diode D_3 introduces new losses to the system. Therefore, a fair comparison of T2 and T3 depends upon the severity of the switching losses (mainly depends upon the output power level of the circuit): this is something we intend to investigate further.

Furthermore, all the three topologies have magnetic losses due to the inductor L1 (T3 has additional losses due to L2); more on this will be explained in the latter part of this section. A summary of the three topologies is tabulated in Table 5 A summarized comparison of the three topologies selected for converter stage 2 to show their major differences in context.

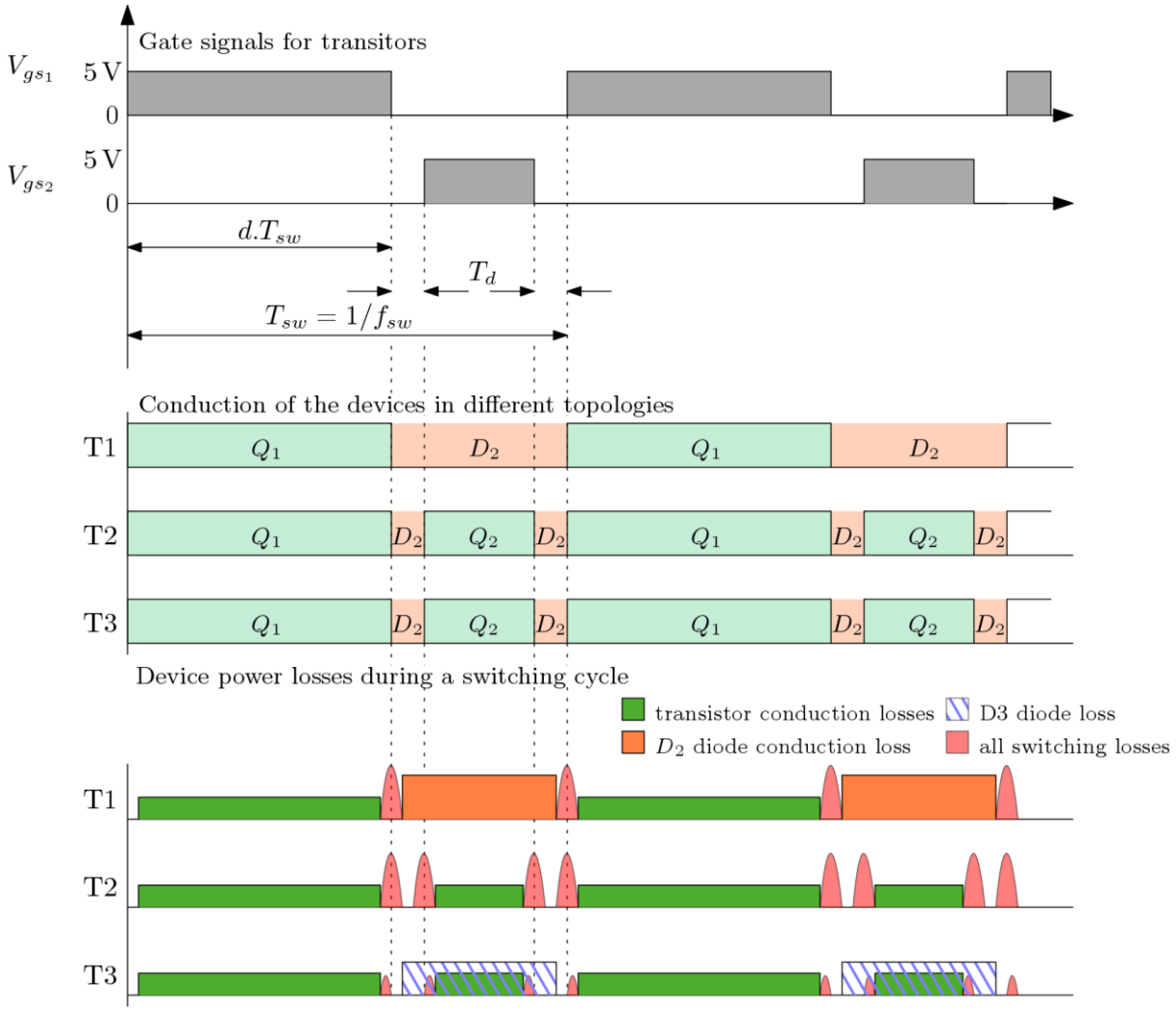


Figure 19 A general comparison of device losses (not to scale) of the three topologies for a single switching cycle

Characteristics	Topology		
	T1	T2	T3
D_2 diode conduction loss	yes	minimized, dead time only	minimized, dead time only
Gate drive requirement	one switch	two switches	two switches
Switching loss type	hard	hard, but soft switching for S_2	hard, but soft switching for S_2
Switching method	conventional	conventional, complementary	conventional, complementary
Additional components	0	1	3

Table 5 A summarized comparison of the three topologies selected for converter stage 2

Hardware Design of the Circuits

One of the main ideas that we implemented in the second version of the project was to develop a set of plug-and-play boards. This helps to test different variations of the system and understand different loss factors without the need to build new circuit boards. For example, with this approach we can test the same topology but with different inductors, as shown in Figure 20, in order to evaluate the operation at different frequencies. We also use a separate control board to provide maximum flexibility

in the testing phase. Furthermore, we have intentionally oversized the circuit so that all devices can be probed easily for measurements and troubleshooting.

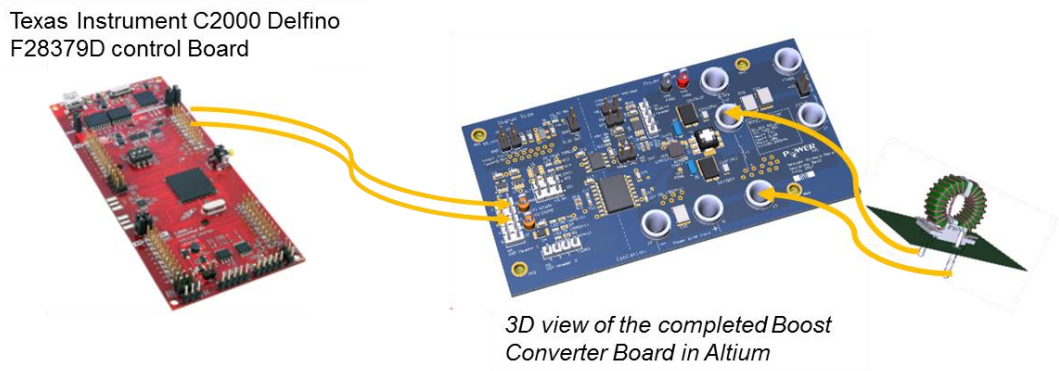
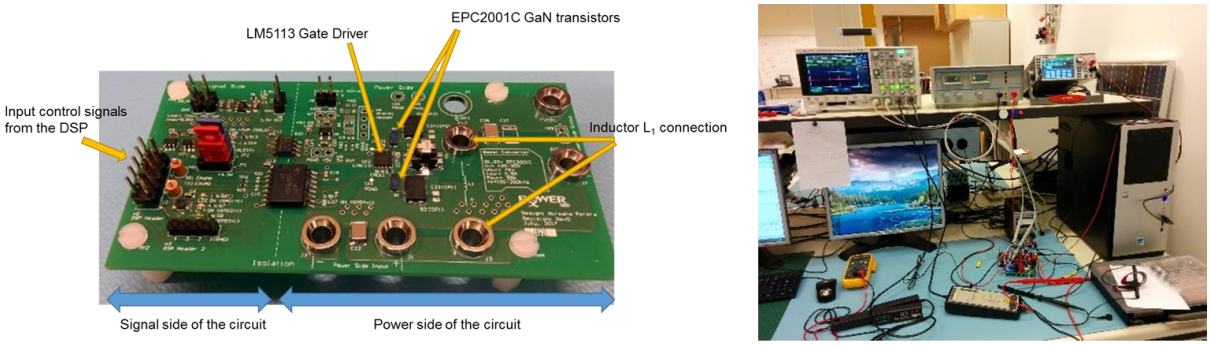


Figure 20 Design of the new plug and play type test boards and components

The fabricated PCB of the second version of the project is shown in Figure 21 (a). Figure 21 (b) shows the wired hardware test setup in our laboratory, during testing. However, the testing and measurement techniques for GaN-based devices are different compared to their well-established Si counterparts, mainly due to higher switching frequency. Therefore, this process served the additional purpose of acquiring new knowledge on testing and measurement techniques for to GaN power devices.



(a) (b)

Figure 21 Development and testing of the Boost Converter unit for Converter Stage 2: (a) manufactured PCB, (b) the experimental test setup

Experimental Results

We tested the topologies T1 and T2 (Figure 18) and obtained very promising efficiency results for the power circuit. The converter was tested at both 10 W and 40 W output powers with the following test conditions for a simple resistive load, R_L: R_L = 40 Ω, dead-time T_d = 50 ns for topology T2, duty cycle ≈ 50%, L_1 = 220 µH (with 0.2 Ω dc resistance). We tested both T1 and T2 topologies with carrier frequency ranging from 100 kHz to 500 kHz (note that in our topologies the carrier and switching frequency is the same), to understand the effect of switching frequency on system losses.

The efficiency against switching frequency results are plotted in Figure 22, for both examined topologies. We observe that topology T2 outperforms topology T1 for both power levels and all carrier frequencies. The main reason for this is the inhibition of the conduction of Diode D_2 in topology T2 (refer to Figure 18 and Figure 19), as minimizing the conduction time of any diode in the circuit would result in reduced system losses. However, the idea was to evaluate the trade-off between the increases in efficiency in topology T2 and the complexity and cost of an additional power transistor.

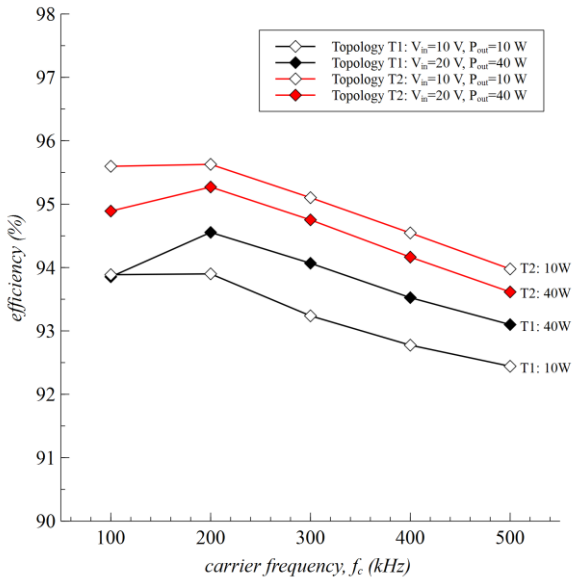


Figure 22: Efficiency comparison of the topologies T1 and T2 which candidates for the converter stage 2 of the system

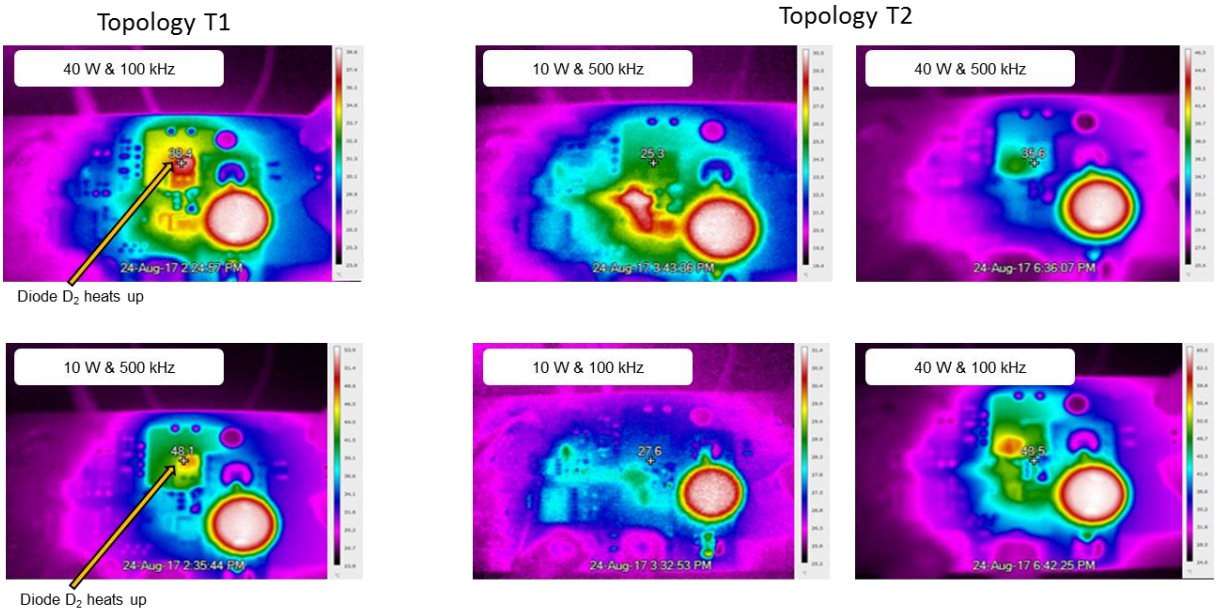


Figure 23: Thermal Images of the circuits during normal operation

A quick and practical way to identify the loss factors of a given circuit is by measuring the temperature rise of each component of the circuit. Thermal images taken during the operation of the circuit are shown in Figure 23: Thermal Images of the circuits during normal operationfor different operating conditions.

Considering the thermal images, we can quickly see that diode D_2 in topology T1 heats up compared to topology T1, confirming the efficiency results and loss analysis. The most important thing to notice here is that in all cases and in both topologies, the inductor is the component that heats up the most (this can be seen as the light round portion of every image near the bottom right corner). Furthermore, Figure 24 shows a thermal image taken on a GaN based commercial boost converter circuit board (Texas Instrument LM5114). The image shows how the inductor heats up to a higher temperature compared to other devices on the circuit. These results can be interpreted that, at these power levels and frequencies, the inductor losses are dominant.

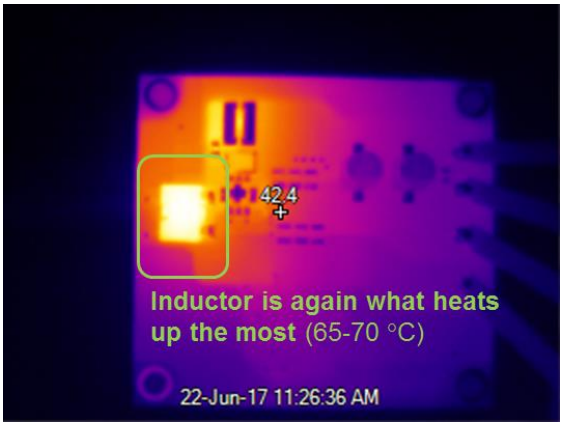


Figure 24 Thermal image showing the heating-up of the inductor of the Commercial LM5114 Evaluation Board with EPC 2001C GaN Devices

Conclusions from the Preliminary Test Results of Year 2017 results

- The commercial, Si-based converter that was originally used to power the Ampera LED unit showed an efficiency of **83 %**, at rated power (38 W and 500 mA).
- We also tested a GaN based commercial boost converter circuit board from Texas Instrument, LM5114 Development board. This platform showed an efficiency of **94-95%** (30-40 W, 500 mA output at 500 kHz).
- The basic converter built during the first version of the project resulted in an efficiency of **87%** at 16 W output power (see Figure 16).
- The converter topology T2 developed at our lab in this second version of the project, shows an efficiency near **96%** at 0.5 A and 1 A outputs (corresponding to 10 W and 40 W, respectively) up to switching frequencies of f_c = 200 kHz.

In the developed topology T2, when reaching up to 500 kHz, efficiency drops to around 94%. The reduction of the efficiency at increasing frequencies can be categorized into three fields:

1. Losses in the power semiconductor switches
    a. switching loss of the power devices
    b. conduction time of diode D_2, i.e., dead-time (T_d) to carrier period ($1/f_c$) ratio
2. Magnetic losses
    a. Core losses for a given inductor
    b. Increased inductor winding ac resistance
3. Auxiliary losses
    a. gate drive loss

The magnetic losses in the inductor greatly affect the boost converter efficiency. Our parallel work on magnetic design aims for minimum magnetic losses, both winding and core losses, to allow a significant efficiency gain.
With the experience on this work, we identified very important analysis stage for efficiency estimation: the ratio between the device losses (switching + conduction), the constant losses of the control

circuits, and the magnetic losses in the power circuit is an essential comparison factor when identifying the feasibility of a topology. For example, if the magnetic components are the major source of losses, then soft switching might not bring any significant efficiency improvement.

This shows the importance of testing different topologies with a fair comparison: having a simpler topology with three variations (T1, T2 and T3) serves exactly this purpose. With topology T3 we will investigate the soft-switching version of the same basic converter topology. It should be emphasized that there are no changes to be made for the control circuit or the gate driver when moving from topology T2 to T3. The additional inductor and diode D3 are plugged to the existing circuit as a separate unit (see Figure 18 and Figure 20).

6.4.3 The Final Design of the full System (2018-2019)

One of the most important goals we set at the beginning of 2018 within this project was to revisit and redesign the autonomous LED lighting system along these five lines:

- efficiency maximization
- increased reliability
- cost minimization
- aesthetics
- interaction with users

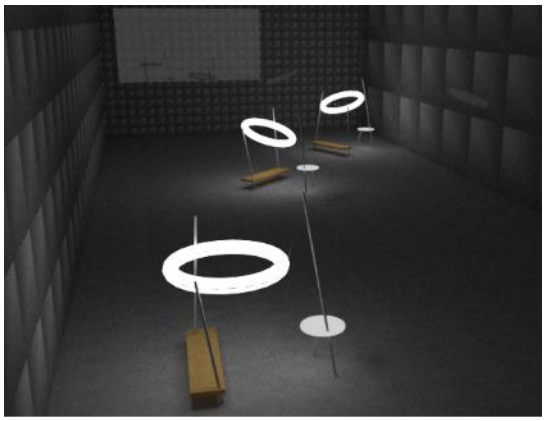


Figure 25: Novel concept of our autonomous LED lighting system.

To this end, we collaborated with the architecture department of EPFL (ENAC) and drastically altered the structure of the autonomous LED light. Considering the system efficiency, simplicity and cost, we decided to place all the solar cell in a single surface on top of the lighting system, in a form of an elliptical shape or even a ring, as depicted in Figure 25. The lighting system can be combined with a bench to attract more people, and enrich unexploited areas in a city, a park or remote areas. The entire ring can be tiled so that the energy harvesting is maximized (considering both the angle of the PV panels with respect to the structure and the inclination of the ring). Another advantage of a closed-loop architecture, such as a ring, is that the thermal management of the enclosed electronics (including the LEDs, the batteries and the converters) is easily implemented with a single source of air flow (e.g. fan).

Another important upgrade on our lighting system is that we now need a single cascaded buck boost converter between the PV cells and the batteries, thus avoiding the use of several converters/modules, as in the previous design of 2017. The same converter can serve different designs (voltage and power levels) with minor changes of its passive components. We also plan to integrate the LED driver in the converter board to minimize complexity, cost and increase the reliability of the entire system. For that purpose we can use a simple constant current driver, like the *TS19601CP5*, with 700mA current capability and up to 70V output withstand voltage. A simple boost converter, with low current requirements can be places between the variable battery voltage and the LED driver input.

At this stage of the project we re-sized all electrical components, as described in the following subsections, but we kept the luminescence and the power of the LED street light as the reference point.

6.4.4 Revised Summary on Daily Energy requirements

Two different estimators of the power consumption of the LED light have been presented in the previous annual SFOE report "*GaN-based Power Electronics for Energy Efficiency Applications*", the conservative power plan and the power-saving plan. The conservative power plan reduces the power of the light to 5% during the night, but for 1 hour the light remains at full power to take into account the motion sensor that will increase the flux to its maximum when a user is passing through. The power-saving plan is way more restrictive with a power reduced to 25% during the peak time and then completely switched off. One hour at full power is also added to account for the sensor. The period of operation in both scenarios is normalised to the full power (100%) of the LED light, as presented Table 6. In the power-saving plan, the LED lamp is estimated to operate for 2.5h during the night, corresponding to 95Wh of energy, while in the conservative power plan, the LED lamp is estimated to operate for 6.3h, corresponding to 247Wh.

Table 6: Estimated usage duration at 100% for both strategies

Strategy	Power-Saving plan	Conservative power plan
Operation at rush hours [h]	1.5	5.3
Operation with sensor detection [h]	1	1
Total time [h]	2.5	**6.3**
Required Power	38W	38W
Energy	95Wh	**247Wh**

6.4.5 Battery Management System

The autonomous LED lighting system is oversized to work with the conservative power plan so we can always switch to the relaxed one if the energy is insufficient. More specifically we set a requirement for five consecutive days of operation without any power income. This leads to a minimum energy storage system (ESS) capacity of $E_{ESS(min)} = 5 \times 240Wh = 1200Wh$.

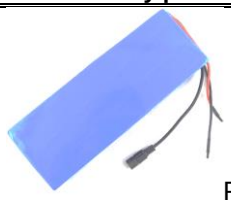
6.4.5.1 Battery selection

We also revisited the batteries technology to make sure we are synced with the current market while ensuring that the system remains lightweight and long lasting. Several alternative battery technologies were considered:

- Lead-Acid/NiCd/NiMH: They offer low energy density at low cost. Considering the capacity requirement of our lighting system, this approach turns out to be undesirable, due to the increased weight.
- Lithium-Ion: They offer high charging efficiency, satisfying specific energy density and they are widely available. On the downside, they exhibit limited maximum number of charging/discharging cycles (approximately 400). Also, lithium-ion batteries use a liquid electrolyte, which make them particularly vulnerable to short-circuits, if misused.
- $LiFePO_4$: lithium-iron phosphate batteries are inherently safer than lithium-ion due to their polymer electrolyte and have more than 2000 charging/discharging cycles capability, while their efficiency remains very good. Thus, despite their limited specific energy density (110 Wh/Kg), we selected this technology for the autonomous lighting system.

A single battery cell is not adequate for medium voltage application due to its low voltage (3.2-3.6V), low capacity and low current. Several cells can be connected in series and/or parallel in a single pack to meet the specifications. However, a problem that one comes across when designing a $LiFePO_4$ ESS is that there is limited manufacturers providing pre-built packs with the required electrical parameters. So, for this prototype we decided to avoid building a custom puck, due to the remarkably high cost, but instead to interconnect several low-cost LiNiCoMn2O4 packs in the right arrangement. Each pack has the characteristics shown in Table 7.

Table 7: Battery pack specifications.



Parameters	Value
Open-circuit voltage	24V
Capacity	10Ah
Standard charging current	2A
Max. charging current	5A
Standard discharge current	10A
Max. discharge Current	15A
Min. Voltage	21V
Max. Voltage	29.4V
Temperature while charging	0 ◦C - 45◦C
Temperature while discharging	-20 ◦C - 65◦C

Lithium batteries should, generally, be prevented from operating lower than 20% and higher than 90% of their total capacity, due to the increased degradation at low and high State of Charge (SoC). In our calculations we assume to use only 70% of their capacity.

In this case the number of battery packs has to be:

$$N_{ESS} \geq \frac{1200Wh}{0.7 \cdot 240Wh\,/\,pack} \rightarrow N_{ESS} = 8\,packs \qquad (0.1)$$

The natural degradation of batteries is not taken into account in this calculation. Even if a battery reaches its End of Life (EoL) (i.e. when 20% of the initial capacity is lost), the light pole can still illuminate unobstructed for 4 consecutive days. Known the nominal voltage of the LEDs and considering the range of operation of our battery packs, we selected a 2S4P (2 packs in series and 4 in parallel) configuration for the ESS. Connecting 2 packs in series increases to ESS voltage to 48V (standardized voltage) that results in higher efficiency of the LED driver due to the low step-up ratio required.

6.4.5.2 Battery Management

Lithium batteries are very compact and effective storage devices and can deliver high currents if needed. However, this comes at a cost: each pack needs to be accompanied by a dedicated circuitry that ensures that all cells/packs are operating within the allowable voltage and current range. These circuits are called Battery Management Systems (BMS). High quality BMSs also regulate the charging process and balance the packs to always be at the same SoC. Since such system are rarely co-packed with the bare batteries, we had to design and develop custom BMSs for our application. The main requirements of our BMS are:

- limit the degradation.
- provide short circuit protection.
- provide under/over voltage protection.
- constantly monitor the temperature of each pack.
- balance all packs to the same SoC.
- share all useful information through an industrial communication link.

But before developing such a complicated circuit, we need to look through the battery's operating principles.

6.4.5.3 Battery Modelling

A battery is an electrochemical device than can produce and store energy. To better understand its operating principles, it is important to establish an accurate equivalent model. Lithium-Ion and $LiFePO_4$ batteries behave the same way, since only the electrolyte differs. It is possible to establish a chemical model, but it is rather complex and not very useful from the circuitry point of view. Thus, an electrical model is preferred even though is less accurate.

A simple way to model a battery is to use a Thevenin equivalent circuit [20]. If the voltage is measured in terms of seconds or minutes, a first order RC model can be used, as in Figure 26(a), in which R_0 represents the losses due to internal defects and $R_1 \cdot C_1$ models the voltage dynamic at the terminal. Although all the chemical reactions inside the battery are temperature dependent, they are not taken into account in the Thevenin's circuit model, for simplicity purposes. Often times the temperature management is considered as a separate problem.

The open-circuit voltage is a function of the SoC, as depicted in Figure 26 (b). Also, when the battery is connected to a load, the actual voltage delivered to the output is smaller than the open-circuit voltage due to the voltage drop on the internal impedance. This impedance is not constant and depends on the current (Figure 26 (b)).

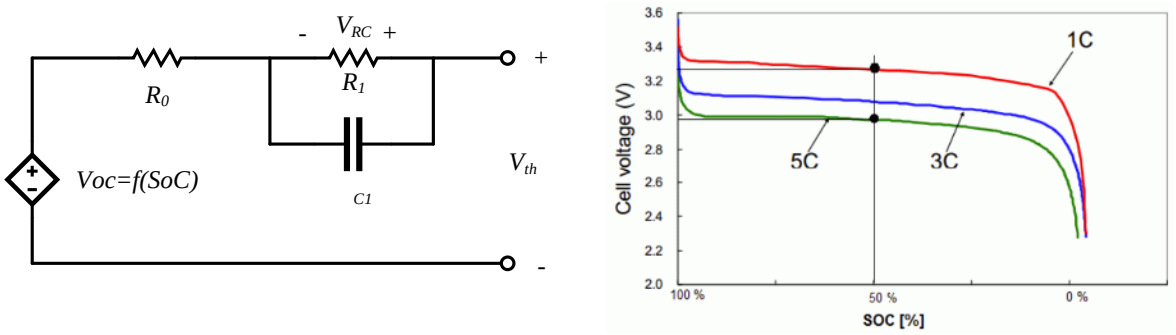


Figure 26: (a) Thevenin equivalent circuit of a battery - first order model. (b) Voltage vs SoC for a single LiFePO4 cell.

6.4.5.4 Battery Balancing

Series and parallel connected cells or packs are always mismatched due to imperfections in the manufacturing process. To get the best performances and limit the degradation the cells/packs need to be balanced and operated at the same SoC. Cells and packs are balanced the same way; each battery has an internal BMS but the packs need an external management.

Series Balancing

In a series connection, the pack with the smallest capacity is the limiting element. Either fully charged or completely empty, the pack gets disconnected, hence the other pack will remain partially charged/discharged. A simple way to address this problem is to provide an alternative path in parallel with the pack. This is normally implemented with a simple high-power resistor, as in Figure 27. In our case, the maximum voltage across the resistor is $V_{BAT\text{-}max}$ = 29.4V and, in order to limit the power dissipation to around 1W, we select a 1kΩ resistor. Thus, the maximal balancing current is $I_{BAL\text{-}max}$ = 29.4mA. The packs needs to be continuously monitored so we can keep them at the same SoC [21].Since the shunt resistor is normally disconnected, a low power, MOSFET (normally off) is used as a switch.

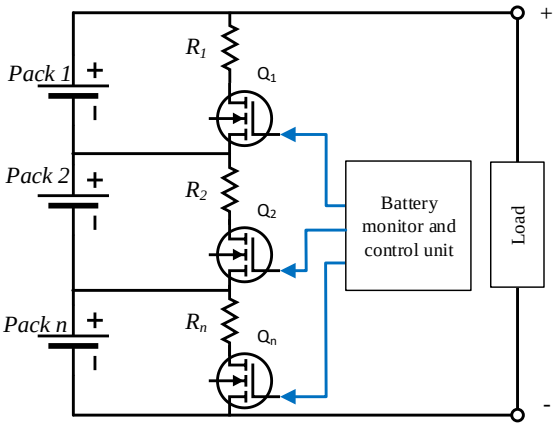


Figure 27: Series balancing topology.

Parallel balancing

In a parallel connection, all the packs have the same voltage. However, if they are not at the same SoC they will have different current levels. In fact, the bigger the difference in SoC, the bigger the current difference. But a higher current means quicker degradation of the battery due to faster heat-up. In the worst case where one of the packs is completely empty/full it won't deliver/accept any more current so the other packs in parallel will have to share the load. Under these conditions, one of the healthy batteries may reaches its current limitation.

In general, batteries in parallel will naturally try to balance themselves, however the balancing currents are not limited. A simple way to limit the balancing current is to connect a small-value power resistor in series to each pack, as in Figure 28. To size the resistor in our configuration, we consider the worst-case scenario, where two fully charged batteries in series are connected in parallel with two more completely empty batteries, so $\Delta V_{BAT\text{-}max} = 2\cdot(V_{BAT\text{-}max} - V_{BAT\text{-}min}) = 2\cdot(29.4V - 21V) = 16.8V$. To limit the power dissipation to less than 5W a 62Ω resistor was chosen. The balancing current is therefore $I_{BAL\text{-}max}$ = 271 mA.

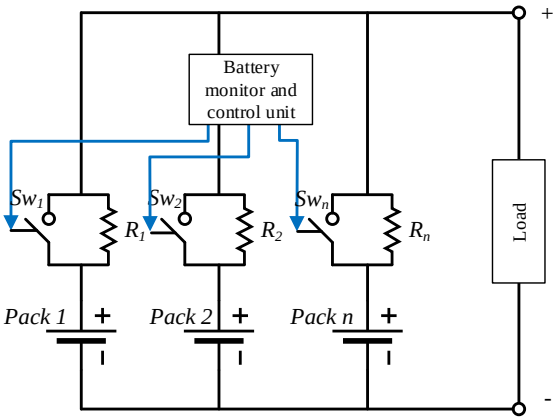


Figure 28: Parallel balancing topology.

Once all the batteries are balanced (at the same SoC) they are expected to stay balanced, since the mismatch in capacity is usually low. It is therefore deduced that the current limitation resistor is not required during normal operation and can be bypassed by a normally-on switch, to avoid unnecessary power dissipation on the resistors.

6.4.5.5 SoC estimation

From the aforementioned analysis, it can be seen that the most critical factor for a successful battery balancing an accurate SoC estimation. An easy way would be to integrate the current over time, also known as the Coulomb Counting (CC) method:

$$SoC = SoC_0 + \frac{1}{C_{cap}} \int_{t0}^{t} i_{bat} dt \quad (0.2)$$

This technique, although simple, it is sensitive to measurement errors. More specifically, in case of an inaccurate current measurement, the error will accumulated over time, which leads to an important drift, especially if the CC counter is not periodically reset. Also the initial SoC has to be precisely determined with another method, since a mismatch on this value cannot be corrected.

A simple way to improve the CC estimation is to use the V-SoC characteristic of the battery. The voltage is continuously monitored and the CC counter is reset to a predefined SoC when a certain threshold is reached (e.g. SoC =100% when $V_{BAT} = V_{BAT\text{-}max}$).

6.4.5.6 Safety Considerations

Thermal runaway

This phenomenon usually occurs in parallel connected battery packs. In more details, if one pack has a higher temperature than the others, its internal impedance will decrease and it will deliver more current to the load. More current means more losses on the internal impedance so the temperature continues to rise, leading to a thermal runaway [22]. If the pack reaches its maximal current it will be disconnected either by the BMS or a protection fuse in series. Still, the other batteries will continue supplying the load with a higher current, which means more power losses and increased temperatures. The whole array can be “lost” due to thermal runaway. It should be highlighted than thermal runaway can occurs both during charging or discharge processes.
The thermal runaway can be prevented in two ways:

- Current limitation: The power resistor introduced for the parallel balancing can be of great importance in limiting the overcurrent due to thermal runaway. However, care should be taken not to exceed the maximum current rating of the series resistor.
- Thermal regulation: a cooling system can be introduced to regulate the temperature of all battery packs. This might be the best way to address thermal runaway, but it increases the complexity and the cost of the entire system.

Over-current

According to Table 7, each battery pack has a current limitation for both the charging and discharge processes. Our BMS has to provide a last-resort protection against overcurrent/short-circuit incidents. This is done by placing a fuse in series with both the charging and discharge ports of each battery pack. The maximal charging current is 5A, while the maximum discharge current is 15A. In reality however, the discharge current should never exceed $I_{LED\text{-}max}$ = 38W/42V = 0.9A. To this end, both charging and discharging ports are equipped with a 5A fuse.

Over/under-voltage

As mentioned earlier a battery should be prevented from operating at a very high or low SoC to prevent excessive degradations. To maximize the life expectancy of our batteries it is highly advised to operate them in a certain voltage range within [21V - 29.4V]. Normally a range of [20%, 90%] guarantees a safe and reliable lifecycle of the battery.

6.4.6 CAN Communication

The communication between the developed BMS boards and the main converter is performed through the industrial rated Controller Area Network (CAN), which is a bi-directional communication protocol.

With this approach the system can be expandable, since multiple boards can be connected to the same CAN-bus. CAN protocol is also able to transmit data over long distances (several meters) at high speed (up to 1 Mbit/s) and has built-in error detection features. Other protocols such as I2C cannot transmit data over long distances. CAN does not use a master-slave hierarchy but we can adopt such a terminology since the DC/DC converter (master) controls everything else. Each board has a TMS320F28035 DSP from Texas Instruments, which is the smallest and most cost effective DSP available with a CAN module.

6.4.6.1 Operating principles

Each device connected to the CAN bus is called a node, as in Figure 29(a). A node has several mailboxes that can be configured for transmission or reception. Each mailbox receives a logical ID (29-bits in extended mode) which is not unique. When a message is sent, the ID is also transferred with it and all the reception mailboxes with the same ID will accept the data (0-8 bytes). This is possible since messages are broadcast on the entire bus instead of using a point-to-point connection.

The CAN protocol requires a transceiver to make the link between the CAN module of a DSP and the bus. There is two reasons for that:

- Bits are represented by a differential voltage to reduce common mode noise (see Figure 29(b)), so the single ended output of the DSP needs to be converted.
- CAN uses an arbitration process with collision avoidance. Each node has to listen to the bus while writing: e.g. if it tries to write a '1' (recessive state) but another node is writing a '0' (dominant state) it loses the arbitration and postpones its message.

The bus consists of 2 lines (CAN High and CAN Low) that are connected to a 120Ω resistor at the two further apart points. By default the two lines are at $V_{DD}/2$ which corresponds to logic '0'. If the differential voltage is non-zero this is a logic '1'. Of course, two additional lines are required to transmit V_{DD} and the ground.

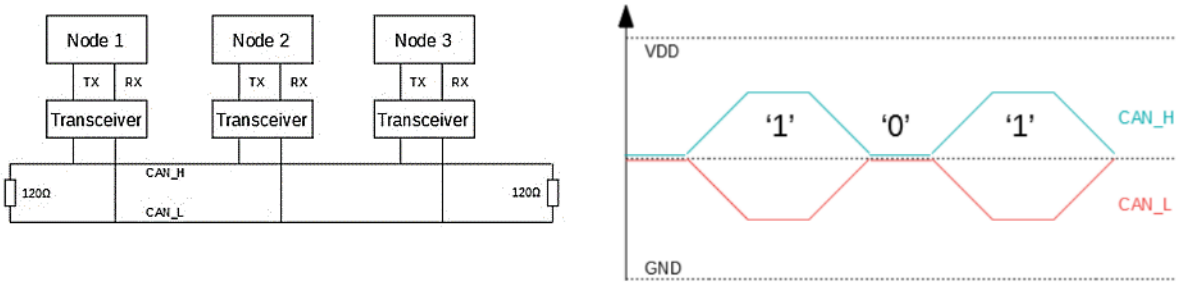


Figure 29: (a) CAN bus architecture and (b) CAN bit representation.

To improve noise rejection we used a shielded and mechanically robust D-Sub 9 cable. The CAN nodes were configured to work at 857.14[*kbits/s*] for high speed communications, as explained in the following set of equations:

$$TQ = \frac{BRP+1}{BaseClk} = \frac{4+1}{60MHz} = 83.33ns \tag{0.3}$$

$$tseg1 = TQ \cdot (TSEG1+1) = 83.33ns \cdot 5 = 416.67ns \tag{0.4}$$

$$tseg2 = TQ \cdot (TSEG2+1) = 83.33ns \cdot 8 = 666.67ns \tag{0.5}$$

$$f = \frac{1}{TQ + tseg1 + tseg2} = 857.14[\text{kbits/ s}] \tag{0.6}$$

6.4.7 Converter Design for the Charging of the Batteries

A GaN-based cascaded buck-boost converter was chosen as the main battery charges from solar power. It is a very simple, efficient and versatile topology that can be used as a buck converter, a boost or a buck-boost. It requires only two transistors and two diodes in an H-bridge configuration.

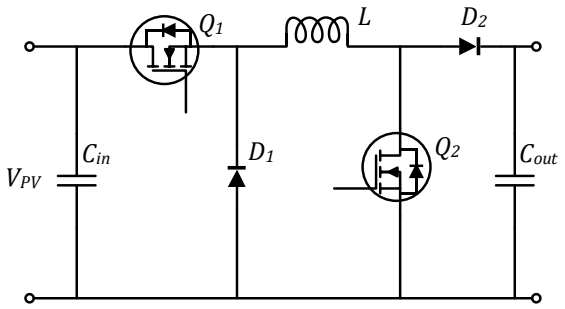


Figure 30: Cascaded buck-boost topology

The idea is to design the PV such that the $V_{PV\text{-}MPP}$ is always smaller than the minimum battery-pack voltage, $V_{BAT\text{-}min}$=42V. This is to avoid feeding energy to the ESS even when the converter in not active. Following this requirement, we can further simplify the converter by removing Q_1 and D_1, and operate it only as a boost converter.

6.4.7.1 Component Selection

The voltage rating of the system allows the selection of low voltage, high current GaN devices, like the GS61008P from GaN Systems, with a breakdown voltage higher than 100V. Their typical on-resistance is 7mΩ, resulting in low conduction losses and in combination with the inherent low switching losses of GaN technology, the need for a bulky and expensive heating is limited. Also, their small footprint allows for a compact circuit design and low weight. The switching frequency of the system is selected to be 150kHz.

Let's consider a PV source of 60 cells in series, forming one string, and 2 strings in parallel with a maximum power of 340W at V_{mp}= 36V (the details for the selection of the PV source will be given later in this report). The nominal duty cycle will then be:

$$D_{nom} = \frac{V_{out} - V_{in}}{V_{out}} = \frac{48V - 36V}{48V} = 25\% \tag{0.7}$$

Let's also allow the current ripple of the inductor to be 10% of its average value.

$$\Delta I_L = 0.1 \cdot I_L = 0.1 \cdot \frac{I_{out}}{1-D} = 0.1 \cdot \frac{P_{mp}}{V_{BAT,nom}(1-D)} = 0.94A \tag{0.8}$$

The inductor value can then be calculated according to the following equation:

$$L = \frac{V_{out} \cdot D \cdot (1-D)}{\Delta I_L \cdot f_{sw}} = 63uH \tag{0.9}$$

In the same manner, we consider a maximum allowable voltage ripple at the output of 1% of the nominal voltage, i.e. 0.48V. The output capacitor is calculated from (0.10).

$$C_{out} = \frac{I_{out} \cdot D}{\Delta V_C \cdot f_{sw}} = 25uF \tag{0.10}$$

6.4.7.2 Finite State Machine – MPPT

The DC/DC converter has to be operated in predetermined states, which can enter with predefined allowable transition actions. This process provides controllability and reliability to the system. In our case the system is governed by the finite state machine (FSM) depicted in Figure 31. All transitions are normally made fully autonomously, but there is also the possibility of manual commands for debugging purposes.

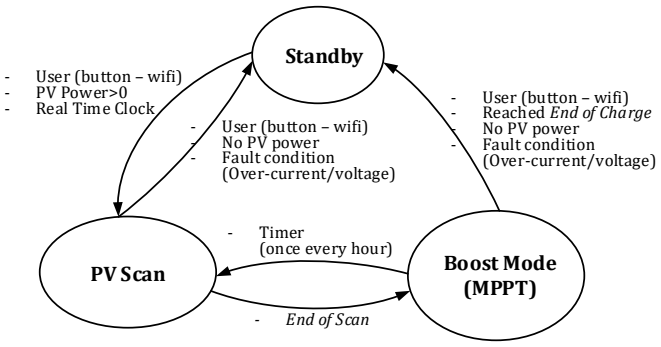
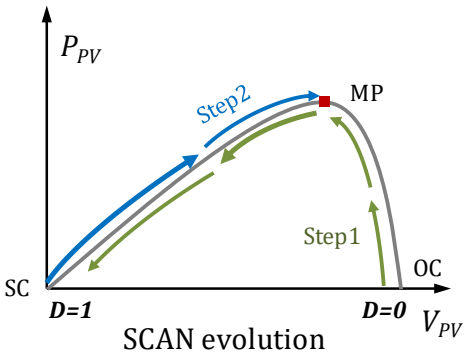


Figure 31: Finite State Machine diagram for the boost converter.

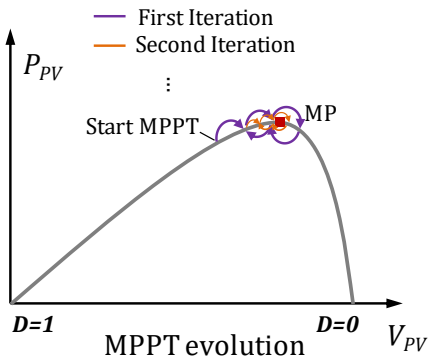
More specifically, the "*Standby*" describes the state where the converter is not charging the batteries (e.g. night time), there is no power transfer and all the devices are off. However, the system keeps monitoring the analog signals to decide for a new transition.

Once the system has detected that there is enough power to feed to the batteries (e.g. daytime - morning), a scanning of the entire PV curve is performed to find the MPP, called "*PV Scan*" and described in Figure 32(a). The scanning process is completed, and the converter returns controllably to the point of maximum extracted power. The next step is to enter the "*Boost Mode*" where a perturb and observe algorithm (P&O) always tracks the MPP. From either the "*PV Scan*" or the "*Boost Mode*" the system can return to the "*Standby*" mode if an over-current over/under-voltage or over-temperature is detected.

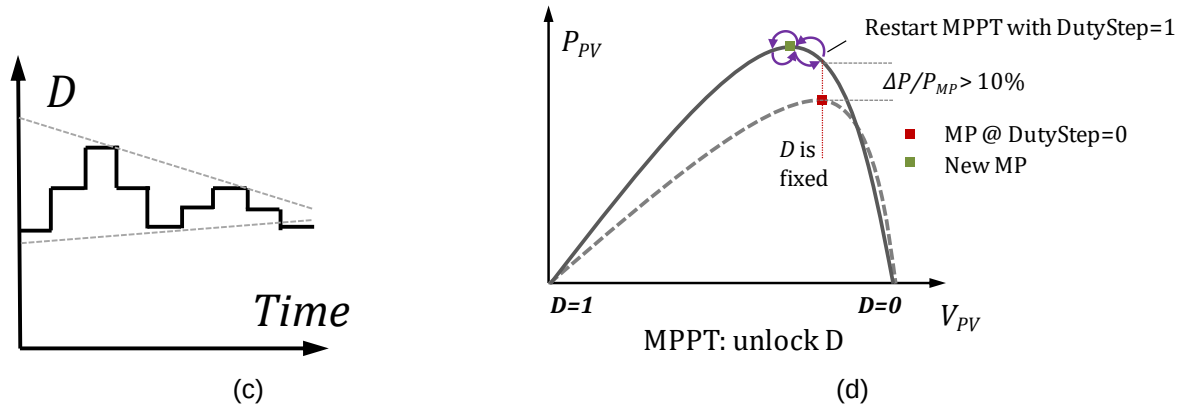
It is worth noting a modified MPPT algorithm was implemented to maximize the efficiency of the system and minimize the power ripple. In more details, the system has the ability to detect perturbations around the MPP and reduce the duty cycle step, until it is locked to a fixed value. This operation is graphically illustrated in Figure 32(b and c). The algorithm can unlock the duty cycle and continue normal P&O operation once the new measured power defers from the locked one by 5%, which is a reflection of a change in the environmental conditions (irradiance or temperature), as shown in Figure 32(d).



(a)



(b)



(c) (d)

Figure 32: Description of the scanning process on a P_{PV}-V_{PV} graph.

The entire control has to be faster than the time constant of the batteries charging process and the rate of change of the lighting conditions, which both changes very slowly in time (in the range of a few sec). So the control frequency was selected to be 1kHz.

6.4.8 PV Generator

We have already established that a battery capacity of 1200Wh is capable of suppling the load for 5 consecutive nights. But we haven't yet discussed how long will it take for the PV source to charge the storage system. This investigation will lead us to determine the power rating of the PV generator.

The minimum requirement for the PV source is to be able to deliver the same power that the LED light consumes during the night with the conservative power plan. And that power should be produced even during December, where the irradiance takes its minimum value.

$$E_{day-\min} = 240Wh \tag{0.11}$$

To make our system even more reliable we require the PV generator to be able to fully charge the batteries within three days. That means that each day the system needs to produce the energy for the next night and some more to accumulate for 4 additional nights.

$$E_{day} = 240Wh\frac{4}{3}240Wh = 560Wh \tag{0.12}$$

Now, depending on the PV technology and the inclination of the solar panels, different number of cells will be required. The most realistic scenario is to consider monocrystalline PV cells that exhibit very good efficiency (typically 17%), have relatively low cost (0.7CHF/W) and are widely available. In this case the required energy from the sun light is E_{sun} = 560 Wh / 0.17 = 3300 Wh. For the inclination we will consider the simples placement ($\theta = 0^o$) and the best case for December, where $\theta = 66^o$. For these two alternatives the required surface is:

$$PV_{Surface} \in [\frac{3300Wh}{1900Wh/m^2}, \frac{3300Wh}{1000Wh/m^2}] = [1.7m^2,\ 3.3m^2] \tag{0.13}$$

Given that the active area of a single monocrystalline PV cell is typically 125mm x 125mm we can calculate the number of required cells:

$$N_{PV} \in [110,\ 210] \tag{0.14}$$

We can, thus, consider to have 120 cells of 2.8 W/cell and 0.6 V_{mp}/cell. The best way to organize these cells is to connect them in series to increase the overall PV voltage so as to be close the

batteries charging voltage: 60 cells in series, forming a PV string and 2 strings in parallel. The total power in standard test conditions (STC) will be 340 W and the MPP voltage 36 V.

6.4.9 Experimental Results

All electrical components of the autonomous LED lighting system were tested, for the first time, in real conditions, with the experimental setup of Figure 33.

We used a high efficiency HIT PV source of 250W nominal power at STC, the DC/DC boost converter connected to two BMS boards through CAN protocol and the 8 battery packs in a 2S4P configuration. The charging port of each battery is connected to the output of the boost converter and the discharge port is powering all three PCBs and feed the LED lighting. At this stage, we used only a single LED driver IC to control the illuminates of the LED strip (48V, 34W, 146 lm/W) via a PWM signal from the main microcontroller of the DC/DC converter.

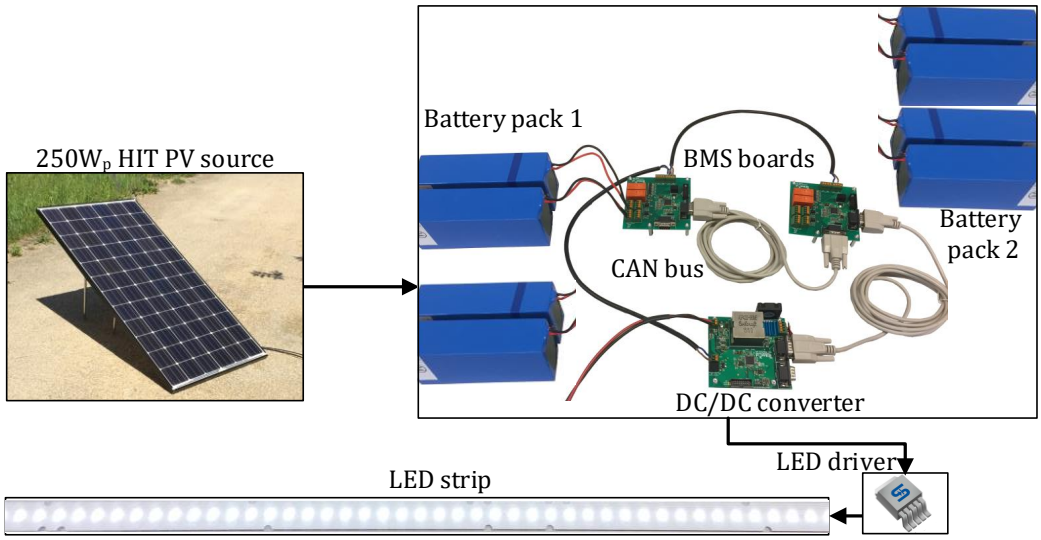


Figure 33: Complete electrical structure for the autonomous LED lighting system.

6.4.9.1 DC/DC converter

The performance of the developed buck-boost converter was initially validated in the experimental setup presented in Figure 34(a). The power input was provided by a controllable constant voltage source and an electronic load with a fixed voltage at 48V emulating the battery array. The input and output voltages and currents were continuously monitored both trough a 300MHz oscilloscope and the on-board microcontroller and transferred to a PC via a JTAG protocol. These measurements are depicted in Figure 34(b) and (c) when the transferred power was 150W, with V_{in} = 31V and V_{out} = 48V. The converter exhibits a remarkable efficiency of 96.2%, much higher than the previous version (Flyback converter) presented in the 2017 annual report "*High-efficiency power converters for potentially-large energy-savings applications*".

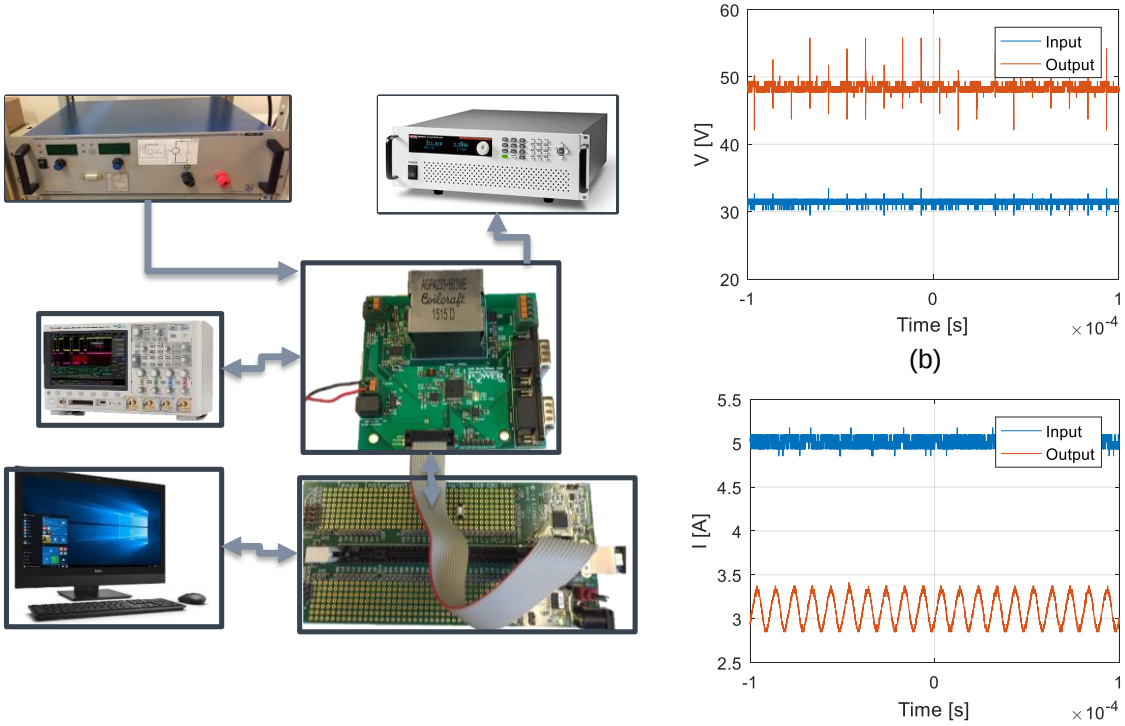


Figure 34: (a) Experimental setup for validating the performance of the DC/DC converter. (b) Input and output voltage and (c) current measurements. *P* = 150W, V_{in}=31V, V_{out}=48V, *n*=96.2%

We first tried to operate the circuit without any external cooling system and observed that the GaN transistors remained in an acceptable operating temperature as a result of their great switching performance and low conduction losses. On the other hand, the series diode of the boost converter soon exceeded 90°C, as can be seen in Figure 35(a). To this end, we chose to place a small heatsink, with a thermal resistance of 16°C/W, on both the output diode and the GaN transistor. A small fan, with just 13 m^3/h, can also be added to lower the temperature even more at nominal power, as illustrated by the thermal image of Figure 35(b).

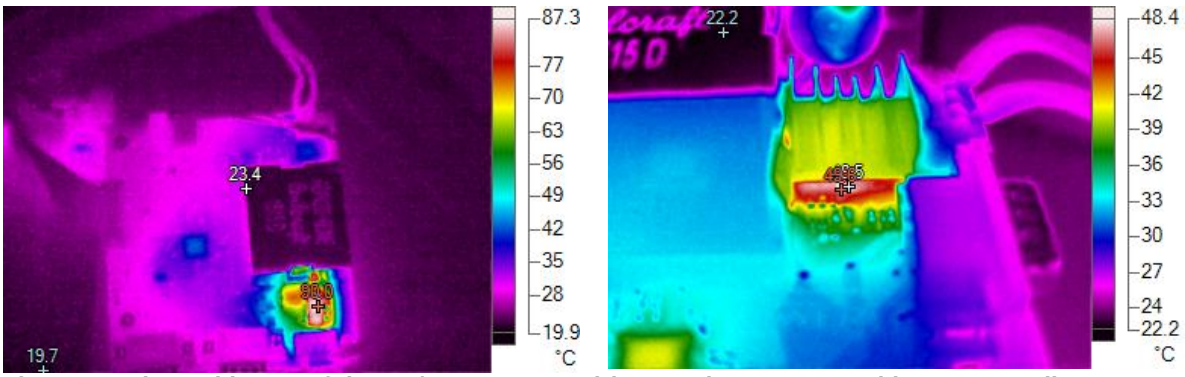


Figure 35: Thermal image of the DC/DC converter. (a) Operation at 150 W without any cooling system. The diode of the boost converter heats-up to 90°C. (b) Operation at 300 W with additional heatsink and forced air cooling at 13 m^3/h.

Having experimentally verified the exceptional performance of our DC/DC converter prototype, we then proceeded with the full-scale experiment under real conditions. We replaced the voltage source with a 250 W_p HIT PV panel and we tested, for the first time, all functionalities of the system (including start-up procedure, PV scan operation, MPPT algorithm, shut-down procedure).

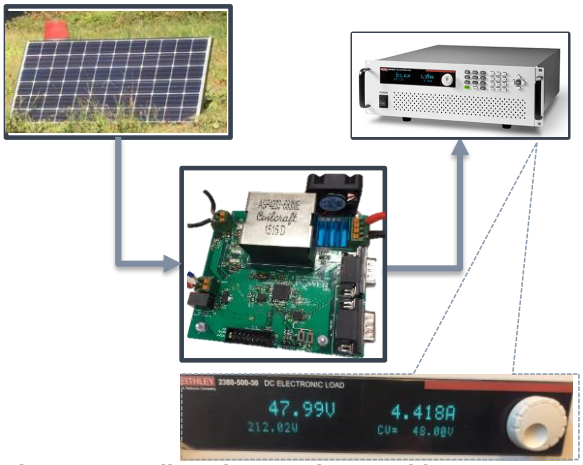


Figure 36: Full scale experiment with a 250W HIT PV. Pmp=210W, Vmp=41V, Imp=5.1A, Vdc=48V.

After a successful scanning of the entire PV curve the system locks to the maximum power point, which, at the time of the experiment was P_{mp} = 212 W at V_{mp} = 40 V. With the output voltage fixed at V_{BAT} = 48V, the duty cycle at MPP was d_{mp} = 18%. Due to the relatively high input voltage of the HIT PV and, consequently, the low duty cycle, the thermal performance of the circuit was impressive, with the highest recorded temperature not exceeding 31.5°C, as can be seen in Figure 37.

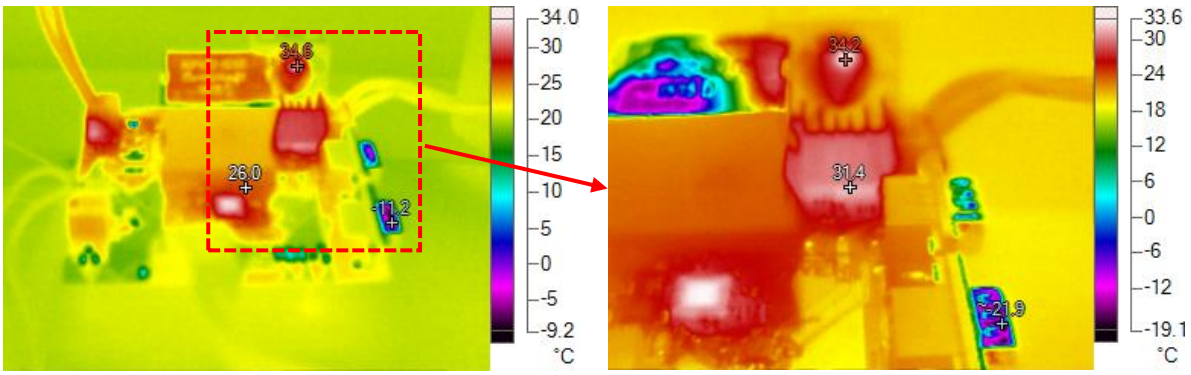


Figure 37: Thermal image of the DC/DC converter operating in real life conditions with a 250 W HIT PV. (a) The maximum temperature of the board doesn't exceed 31.5°C.

In real life conditions the irradiance is not always uniform over the PV source. We believe it is of paramount importance to evaluate the operation of our system under shading conditions. To this end, we partially shaded the HIT PV panel and recorded the power and duty cycle. Since all solar cells are in series in this commercial PV panel, shading half of the panel results in a dramatic reduction of the power output. Indeed, the power dropped from 210 W to only 10 W and the duty cycle from 19% to just 2%. The modified P&O algorithm could effectively unlock the duty cycle and track the new MPP. Once the shading was removed the MPPT locked successfully to the old MPP with minimum power ripple.

Also the system can safely be shut-down, either by the user or due to a fault condition. In our experiment we used an external signal to interrupt the normal MPPT operation. The converter "goes" directly to "*Standby*" mode and the power reduces from P_{mp} = 210 W to 65 W, which is the crossing point of V_{BAT} = 48V with the PV curve.

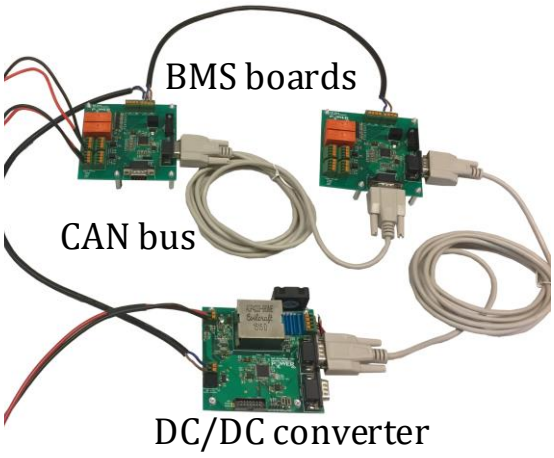
6.4.9.2 Battery Management System

Two BMS board where developed to manage the eight in total battery packs and are connected with the buck-boost converter through CAN bus (see Figure 38(a)). Each BMS monitors the temperature,

voltage and current measurements, as well as the SoC of all connected batteries. It is also responsible for controlling the series balancing between the batteries. In return, the DC/DC converter sends a single to the BMS boards indicating if and for which pack the parallel balancing should be activated.

We first tested the *unidirectional CAN communication*, i.e. the BMS sends a simple message to the DC/DC converter. An effective transmission was observed through the Code Composer Studio platform, and more specifically the real time debugging tool, Figure 38(b). We then proceeded in establishing a successful *bidirectional CAN communication*: the converter was sending a single message to each BMS board and they were sending back only a single temperature measurement to the master board. As can be observed in Figure 38(b), the converter is correctly transmitting and receiving data. It uses mailboxes 0 and 1 for transmission and mailboxes 16 and 24 for reception (respectively for BMS_1 and BMS_2).

The last step for finalizing the CAN communication was to realize a **real-scale test**. The DC/DC converter sends a message to each BMS slave board (command signal for parallel balancing operations), while each BMS board sends 8 messages (voltage, current, temperature measurements and SoC for each battery pack). Since the number of transmitted messages was high and CAN algorithm was updated once every 1ms (synchronized with the ADC conversion frequency), we had to reduce the CAN update frequency to 250Hz and increase the bus speed to 853 [kbit/s]. This way we manage to establish a successful communication with all the different subsystems.



(a)

Variables | Expressions | Registers

Expression	Type	Value
CAN_Node_Status	struct CAN_NODE_STATUS	{FormError=0,BitError=0,Stu...
FormError	unsigned int	0
BitError	unsigned int	0
StuckError	unsigned int	0
ChecksumError	unsigned int	0
StuffBitError	unsigned int	0
AckError	unsigned int	0
BusOffError	unsigned int	0
PassiveError	unsigned int	0
WarningStatus	unsigned int	0
SuspendStatus	unsigned int	0
CCEStatus	unsigned int	0
PowerDownStatus	unsigned int	0
ReceivingStatus	unsigned int	1
TransmittingStatus	unsigned int	1
CAN_TEC	unsigned long	0
CAN_REC	unsigned long	0
ECanaMboxes.MBOX0.MDL.all	unsigned long	0x3E0C3747 (Hex)
ECanaMboxes.MBOX0.MDH.all	unsigned long	0x3DFE6A49 (Hex)
ECanaMboxes.MBOX1.MDL.all	unsigned long	0x3DFE6A49 (Hex)
ECanaMboxes.MBOX1.MDH.all	unsigned long	0x3E092BC8 (Hex)
ECanaMboxes.MBOX16.MDL.all	unsigned long	0x3C821FB8 (Hex)
ECanaMboxes.MBOX16.MDH.all	unsigned long	0x3C964DC9 (Hex)
ECanaMboxes.MBOX24.MDL.all	unsigned long	0x3C92C5D2 (Hex)
ECanaMboxes.MBOX24.MDH.all	unsigned long	0x3CAE201C (Hex)
ECanaRegs.CANRMP.all	unsigned long	0x00010000 (Hex)

(b)

Figure 38. (a) Connection of the two BMS boards and the DC/DC converter. (b) Real time debugging of the CAN communication through Code Composer Studio.

6.4.10 Summary and Outlook

We have demonstrated efficient converters based on GaN devices that enabled the development of a fully autonomous LED lighting system. Both hardware and software were evaluated under real operating conditions. Our main achievements are listed below:

- Development of a generalized buck/boost GaN converter with an efficiency >96%. Its input and output operating voltage are between 0V – 100V and the rated power is 350W. The simplicity of this circuit has a decisive effect on the cost and reliability of the system.
- Demonstration of fully functional battery management system. This achievement was of great importance for the safe operation (charge/discharge) of the energy storage system. Each board can regulate up to 4 batteries and can continuously monitor their voltage, charging and discharging current as well as their temperature. The developed BMS board also provides balancing of the different battery packs and prevents their degradation. That results in increased reliability and long life expectancy of the system.
- We selected an efficient, on-chip LED driver that can control the illumination of our lighting system with a simple PWM single from the microcontroller.
- A stable, industry rated CAN protocol was implemented for the communication of the different components of our system. The flexibility of this protocol allows expanding our design with more (or even less) BMS boards. Also built-in error detection feature allows reliable communication even in long distances.
- A sophisticated control structure based on a simple finite state machine was adopted. The controller ensures safe system operation under any conditions (start-up, normal operation-MPPT, shut-down, fault, etc.)

6.5 GaN-Based Micro-Converters for Harvesting Maximum Energy from PV Panels with High Conversion Efficiency

6.5.1 Introduction

Despite having a sun exposure comparable to that of Belgium and Germany, solar energy occupies only 1.7% of Swiss electricity production; this rate is 4.7% and 6.1% for Belgium and Germany respectively [23]. Swiss Energy Strategy 2050, provides a huge motivation in terms of investments in photovoltaics. With the rapid development of renewable energy sources (RESs), low voltage dc (LVDC) microgrid has better performance to integrate different RESs and energy storage systems (ESSs). Being mostly dc sources, with their uncertain nature and intermittent characteristics of renewables such as solar irradiation, clarifies the importance of having efficient converters for harvesting more energy in such microgrids. GaN promises improvement in efficiency, size, and overall converter performance, especially while discussing about LVDC (<1kV). To take the advantage of the opportunity here, a target was defined to design a DC-DC mirco-converter for direct connection of a standard PV panel (20~40 V and 10 A) to a DC grid. The converter tracks the maximum power point (MPP) of the PV panel, ensuring the maximum energy harvest from the PV panel. The design also took advantage of high switching frequency allowed by GaN semiconductor, for achieving a smaller size of the converter. GaN provides potentials, but it requires a comprehensive study, analysis and design in order to make the most out of what it offers. In the following parts we cover these aspects (choice of topology, design of magnetics and some control aspects).

6.5.2 Analysis and Implementation

From the power system point of view, PV panel operation has several challenges. An important issue with traditional utilization is the partial shading, the condition in which all the PV panels are not receiving equal irradiation from the sun, shown in Figure 39. This is a problematic scenario, since the PV panels are put in series to increase the voltage level to a required value by a grid-connected inverter. In this scenario, the panel with the minimum irradiation defines the current of the whole string, resulting in a drop of harvested energy. Dedicating a micro-converter that is able to track the maximum power point (MPP) of each panel is going to be a perfect match for this application. If the converter is able to provide the high voltage step-up, it could directly connect a PV panel to a DC bus; while still having the freedom to use an inverter for connection to an AC-grid. This concept, shown in Figure 40 is proven to compensate up to 30% of PV losses, by providing the local MPPT [24]. The converter design from the power electronics point of view shall achieve requirements listed in Table 8.

Figure 39 Partial shading leads to a huge reduction of energy harvest, which can be avoided by use of micro-converters dedicated to each panel.

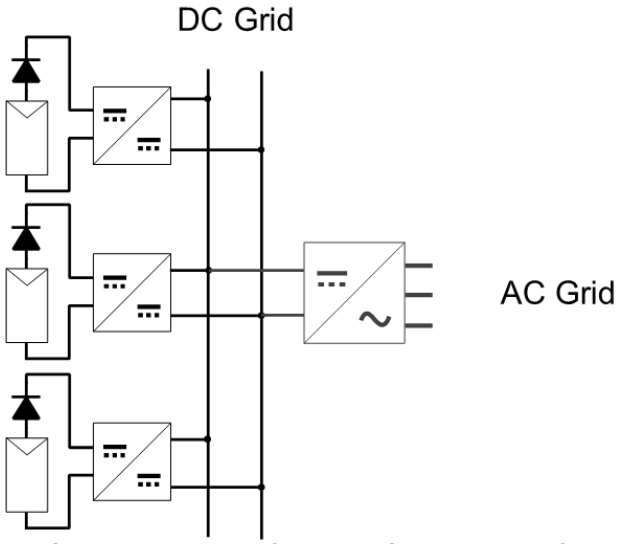


Figure 40 Concept of DC-DC micro-converter for harvesting maximum energy of a PV power system.

Table 8. Specifications of the designed converter.

Parameter	Value
Rated Input Voltage	33 V
Max. Input Voltage	40 V
Max. Input Current	10 A
DC BUS Voltage	350 ± 10%
Switching Frequency	300 kHz

6.5.3 Investigation of Appropriate Topology

There are two categories of DC-DC converter topologies: isolated, and non-isolated. Non-isolated topologies include the boost converter and its various derivatives, which in summary would suffer from low efficiency due to the switching losses, increased at high voltages and diode's reverse recovery current. There are also other types of converters based on voltage multiplication, which have the drawback of limited controllability of the output voltage. In this context the isolated topologies could be a great candidate, especially while there is such a huge difference between input and output voltage levels.

Isolated DC-DC converters usually employ a high-frequency transformer. This high-frequency transformer solves the problem of high step-up voltage by adjusting the number of primary and secondary winding turns. Having this in mind that topologies which inherently have the advantage of soft-switching are necessarily preferred over hard-switched topologies (this is also depending on the application in which the converter is used), which lead to high switching losses and therefore lower efficiencies. Especially GaN transistors have lower $R_{ds(on)}$ compared to other switching devices, which leads to lower conduction losses. A combination of soft-switching topologies (for removing switching losses) and reduced conduction loss of GaN devices, makes us capable of achieving higher efficiencies.

Here at POWERlab, we investigated several topologies, as is shown in Figure 41:

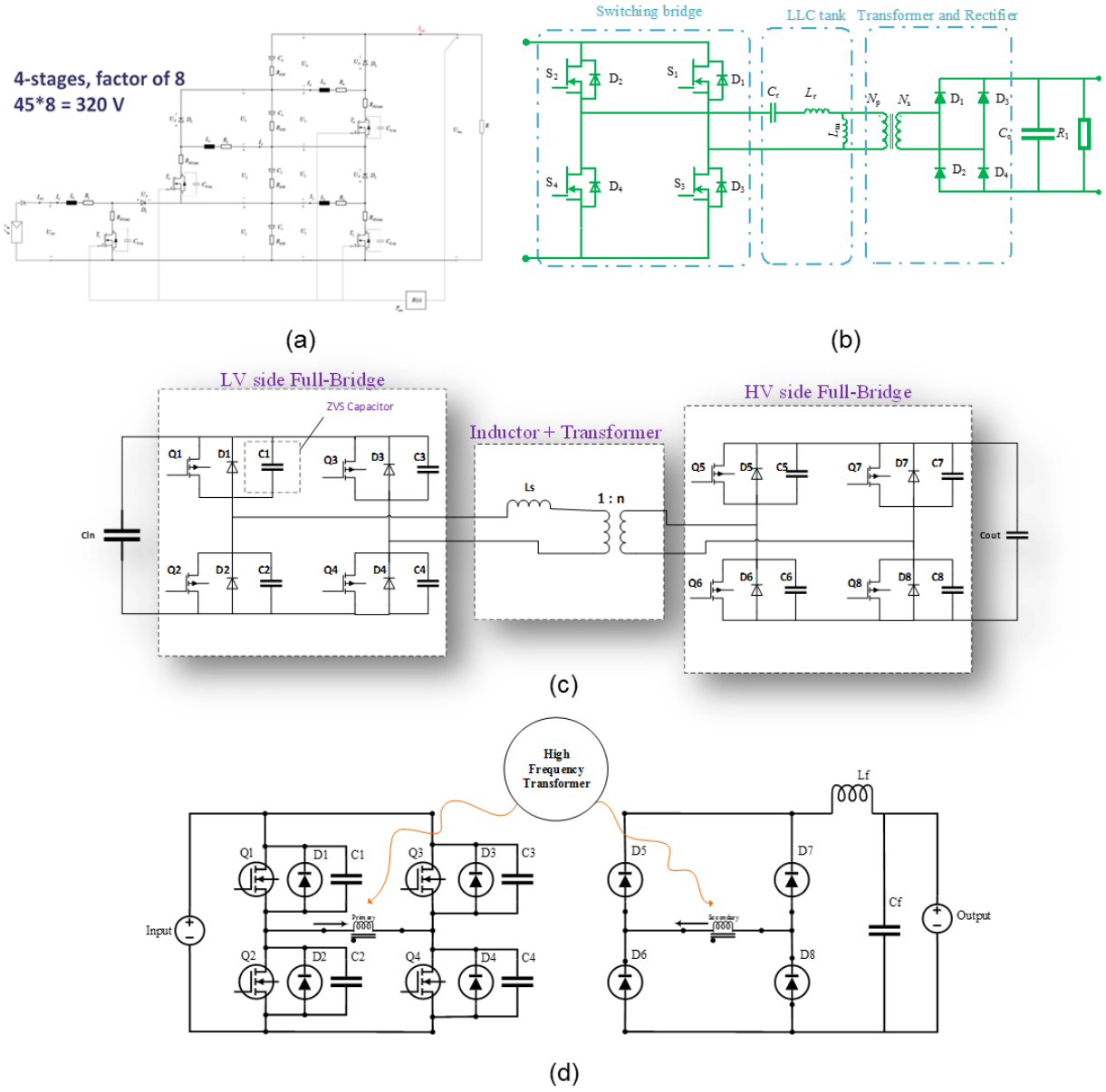


Figure 41 Investigated micro-converter topologies (a) Multi-stacked boost Converter (b) LLC Resonant Converter (c) Dual Active Bridge Converter (DAB) (d) Phase-Shifted Full-Bridge Converter (PSFB)

As it can be seen in Figure 41, we are interested in using topologies which enable higher power ratings as well as soft-switching to minimize the losses. Topology (a) suffers from hard-switching and higher losses. The other three topologies have the advantage of a galvanic isolation between two voltage levels, and require the utilization of a high frequency transformer. Furthermore, they also benefit from Zero Voltage Switching (ZVS) which is a method for soft-switching.

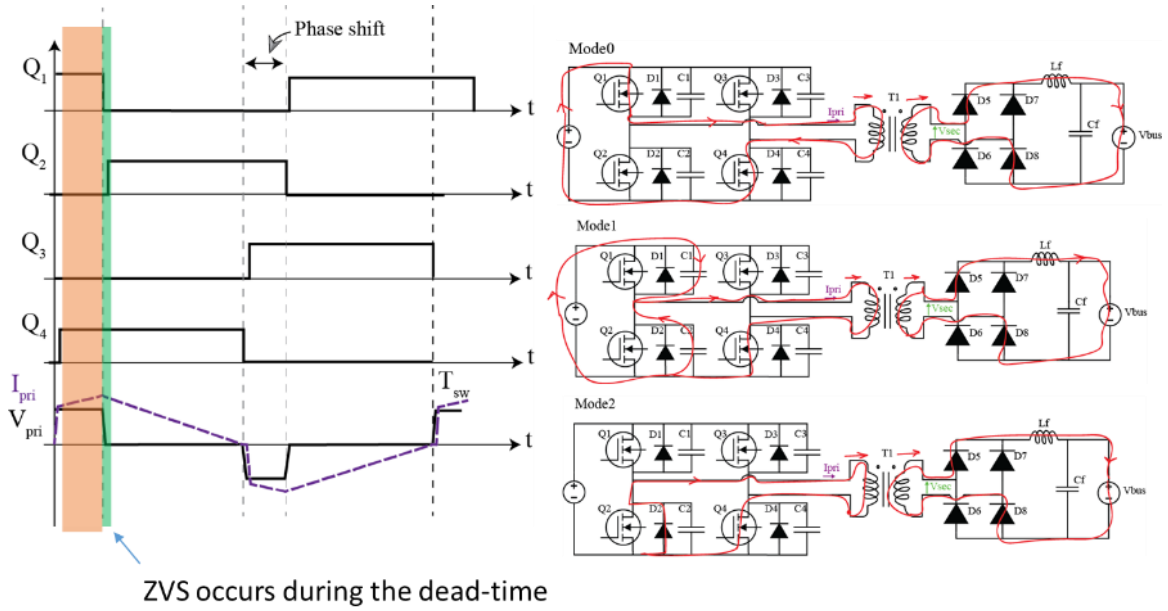
Discussing about topology (b), it is a variable frequency LLC resonant converter [25][26], and hence the modulation is frequency based and has some challenges compared to the conventional PWM modulation. Furthermore, for utilizing the best performance out of magnetics, which here is the high step-up transformer, it is a priority to have fixed frequency.

Topology (c) is a Dual-Active-Bridge (DAB) which utilizes the high frequency transformer, as well as two full-bridges, for primary and secondary. It has the ability to transfer power in both directions (which is an ideal topology for HVDC converters on larger scales). For this application, bi-directional power transfer is not needed. Considering the increased number of switches and the complex controllability of this converter, makes it not the ideal choice for this application. For later applications and migration to higher powers, higher voltages, this topology is considered a good choice.

Finally, topology (d), which is called Phase-Shifted Full-Bridge converter [27], we have almost all the advantages we are looking for. Modulation is based on phase shift with fixed frequency. Also, it supports ZVS, enabling us to lower the switching losses, and also it is isolated.

A phase-shifted full-bridge (PSFB) topology was therefore chosen to realize the DC-DC conversion in a single stage topology. Relatively simple control and the ability to realize a high step-up in the voltage are the strong points of this approach.

As achieving a compact size was a priority of the design, a high switching frequency of 300 kHz was chosen. At these high switching frequencies, the efficiency of the converter starts to degrade, as a direct result of switching losses. To address this problem, two solution was proposed by the designer. A first one was to minimize the switching losses by using a topology that allows for soft-switching. This is a technique that significantly reduces the losses during the switching transition of a semiconductor, by shifting the overlap between transition of voltage and current of a device. The nominated PSFB topology inherently achieves soft-switching [27]. The operation of the topology for zero-voltage switching (ZVS) is illustrated in Figure 42. In Mode0, switches Q1 and Q4 are on, charging the leakage inductance of the transformer. In Mode1, Q1 is turned off, to make the condition ready for Q2 turn-on. This period is also known in power electronics as the dead time. During this period, marked with green in Figure 42(a), the output capacitance of the switch Q2 is discharged, and the voltage is reduced to zero. In case of extended dead time, the antiparallel diode D2 conducts and keeps the voltage close to zero. Then the gate signal command is issued to turn Q2 on, with zero voltage.



(a) (b)

Figure 42 (a) Switching transition of Q2; Gate drive signals for Q1 to Q4 and (b) operating modes of PSFB topology

The most challenging part of the design, was design and manufacturing of the high frequency transformer, responsible for achieving the step-up in the voltage. The transformer is also very important as its leakage inductance together with output capacitance of the switches allow for ZVS. Several finite element analysis (FEA) was performed, to structure the layout and arrangement of the windings in the transformer. The transformer achieved the requirements of the design, and its characteristics are listed in Table 9.

Table 9. Specifications of the high-frequency transformer.

Parameter	Value
Turns ratio (N_p:N_s)	5:60
Core	PQ 32/20 and PQ 32/30 N95
AC resistance (from primary side)	27.5 mΩ
Leakage inductance (L_r)	215 nH

6.5.4 Design of Magnetics

As mentioned before, the transformer has a critical role in this design: it is responsible for the high step-up in the voltage level as well as providing the isolation between primary and secondary. Also, its leakage inductance in combination with a series inductor helps the converter to achieve ZVS.
Considering the design specifications, we tried first to purchase the transformer from other companies who have the master technology in design of magnetics. As a disappointment, none of them could manufacture the custom design for us, or at least they needed us to ask for a huge number of quotes before they start the design. This is not reasonable for the prototyping phase in which we want to test the design and evaluate its performance. It did not set us back from going for what we had in mind, and we started to design the transformer.

Our priorities in the design were: high step-up ratio, small size, and efficiency. Having this in mind, the study, simulation and analysis of magnetics was started.

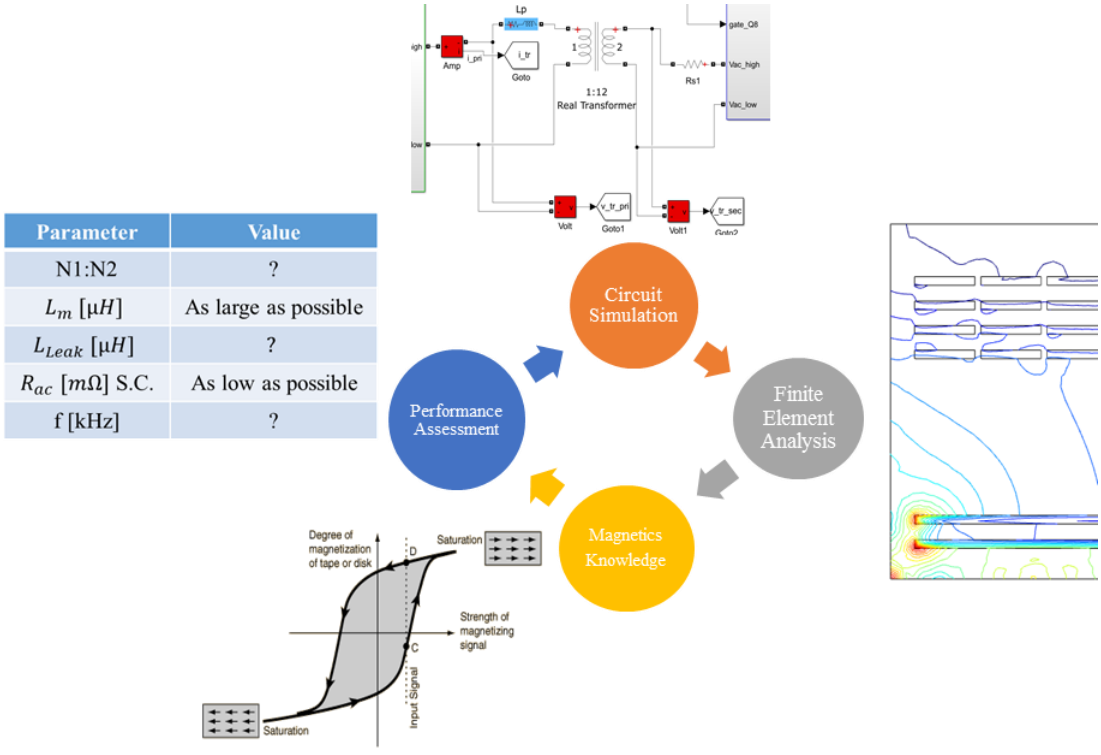
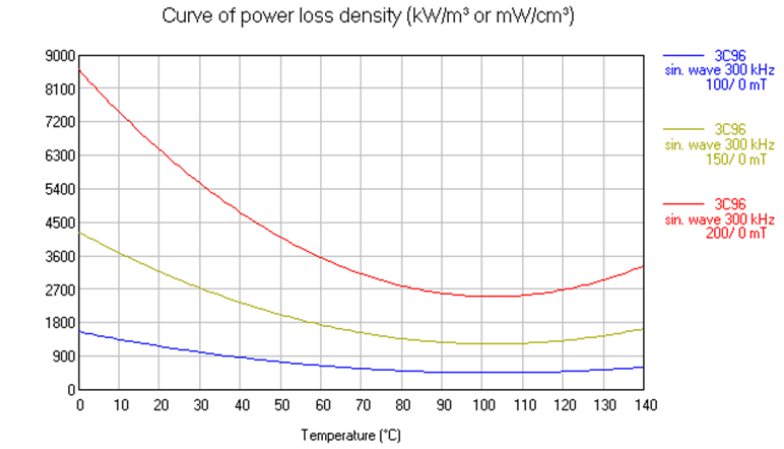
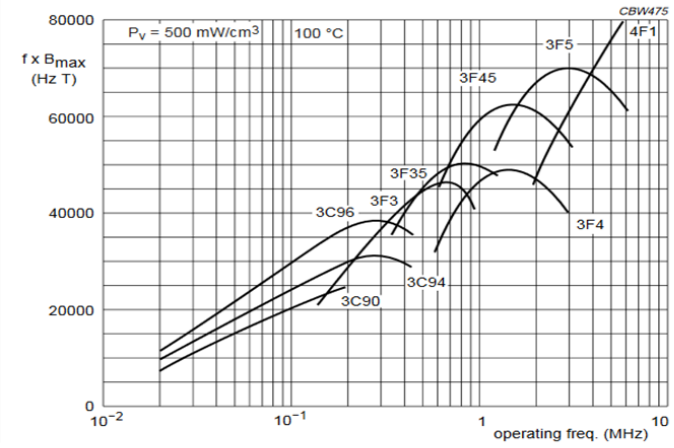


Figure 43 Iterative approach for the design of magnetics (transformer and series inductor)

Figure 43 illustrates our approach for solving the magnetics optimization problem in the design. It is and iterative approach in which knowledge of magnetics, as well as finite element analysis and simulation tools help us to reach the performance goal for the magnetic design.
Looking at current magnetic materials technology, they only allow for small magnetic field densities (indicated with *B* in literature) in high frequency applications, and it is a limitation for designing high frequency high performance converters. This in turn shows the importance of a well design for having the lowest possible losses, because as the magnetic field density in the core increases, so do the core losses. Figure 44 **(a)** shows the core loss density of material C96 from Ferroxcube © [28] under three different magnetic field densities and various temperature. As it can be seen, for a 300 kHz waveform, doubling the value of *B*, will result in much higher losses in the core than only twice. Also Figure 44 **(b)** illustrates that different magnetic materials show different characteristics and therefore a knowledge of magnetics is a necessary step toward designing the high frequency power electronics converters, and in this case, micro-converter for PV panels.



(a)

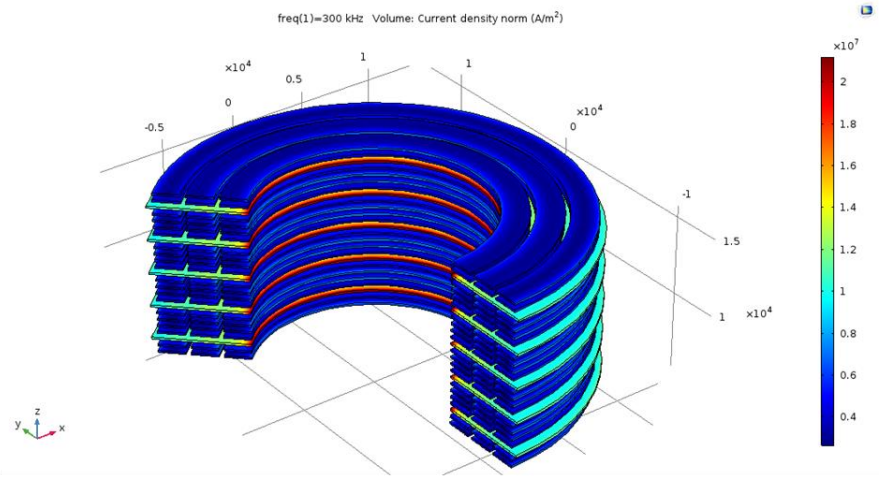


(b)

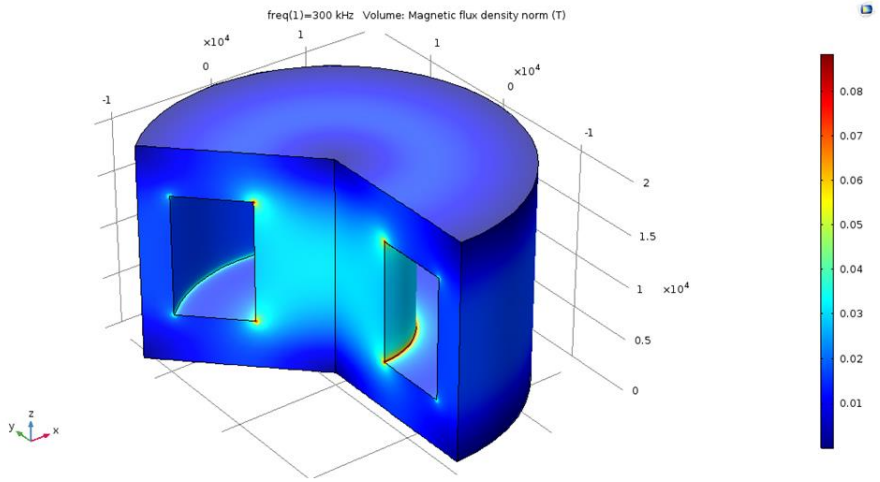
Figure 44 Study of magnetic components: (a) Curve of power loss density vs. temperature with *B*= 100 mT, 150 mT, and 200 mT for 3C96 material from Ferroxcube for 300 kHz frequency wave form. (b) Figure of merit (*f* x B_{max}) for different magnetic materials from Ferroxcube. Each material is well suited for a specific frequency, and magnetic field density, which translates into voltage

Using finite element analysis software, in this case COMSOL Multiphysics, help us to investigate the distribution of magnetic fields inside the core, and have an estimation of the inductance and resistance of the magnetics in high frequencies [29].

Our target frequency is 300 kHz, which results in reduced size of magnetic components, while considering the limitation in the magnetic materials as mentioned before. For satisfying the high step-up ration of the transformer, a turn ration of 5:60 was chosen for avoiding the core to be saturated. Furthermore, for reducing the AC resistance, due to the well-known “skin effect” and “proximity effect”, an interleaved architecture was selected. Figure 45 illustrates the Finite Element Analysis (FEA) simulation of the designed transformer in COMSOL Multiphysics:



(a)



(b)

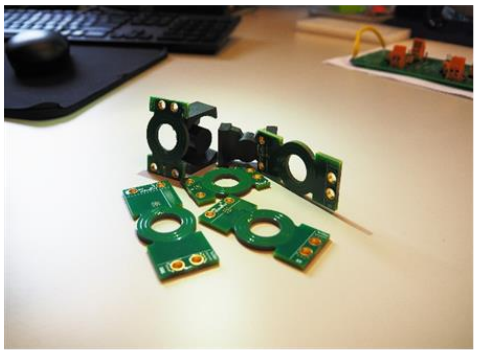
Figure 45 FEA simulation of the planar transformer in COMSOL Multiphysics: (a) Current density norm in the primary and secondary windings under short-circuit test of the transformer (primary current is 10A and secondary windings are shorted), (b) Magnetic flux density norm under open circuit test condition in the transformer (primary voltage peak is 40V 300 kHz sine wave form and secondary windings are open).

The test results from COMSOL simulations in Figure 45 is illustrated in **Table.10**:

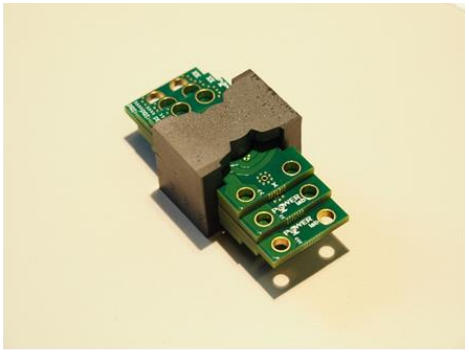
Equivalent AC Resistance from Primary Side (Rr)	**17.826 mΩ**
Leakage Inductance (Lr)	**15.73 nH**
Magnetizing Inductance (Lm)	**258.75 µH**
frequency	**300 kHz**

Table.10: Simulation results from transformer's short circuit and open circuit tests

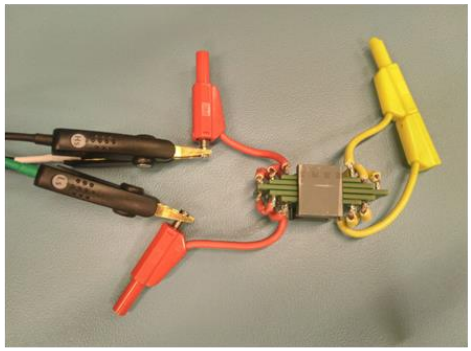
After this initial evaluation, we built a prototype based on the design. **Figure 46** shows the planar transformer. Planar transformers have the advantage of lower leakage inductance, excellent thermal behaviour, increased reproducibility, significant manufacturing simplicity and higher reliability [30]. The prototype is consisted of 5 section, each section is a 6-Layer-PCB. Each stack is then connected with wires to other stacks to make the full transformer (the connection for both primary and secondary is series).



(a)



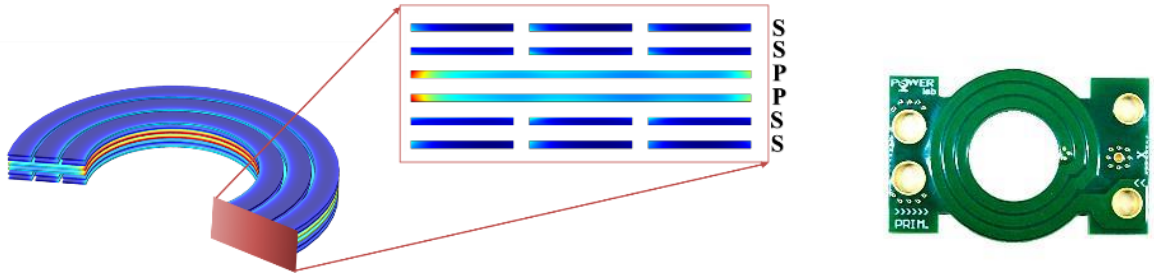
(b)



(c)

Figure 46 Experimental realization of the designed transformer: (a) Stacks of transformer layers and cores, separated. (b) Planar transformer's top view without connection wires. (c) Transformer's top view with connections, under short circuit test.

The transformer was designed to have small AC resistance, and therefore an interleaved structure [31], shown in **Figure 47** was utilized.



(a) (b)

Figure 47 (a) Structure of the transformer for minimizing AC resistance at 300 kHz switching frequency and (b) a stack of 1:12 turns ration manufactured in a 6-layer planar PCB.

Full-load operation of the transformer proved a power density of greater that 6 kW/l (equivalent of 100 W/inch^3), which is a great achievement, for the high step-up. The Assembled planar transformer with dimensions of 70mm x 35mm x 25mm (L x W x H) is shown in **Figure 48**.

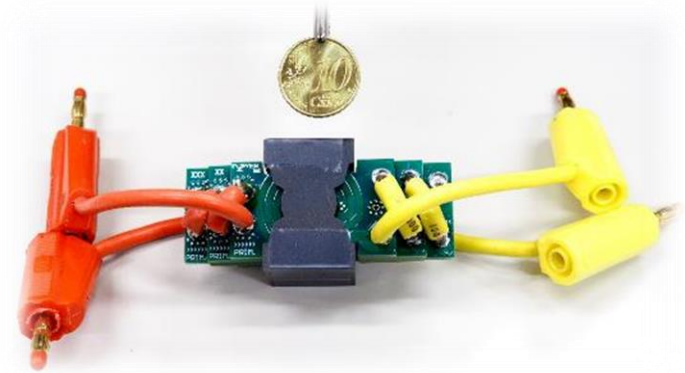
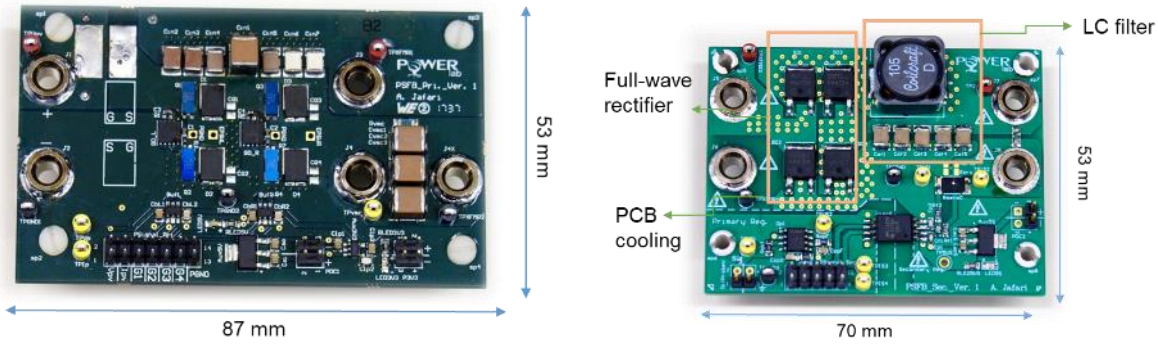


Figure 48 Planar transformer achieving a power density of more than 6 kW/l (100 W/inch3).

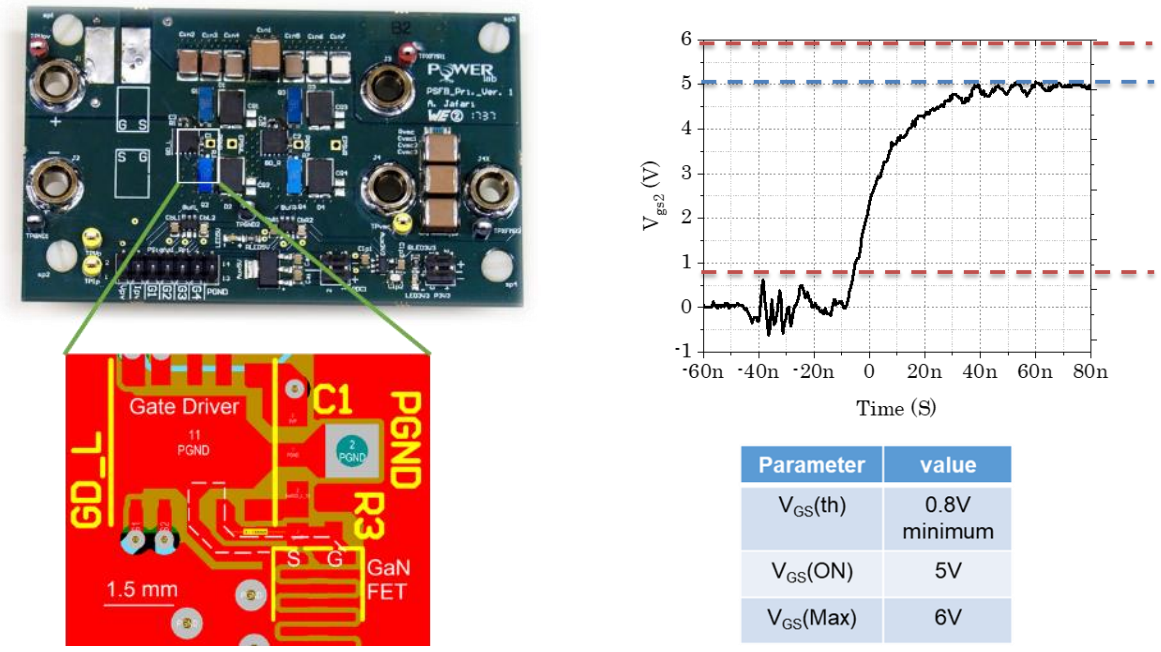
The transformer is accompanied with primary and secondary bridges. The low voltage bridge (primary side) is consisted of EPC2022 GaN devices. Secondary side is a full-wave rectifier consisted of SiC Schottky diodes (IDM02G120C5XTMA1) for ultrafast switching performance. The designed PCB layout of primary and secondary are shown in **Figure 49 (a)** and **(b)** respectively.



(a) (b)

Figure 49 (a) Primary bridge consisted of EPC GaN transistors and (b) secondary bridge consisted of SiC Schottky diodes and the LC output filter

There are several considerations regarding the design of the two bridges [32]. On the primary side, high-frequency PCB design measures are considered, to satisfy the strict driving condition for EPC2022 GaN devices. This includes the gate immunity from overshoot while turn-on, and undershoot while turn-off, due to the parasitic inductance of the gate drive loop. **Figure 50 (a)** shows the PCB layout for the gate drive loop, and **Figure 50 (b)** illustrates the resulting gate drive signal (V_{GS}) which satisfies the strict requirements of driving GaN FETs.



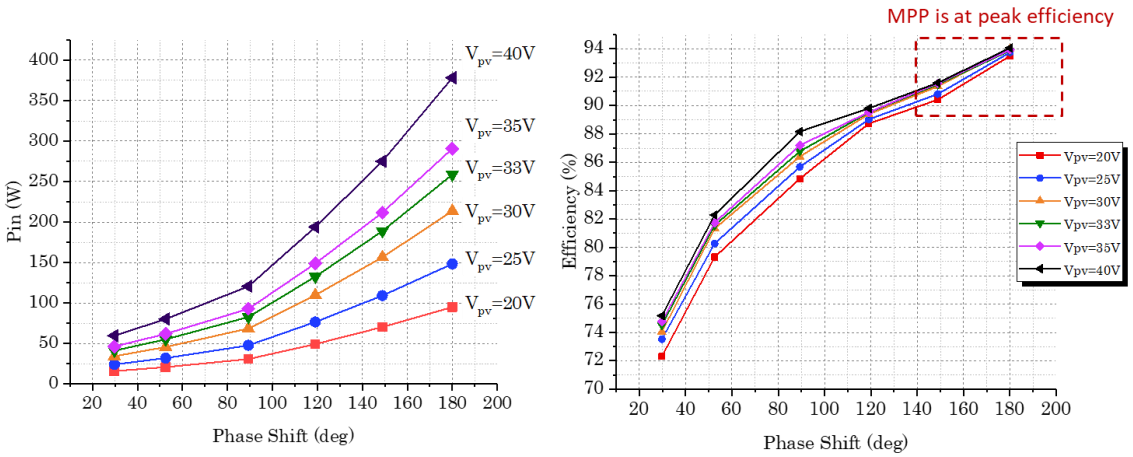
Parameter	value
V_{GS}(th)	0.8V minimum
V_{GS}(ON)	5V
V_{GS}(Max)	6V

(a) (b)

Figure 50 (a) Minimized gate drive loop for minimizing the inductance and (b) the resulting gate drive signal, satisfying strict requirements of driving GaNFET EPC2022.

On the secondary side, thermal vias are utilized to spread the heat from the Schottky diodes to the PCB surface, which resulted in the control of the temperature without use of any heatsinks or forced air cooling. This is a great achievement, making the design reliability high and life time very long.

The converter prototype was tested and the efficiency was measured for different loads and input voltages (remembering that the input of the converter is connected to a PV panel which its voltage varies between 20 *V* to 40 *V*, while the maximum power point in STC occurs at 33 *V*). The results are shown in **Figure 51.**

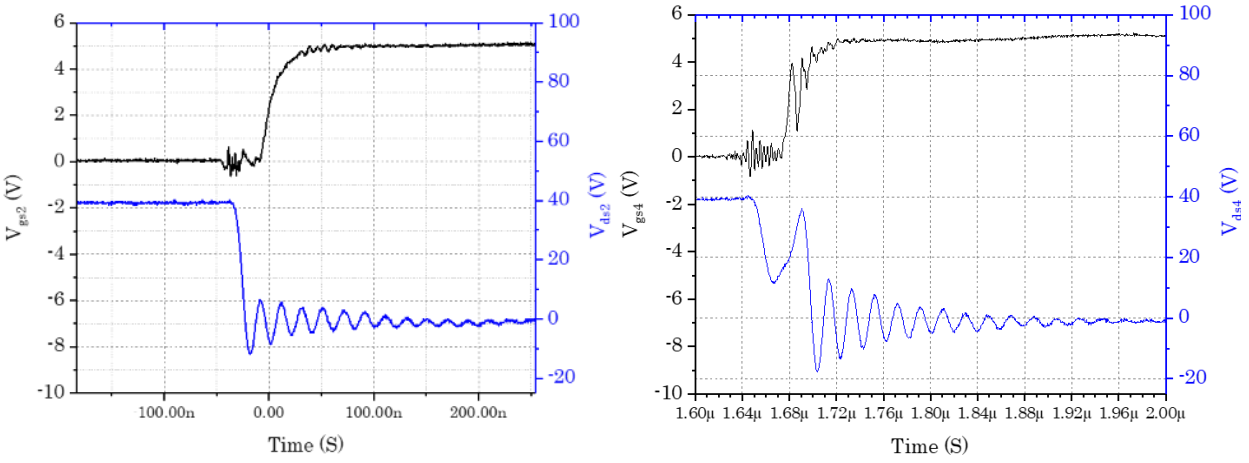


(a) (b)

Figure 51 Performance of the DC-DC micro-converter: (a) Input power versus phase shift as the control parameter and (b) efficiency versus phase shift

Phase shift between the two legs of the primary full-bridge is the parameter which determines the amount of power delivered from primary to secondary DC link. These legs are called leading and lagging legs. Interpreting the performance data of the converter, we can observe that the power capability and efficiency of the converter increases with increasing input voltage. At the rated operating conditions, the converter has its highest efficiency, which is thanks to the soft-switching of the primary switches. As the load reduces, while the core losses in the transformer remains constant, the soft-switching is reduced due to the partial load operation, and this results in a reduction of efficiency.

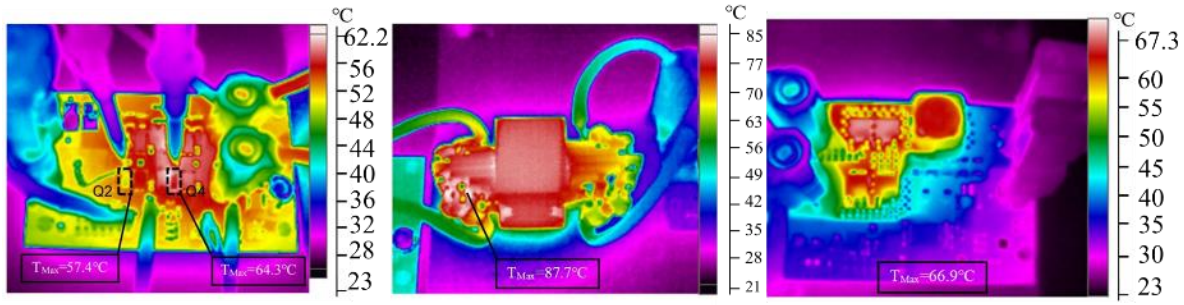
Waveforms regarding the soft-switching performance of the converter are illustrated in **Figure 52** for switches in the leading and lagging legs, respectively. The leading leg has a more relaxed restrictions for achieving ZVS, because both the leakage inductance of the transformer as well as the secondary side filter inductance participate in commutation of its switches; whereas for the lagging leg switches, only the leakage inductance of the transformer is involved during the switching transition. This also results in different temperatures for the switches of each leg, as an indication of correct behavior of the circuit (**Figure 53 (a)**).



(a) (b)

Figure 52 Soft-switching performance; (a) Drain to source voltage and gate to source voltage for the leading leg, achieving full ZVS and (b) the lagging leg, achieving partial ZVS

Thermal performance of the converter is shown in **Figure 53**. As mentioned before, the converter achieved a high efficiency of more than 93% for the full-load operation. This resulted in further reduction of the size, as there was no need to provide cooling through heatsink or a fan [33].



(a) (b) (c)

Figure 53 Thermal images of the converter: (a) primary inverter with maximum temperature below 65°C; (b) transformer with maximum temperature below 90°C; (c) secondary rectifier with maximum temperature below 70°C.

6.5.5 Future Prospects for Micro-converter Systems

As a summary, the designed converter provides efficient energy conversion from PV panels, and increases the energy harvested from the PV generator. The prototype proved to take the advantage of high-frequency operation to reach compact size. This is achieved thanks to increased switching frequency made possible by GaN technology, and corresponding magnetic design of the high-frequency transformer.

The efforts did not end to the PV micro-converter. To explore the potential of magnetically isolated DC-DC converters, which have a great potential in low voltage direct current (LVDC) applications such as photovoltaic converter and electric vehicle (EV) charger, a generalized converter was developed, aiming for higher power levels. The ability of the converter to be scaled up in a multi-cell high power converter, makes it a very interesting choice for EV chargers inside electric cars. The outlook for a future DC grid, which can also be running independent of the AC grid, is summarized in **Figure 54**. Several energy sources generate LVDC. Almost all the consumer loads require DC voltage, either directly or indirectly. In this context, the role of the DC-DC converters becomes important, as they are the heart of energy conversion in such a network.

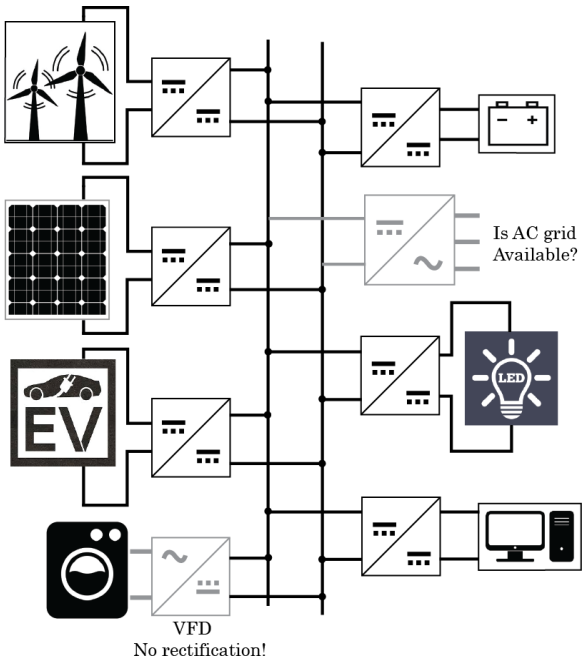


Figure 54 A future DC grid, running based on DC-DC converters, with possibilities to be interconnected to the AC grid or not (flexible)

Outlook

GaN HEMTs can enable much higher switching frequencies and switching speeds for power converters that allow to accomplish what Si based technologies cannot. This is a new regime of operation for power electronics where the power device directly influences the circuit operation and resulting losses. The losses directly dictate the integration capabilities of the power electronic system, and therefore, needs to be well understood. This demands proper knowledge of the circuit's high-frequency behaviour both from device and circuit levels.

While investigation of the applications for GaN was a main goal of this project, there are more to do in terms of understanding the device behavior in future. Demand for higher efficiencies and power densities on one side, and improved performance made possible with new materials on the other hand has made it possible to make converters with ultra-high efficiency, which is impossible to measure with electrical measurement equipment. The prospect of research in POWERlab involves accurate thermal measurement of the losses in power converters.

In this sense we plan to investigate the relationship between device physical properties and consequent losses in the power electronic circuit, especially at very high switching frequencies. First step in achieving this would be to lay the technical basis in correctly characterizing GaN losses which are critical in MHz range applications. New measurement techniques are to be built to capture important characteristics, such as the output capacitance. This aids in developing accurate models so that we can correctly predict system performance. In the long-run, this will greatly reduce the system design time. We are currently developing new methods and measurement systems to better understand GaN High Electron Mobility Transistors' (HEMT) switching behavior and resulting losses, and their measurements.

Publications

The scientific achievements of our group related to this project are listed below.

1. R. Faraji, G. Kampitsis, H. Farzanehfard, M. Mattavelli, E. Matioli, M. Esteki, “Fully-Soft Switched High Step-up Non-Isolated Multi-Input DC-DC Converter”, (under review) 2019
2. M. S. Nikoo, A. Jafari and E. Matioli, “On-Chip High-Voltage Sensors Based on Trap-Assisted 2DEG Channel Control”, **IEEE Electron Device Letters**, 1-1, 2019
3. L. Nela, M. Zhu, J. Ma, and E. Matioli, “High-performance nanowire-based E-mode Power GaN MOSHEMTs with large workfunction gate metal”, **IEEE Electron Device Letters**, 1-1, 2019
4. R. A. Khadar, C. Liu, R. Soleimanzadeh, and E. Matioli, “Fully-vertical GaN-on-Si power MOSFETs”, **IEEE Electron Device Letters**, Vol. 40, issue 3, 443-446, March 2019
5. J. Ma, G. Kampitsis, P. Xiang, K. Cheng and E. Matioli, “Multi-Channel Tri-gate GaN Power Schottky Diodes with Low ON-Resistance”; **IEEE Electron Device Letters**, vol. 40, no. 2, pp. 275-278, 2018.
6. J. Ma, C. Erine, P. Xiang, K. Cheng and E. Matioli, “Multi-channel tri-gate normally-on/off AlGaN/GaN MOSHEMTs on Si substrate with high breakdown voltage and low ON-resistance”, **Applied Physics Letters**, 113, 24, 242102, 2018.
7. Jafari and E. Matioli, “High Step-Up High-Frequency Zero-Voltage Switched GaN-Based Single-Stage Isolated DC-DC Converter for PV Integration and Future DC Grids**”** PCIM Europe 2018.
8. Liu, R. Abdul Khadar and E. Matioli, “Vertical GaN-on-Si MOSFETs With Monolithically Integrated Freewheeling Schottky Barrier Diodes”, **IEEE Electron Device Letters**, vol. 39, no. 7, pp. 1034-1037 , 2018
9. T. Wang, J. Ma and E. Matioli, “1100 V AlGaN/GaN MOSHEMTs With Integrated Tri-Anode Freewheeling Diodes”, **IEEE Electron Device Letters**, vol. 39, no. 7, pp. 1038-1041, 2018.
10. C. Liu, R. A. Khadar and E. Matioli, “645 V quasi-vertical GaN power transistors on silicon substrates”, 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (**ISPSD**), p. 240-243, 2018.
11. M. Zhu and E. Matioli, “Monolithic integration of GaN-based NMOS digital logic gate circuits with E-mode power GaN MOSHEMTs”, 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (**ISPSD**), p. 236-239, 2018.
12. J. Ma and E. Matioli, “Uni-directional GaN-on-Si MOSHEMTs with high reverse-blocking voltage based on nanostructured Schottky drain**”,** IEEE 30th International Symposium on Power Semiconductor Devices and ICs (**ISPSD**), p. 192-195., 2018.
13. J. Ma, and E. Matioli, “2 kV slanted tri-gate GaN-on-Si Schottky barrier diodes with ultra-low leakage current”, **Appl. Phys. Lett.**, vol. 112, 052101, 2018.
14. R. A. Khadar, C. Liu, L. Zhang, P. Xiang, K. Cheng and E. Matioli, “*820 V GaN-on-Si Quasi-Vertical P-i-N Diodes with BFOM of 2.0 GW/cm^2*”, **IEEE Electron Device Letters**, vol. 39, no. 3, pp. 401-404, Mar. 2018. **(editor’s pick of the IEEE Electron Device Letters)**
15. C. Liu, R. A. Khadar and E. Matioli, “*GaN-on-Si Quasi-Vertical Power MOSFETs*”, **IEEE Electron Device Letters**, vol. 39, num. 1, p. 71-74, 2018.
16. J. Ma, M. Zhu and E. Matioli, “*900 V Reverse-Blocking GaN-on-Si MOSHEMTs with a Hybrid Tri-anode Schottky Drain*”, **IEEE Electron Device Letters**, p. 1-1, 2017.
17. G. Santoruvo and E. Matioli, “*In-Plane-Gate GaN Transistors for High-Power RF Applications*”, **IEEE Electron Device Letters**, vol. 38, num. 10, p. 1413-1416, 2017.
18. J. Ma, D. C. Zanuz and E. Matioli, “*Field Plate Design for Low Leakage Current in Lateral GaN Power Schottky Diodes: Role of the Pinch-Off Voltage*”, **IEEE Electron Device Letters**, vol. 38, num. 9, p. 1298 - 1301, 2017.
19. J. Ma and E. Matioli, “*Slanted Tri-gates for High-Voltage GaN Power Devices*”, **IEEE Electron Device Letters**, vol. 38, num. 9, p. 1305 - 1308, 2017.
20. J. Ma and E. Matioli, “High Performance Tri-gate GaN Power MOSHEMTs on Silicon Substrate”, **IEEE Electron Device Letters**, vol. 38, num. 3, p. 367 - 370, 2017.

21. J. Ma and E. Matioli, "*High-Voltage and Low-Leakage AlGaN/GaN Tri-Anode Schottky Diodes With Integrated Tri-Gate Transistors*", **IEEE Electron Device Letters**, vol. 38, num. 1, p. 83-86, 2017.
22. J. Ma, G. Santoruvo, P. Tandon and E. Matioli, *Enhanced electrical performance and heat dissipation in AlGaN/GaN Schottky barrier diodes using hybrid tri-anode structure*, ***IEEE Transactions on Electron Devices***, vol. 63, num. 9, p. 3614 - 3619, 2016.

References

[1] M. Danilovic, Z. Chen, R. Wang, F. Luo, D. Boroyevich, and P. Mattavelli, "Evaluation of the switching characteristics of a gallium-nitride transistor," in 2011 IEEE Energy Conversion Congress and Exposition, Phoenix, AZ, USA, 2011, pp. 2681–2688.
[2] S. Jiang et al., "All-GaN-Integrated Cascode Heterojunction Field Effect Transistors," IEEE Transactions on Power Electronics, vol. 32, no. 11, pp. 8743–8750, Nov. 2017.
[3] B. Sun, R. Burgos, X. Zhang, and D. Boroyevich, "Active dv/dt control of 600V GaN transistors," in 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 2016, pp. 1–8.
[4] D. Reusch and J. Strydom, "Understanding the Effect of PCB Layout on Circuit Performance in a High Frequency Gallium Nitride Based Point of Load Converter," p. 7.
[5] X. Zhang, Z. Shen, N. Haryani, D. Boroyevich, and R. Burgos, "Ultra-low inductance vertical phase leg design with EMI noise propagation control for enhancement mode GaN transistors," in 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 2016, pp. 1561–1568.
[6] R. Gelagaev, P. Jacqmaer, and J. Driesen, "A Fast Voltage Clamp Circuit for the Accurate Measurement of the Dynamic ON-Resistance of Power Transistors," IEEE Transactions on Industrial Electronics, vol. 62, no. 2, pp. 1241–1250, Feb. 2015.
[7] T. Yao and R. Ayyanar, "A Multifunctional Double Pulse Tester for Cascode GaN Devices," IEEE Transactions on Industrial Electronics, vol. 64, no. 11, pp. 9023–9031, Nov. 2017.
[8] J. Ma and E. Matioli, "2 kV slanted tri-gate GaN-on-Si Schottky barrier diodes with ultra-low leakage current," Appl. Phys. Lett., vol. 112, no. 5, p. 052101, Jan. 2018.
[9] J. Ma, M. Zhu, and E. Matioli, "900 V Reverse-Blocking GaN-on-Si MOSHEMTs With a Hybrid Tri-Anode Schottky Drain," IEEE Electron Device Letters, vol. 38, no. 12, pp. 1704–1707, Dec. 2017.
[10] J. Ma, D. C. Zanuz, and E. Matioli, "Field Plate Design for Low Leakage Current in Lateral GaN Power Schottky Diodes: Role of the Pinch-off Voltage," IEEE Electron Device Letters, vol. 38, no. 9, pp. 1298–1301, Sep. 2017.
[11] J. Ma and E. Matioli, "High Performance Tri-Gate GaN Power MOSHEMTs on Silicon Substrate," IEEE Electron Device Letters, vol. 38, no. 3, pp. 367–370, Mar. 2017.
[12] J. Ma and E. Matioli, "High-Voltage and Low-Leakage AlGaN/GaN Tri-Anode Schottky Diodes With Integrated Tri-Gate Transistors," IEEE Electron Device Letters, vol. 38, no. 1, pp. 83–86, Jan. 2017.
[13] J. Ma and E. Matioli, "Improved electrical and thermal performances in nanostructured GaN devices," in 2016 International Conference on IC Design and Technology (ICICDT), Ho Chi Minh City, 2016, pp. 1–4.
[14] J. Ma and E. Matioli, "Slanted Tri-Gates for High-Voltage GaN Power Devices," IEEE Electron Device Letters, vol. 38, no. 9, pp. 1305–1308, Sep. 2017.
[15] SuisseEnergie. L'eclairage efficace des rues avec des led. 2016.
[16] AFE. Guide d'application de la norme europeenne eclairage public en13201. 2007.
[17] Photovoltaic geographical information system . http://re.jrc.ec.europa.eu/pvgis/apps4/pvest.php.
[18] Suntag. http://suntag.ch/index.php.
[19] General transport management of geneva - traffic statistics. http://ge.ch/transports/guichet-technique/statistiques-de-la-mobilite/le-trafic-motorise/trafic-journalier.
[20] C.-S. Huang and M.-Y. Chow, "Accurate Thevenin's circuit-based battery model parameter identification," in 2016 IEEE 25th International Symposium on Industrial Electronics (ISIE), Santa Clara, CA, USA, 2016, pp. 274–279.
[21] "Cell balancing maximizes the capacity of multi-cell batteries," EETimes. [Online]. Available: https://www.eetimes.com/document.asp?doc_id=1230515. [Accessed: 26-Sep-2018].

[22] Y. Zhang, R. Zhao, J. Dubie, T. Jahns, and L. Juang, “Investigation of current sharing and heat dissipation in parallel-connected lithium-ion battery packs,” in 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 2016, pp. 1–8.
[23] A. Mombelli, “Renewable energies: Switzerland lagging behind in Europe,” swissinfo.ch, 17-May-2017. [Online]. Available: https://www.swissinfo.ch/eng/politics/energy-strategy-2050_renewable-energies-switzerland-lagging-behind-in-europe/43187716.
[24] A. Ghaffari, M. Krstić, and S. Seshagiri, “Power Optimization for Photovoltaic Microconverters Using Multivariable Newton-Based Extremum Seeking,” IEEE Transactions on Control Systems Technology, vol. 22, no. 6, pp. 2141–2149, Nov. 2014.
[25] M. Kasper, M. Ritz, D. Bortis, and J. W. Kolar. PV Panel-Integrated High Step-up High Efficiency Isolated GaN DC-DC Boost Converter. In Intelec 2013; 35th International Telecommunications Energy Conference, SMART POWER AND EFFICIENCY, pages 1–7, October 2013.
[26] Jiangheng Lu and A. Khaligh. 1kw, 400v/12v high step-down DC/DC converter: Comparison between phase-shifted full-bridge and LLC resonant converters. In 2017 IEEE Transportation Electrification Conference and Expo (ITEC), pages 275–280, June 2017.
[27] Xinbo. Ruan. Soft-switching PWM full-bridge converters : topologies, control, and design. 2014.
[28] Edward Hebner. Soft Ferrites and Accessories Data Handbook (Ferroxcube), 2013.
[29] Irma VILLAR. Multiphysical Characterization of Medium-Frequency Power Electronic Transformers. PhD thesis, ECOLE POLYTECHNIQUE FDRALE DE LAUSANNE, EPFL, Switzerland, 2010.
[30] M. A. Saket, N. Shafiei, and M. Ordonez. Planar transformer winding technique for reduced capacitance in LLC power converters. In 2016 IEEE Energy Conversion Congress and Exposition (ECCE), pages 1–6, September 2016.
[31] Z. Ouyang, O. C. Thomsen, and M. A. E. Andersen. Optimal design and tradeoffs analysis for planar transformer in high power DC-DC converters. In The 2010 International Power Electronics Conference - ECCE ASIA -, pages 3166–3173, June 2010.
[32] Alex Lidow, Johan Strydom, Michael de Rooij, and David Reusch. GaN Transistors for Efficient Power Conversion. WILEY, USA, second edition, 2015.
[33] A. Jafari and E. Matioli, “High Step-Up High-Frequency Zero-Voltage Switched GaN-Based Single-Stage Isolated DC-DC Converter for PV Integration and Fu- ture DC Grids,” p. 6, 2018.