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Schlussbericht 20. Oktober 2011

Bi-directional Charger for swiss2G

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Swisselectric Research (SER), Bundesamt für Energie (BFE)

Bidirectional Charger and S2G Controller

Swiss2G Deliverable T2.2

20.10.2011

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T 2.2 Bidirectional Charger and S2G Controller

Summary
In this task the hardware components were developed which are required for the real world testing of the S2G algorithm in phase 2 of the project. In spite of the interruption of the development of the bidirectional charger due to a non accepted delay of the development phase 2 testing is possible because a suitable commercial product is on the market in the meantime. The second essential component is the module for the measurement of the main grid parameters at the socket which are frequency, voltage and current. This first generation measurement module was integrated into the grid data logger so that grid data and the effect of the S2G algorithm can be tested during phase 2 of the project. Foreseen are the use in home charge devices, electric vehicles with bidirectional charger as far as they can be made available, heat pumps and houses with PV and battery.

Content

1. Introduction

The objective of this task T 2.2 was to make prototypes of the S2G hardware components available so that they can be used during phase 2 for real world testing of the S2G concept. These components are:

- The bidirectional charger (BIDIR) for electric vehicles
- The measurement module for frequency, voltage and current
- A hardware which can host the S2G algorithm

Following these components are described and how they can be used for phase 2 of the project.

2. Bidirectional charger (BIDIR)

The development of the bidirectional charger for electric vehicles was included in the project because it is a prerequisite for the exchange of power in both directions between the grid and the electric vehicle and because at the time of the project definition and start such a charger was not available on the market. The development was started in a cooperation of the companies drivetek ag in Switzerland and SMART Electronic Development GmbH in Germany. A drivetek report of the development results is part of final report of phase 1. Fig. 1 shows the block diagram for the charger integration into the electric vehicle and fig. 2 shows a 3D view of the charger. The main parameters of the specification are presented in table 1. The specification was designed battery type neutral.

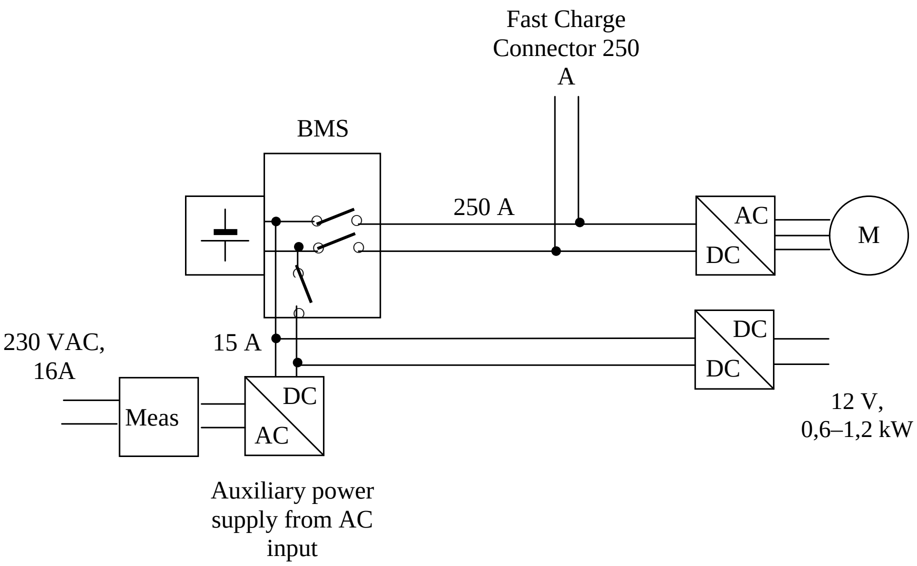


Fig. 1: Block diagram of BIDIR integration into the electric vehicle.

The concept provides the charging of the 12V battery when 230VAC is available, includes the measurement circuit and assumes the charge control by the battery management unit.

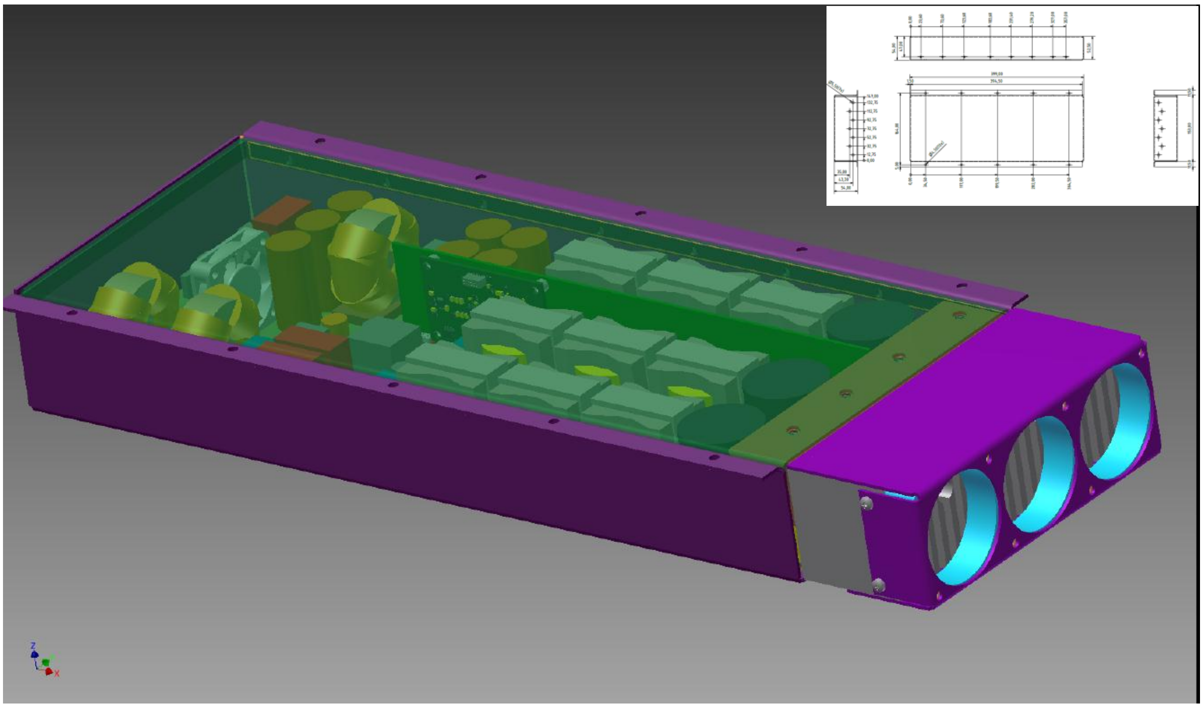


Fig. 2: 3D view of the charger with air cooling

AC	1Ø 230 VAC -15%, +10%
	Current <16A programmable
	Full input protection
DC	Charge/discharge power 3500W
	Battery voltage range 200 – 400 VDC programmable
Temperature	-25°C to 65°C 100% power, 85°C reduced power
Protection	Protection class IP 54

Table 1: Main charger parameters as specified

Since the beginning of the S2G project two of the initial conditions changed: The drivetek/SMART development suffered a delay of ca 5 months so that the new BIDIR charger could not be available for phase 2 of the project and a bidirectional charger with similar specification was available on the market now (encl.1). In order to maintain the overall schedule of the S2G project the own development of the bidirectional charger was stopped and for phase 2 the KACO charger will be used.

3. Measurement Module

The basic assumption of the S2G concept is the use of local grid data for the power consumption regulation. Therefore a prerequisite is a statistical and economic measurement of these grid data. A first measurement module was developed by SMART Electronic Development GmbH on order by Battery Consult. The block diagram of this module (fig.3) shows the use for the Grid Data Logger. The inner part in fig. 3 is the measurement module which was planned to be used for the bidirectional charger. It is also part of the Grid Data Logger which allows monitoring of the grid data over a long period. Per phase voltage, current and frequency are measured. The current up to 16A can be measured directly and for any higher current a conventional current transducer is used. In this way the data can be collected as well at a normal household socket as at the transformer. The data are logged and/or transmitted by one of the four interface options: Ethernet, USB, CAN or RS2485.

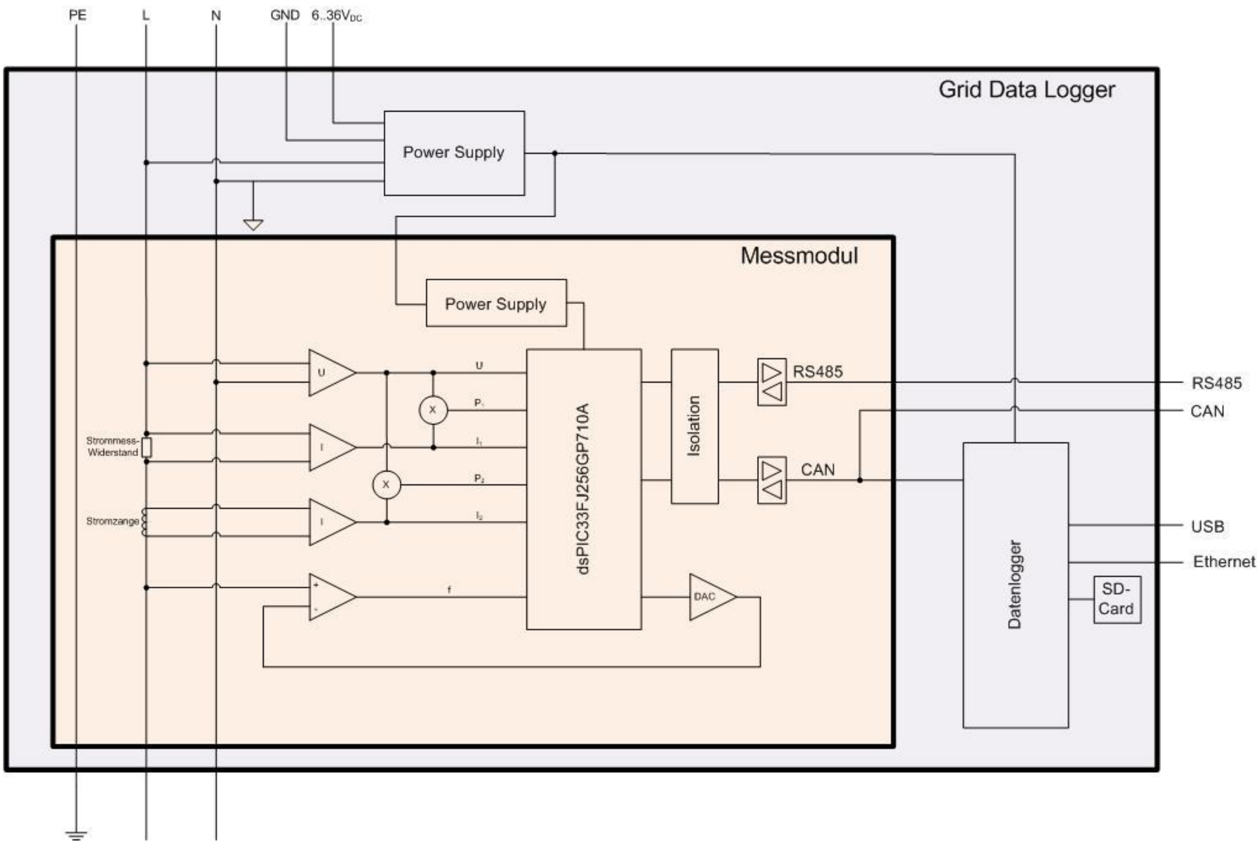


Fig.3: Block diagram of the measurement module as integrated into the grid data logger.

First measurement modules are integrated in the Grid Data Logger (fig.4 and 5) and will be used either for simple measuring and monitoring of grid data or in combination with applications like a HomeChargeDevice (HDC) where it is operated in connection to electric vehicle charging.

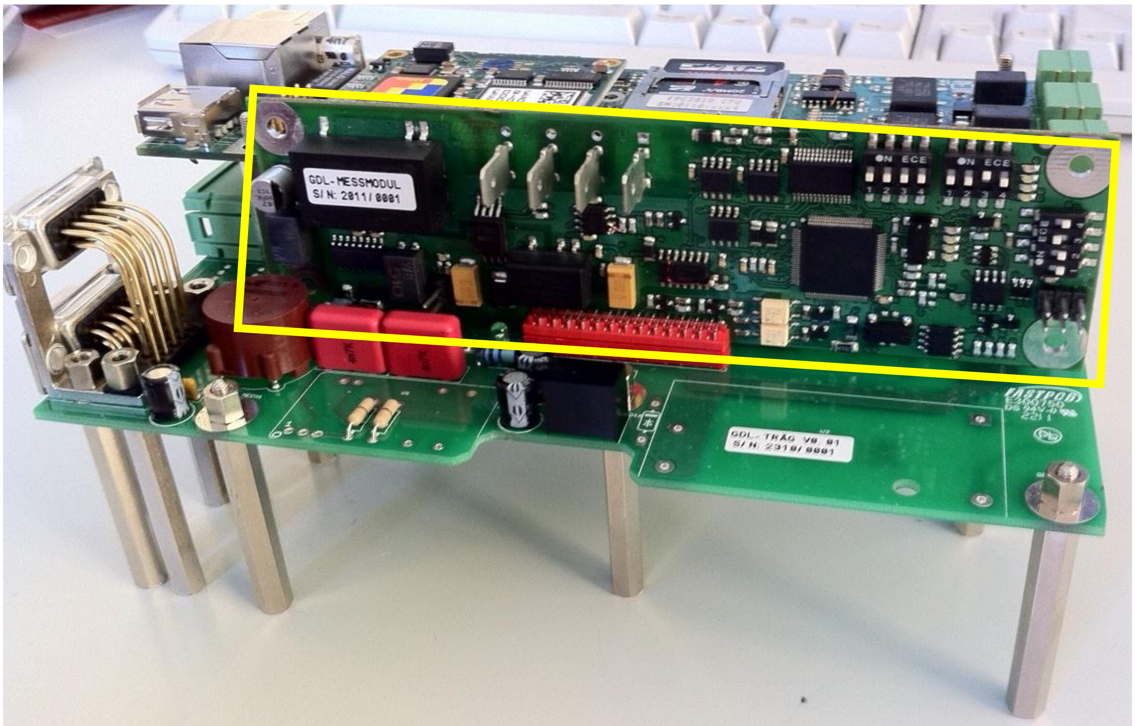


Fig. 4: PCB of the GDL with the measurement circuit marked in yellow

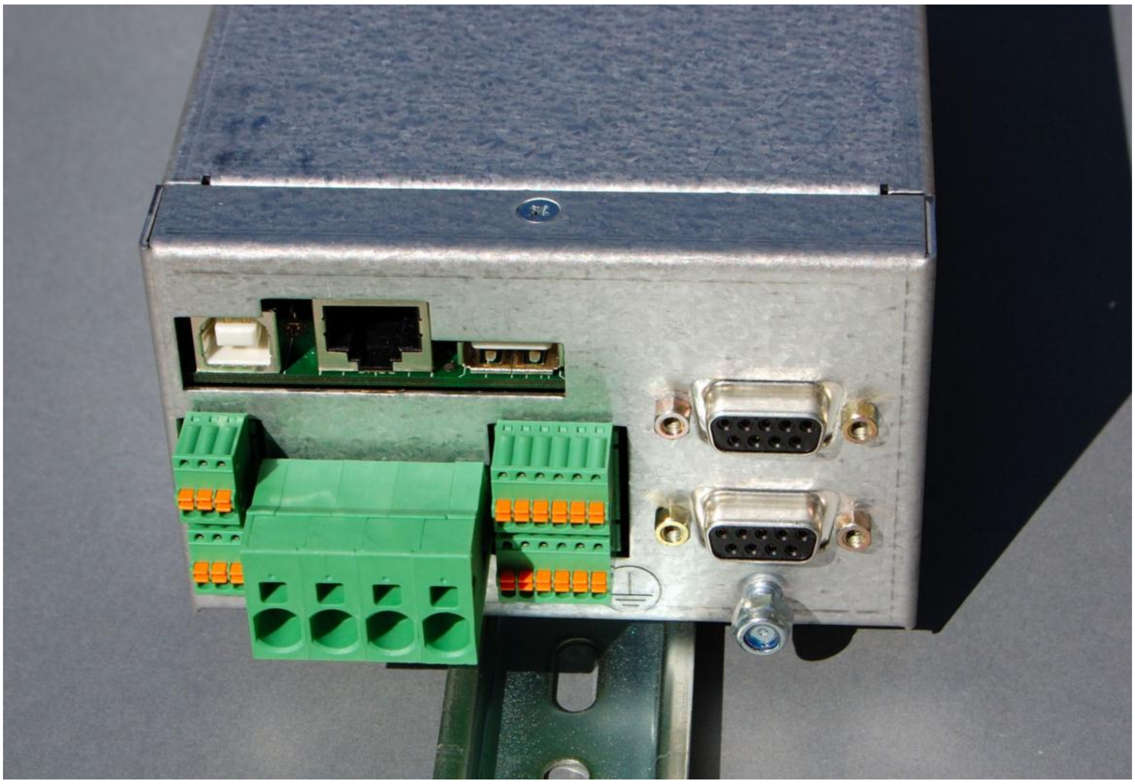


Fig. 5: Prototype Grid Data Logger with I/Os

Using the GDL first test data were taken for a period of 8 hours as shown in fig.6a to 6c. Many more data at different location are to be taken and have to be statistically evaluated in order to confirm the applicability of the algorithm under all conditions and at any time.

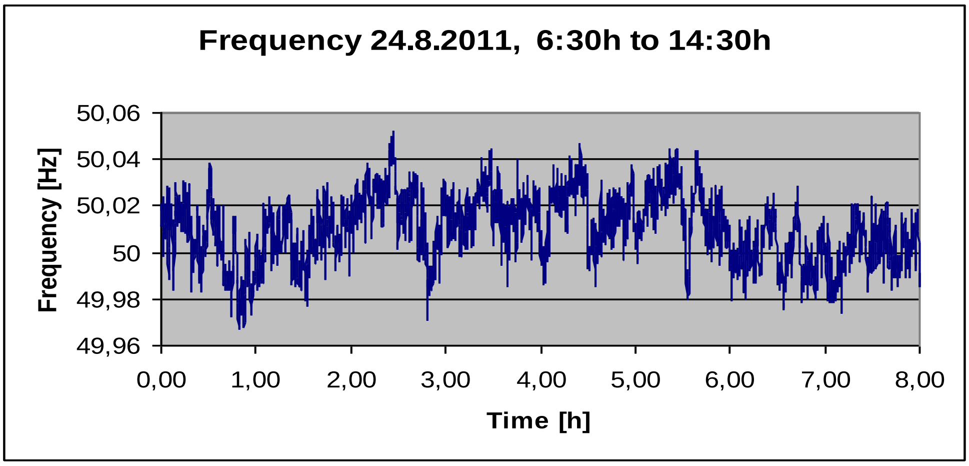


Fig. 6a

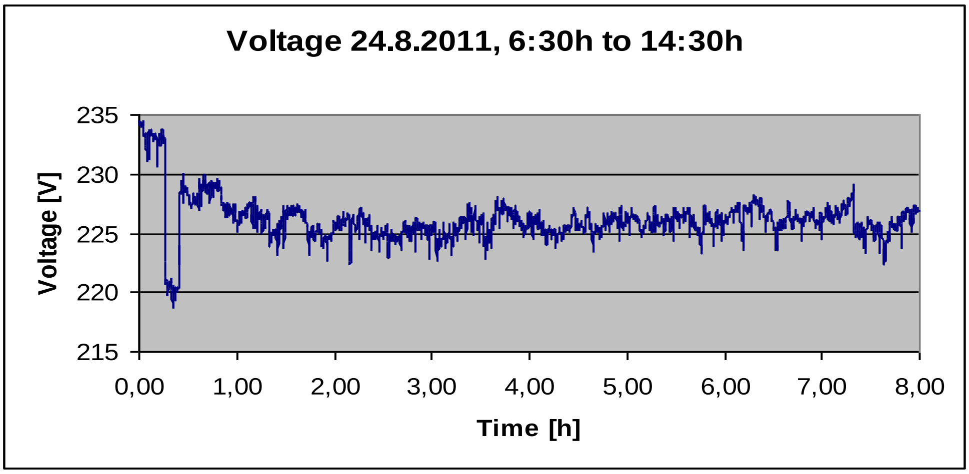
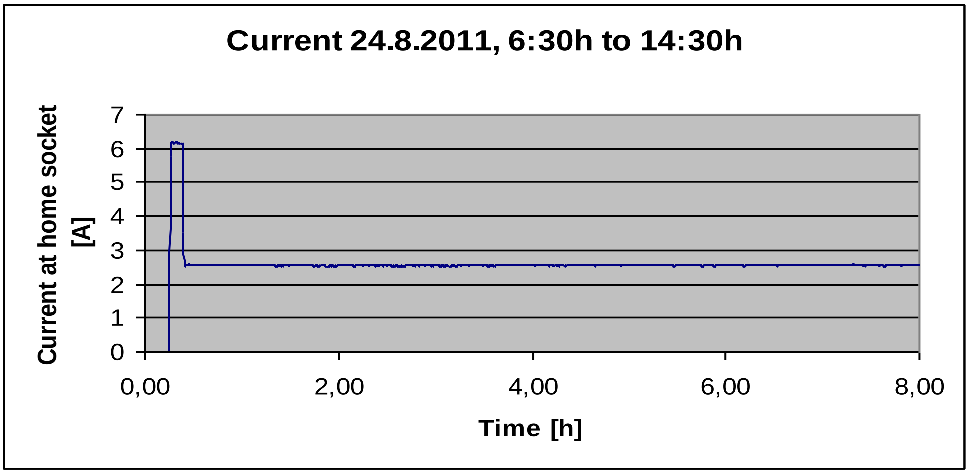


Fig. 6b



4. S2G Algorithm Real World Testing

The GDL has sufficient microprocessor power to host the S2G algorithm. 2 I/O pairs allow the direct control of any power consuming equipment and simultaneously the logger function can register the corresponding grid data. In this way the most important candidates are the electric vehicle just for charge or for charge and discharge if a bidirectional charger is installed in this vehicle, the increasing number of heat pumps which more and more will replace boilers. These are the main high power consuming appliances which are flexible enough to be operated at optimal periods during the day and the week. This will become more and more important with an increasing contribution of renewable energies in the grid.

6. Enclosure: Specifications of Kaco bidirectional charger

Elektrische Daten	KPF3301
Eingangsgrößen	
AC-Spannung	230V, -15% / +20%
AC-Netz / Frequenz	50Hz, -1% / +1%
AC-Netz / maximaler Strom	16A *
AC-Netz / Nennleistung	3,3kW
Ausgangsgrößen Traktionsbatterie	
Spannung	210V- 365 V *
Nenn-Ladestrom	17A *
Nennladeleistung	3,3kW
Ausgangsgrößen Bordnetzbatterie	
Nennspannung	14,4V
max. Ladestrom	10,5A
max. Ladeleistung	150W
Allgemeine elektrische Daten	
bidirektionaler Betrieb	Ladung der Hochvoltbatterie Entladung / Rückspeisung in das öffentliche Versorgungsnetz
Wirkungsgrad (bezogen AC-Netz / Traktionsbatterie)	> 90%
Galvanische Trennung zwischen Ein- und Ausgang	2,5kV
Mechanische Daten	
zulässige Umgebungstemperatur	-25°C…70°C
Derating	ab 60°C; 10% / °C
Kühlung	forciert, elektronisch gesteuert
Gehäuse	Alu-Blechgehäuse, pulverbeschichtet
Schutzart	IP40
Farbe	schwarz
Abmessungen	370 x 300 x 90 mm
Gewicht	12kg
Kommunikation	
Highspeed-CAN	CAN-2.0B, 500kbit/s
Seriell	RS232
Normen	
Konformität zu DIN VDE 0126-1-1	

*) Werte über CAN parametrierbar

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Status report after project abortion

Bidirectional charger 3.5kW

for V2G applications

A-sample development for the S2G project

Approval		
Company	Name	Signature
KWO	Max Ursin	
Battery Consult	Cord Dustmann	
Drivetek AG	Markus Schwab	

Distribution list		
Company	Name	Signature

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Table of contents

1 Change documentation

The changes were inscribed from the first approved version (1.0.0). Before a change is inscribed, the version number of the document has to be inscribed.

Number	Page / section	Description	Date	Name
1	all	Version 1.0.0 compiled	20.09.2011	M.Schwab

2 Introduction

The goal of this project was to develop a bidirectional charger for V2G applications and the S2G project. It was the plan to realize an A-sample in cooperation with Smart-GmbH.

After severe project difficulties in the specification phase and the project terms the result was a substantial project delay.

Even though this delay was reported several times in the early stage of the project, the project management team did not succeed to find an adequate solution in time.

As a result, the project has been abandoned in a relatively late stage (approx. 45% of the project budget).

2.1 Aim of document

This document describes the implemented concepts and the results of the engineering work that has been done so far at drivetek for this project.

2.2 Scope of document

This document describes solely the electronics design. The circuits are not described in detail. The according calculations are not part of this document.

2.3 Terms and abbreviations

abbr.	Description
V2G	Vehicule to grid
S2G	Swiss to grid project
RCD	Residual current device
AFI	Allstromsensitiver FI Schutzschalter
DSP	Digital signal processor
SW	Software
HW	Hardware
OC	Over current
PWM	Pulse width modulation
L	Line connection of the public grid
N	Neutral connection of the public grid
IGBT	Insulated gate bipolar transistor
HB	Half bridge
EMI	Electromagnetic interference
EMC	Electromagnetic compatibility
AC	Alternating current
DC	Direct current
CAN	Controller area network
BMS	Battery management system

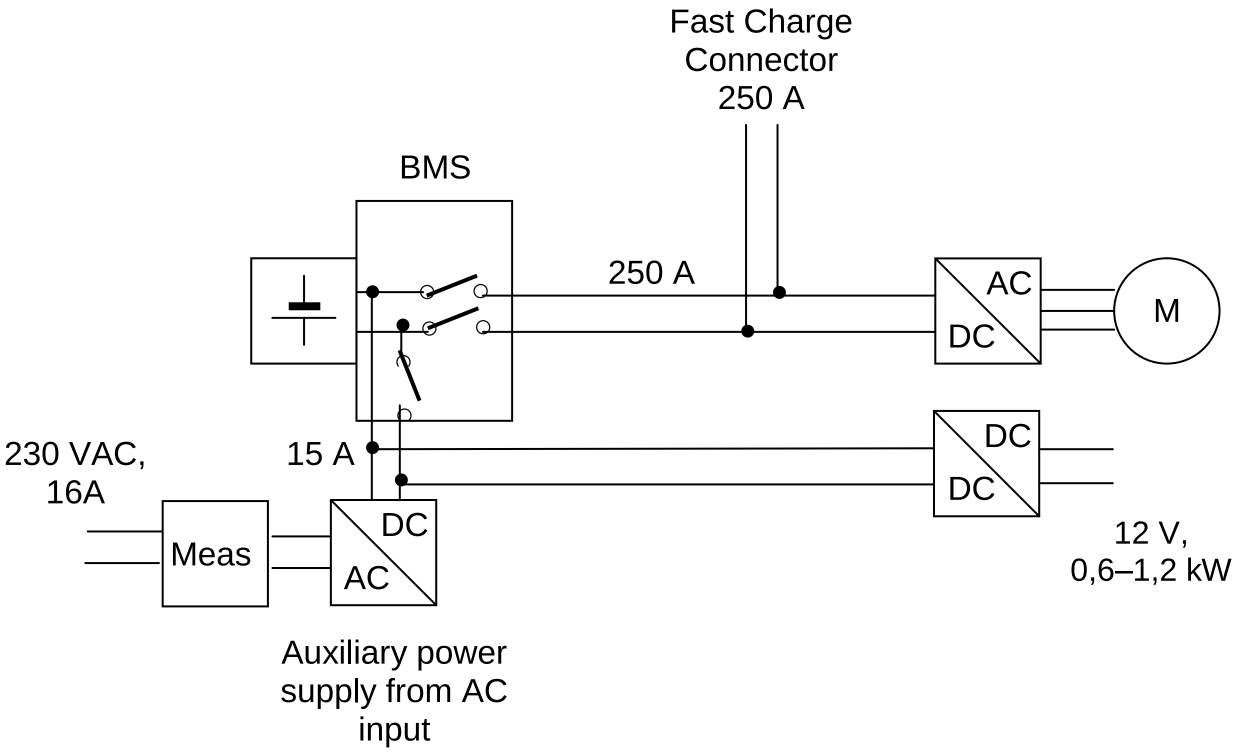
2.4 References

Ref. No.	Document	Description	Author
[1]	1325-2-00-30-0.0.1	Analysis bidirectional charger	M.Schwab
[2]	1325-2-00-20-0.0.9	Specification V2G charger	M.Schwab / Smart GmbH
[3]	1325-2-00-30-0.0.1	Design bidirectional charger	M.Schwab
[4]	1325-3-MB-50-0.0.1	Schematic mainboard bidirectional charger	M.Schwab
[5]	1325-3-CB-50-0.0.1	Schematic controlboard bidirectional charger	M.Schwab
[6]	SPRUG04A, 10.2008	Reference guide TMS320x2833x, 2823x Enhanced Pulse Width Modulator (ePWM) Module	Texas Insturments

3 Concepts

3.1 Circuit concept

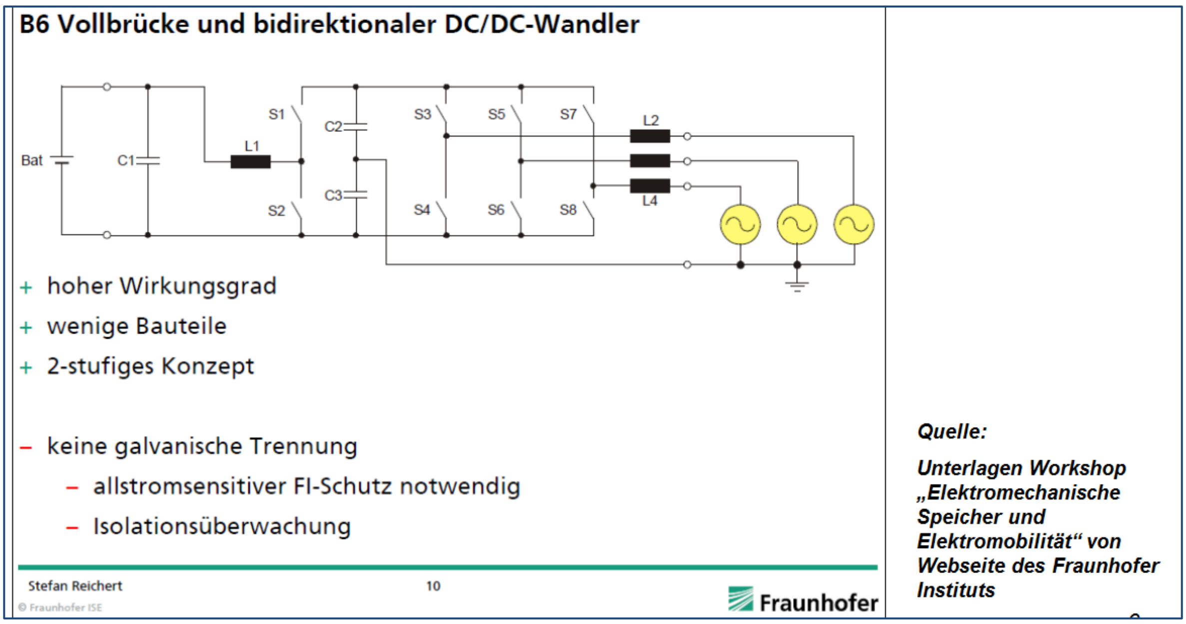
The V2G charger shall be used like shown below.



For further details, see the draft specification [3].

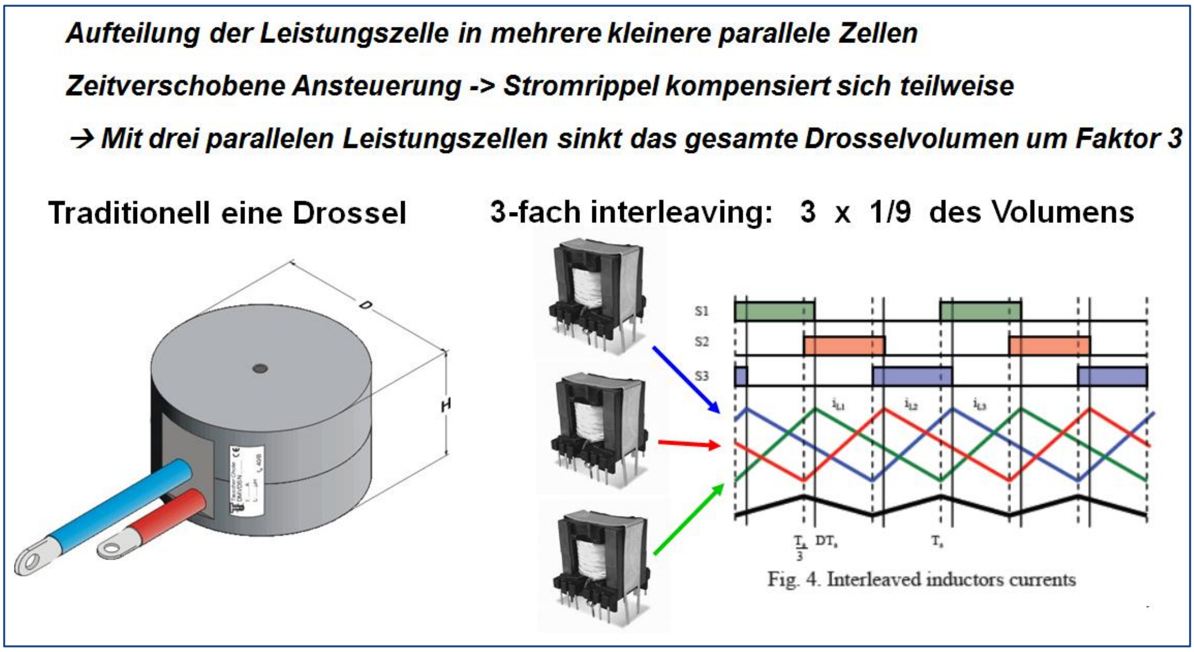
3.2 Electronic concept of power cell

The following basic concept has been choosen, it has been agreed to realize no galvanic separation to minimize the volume and maximize the efficiency.

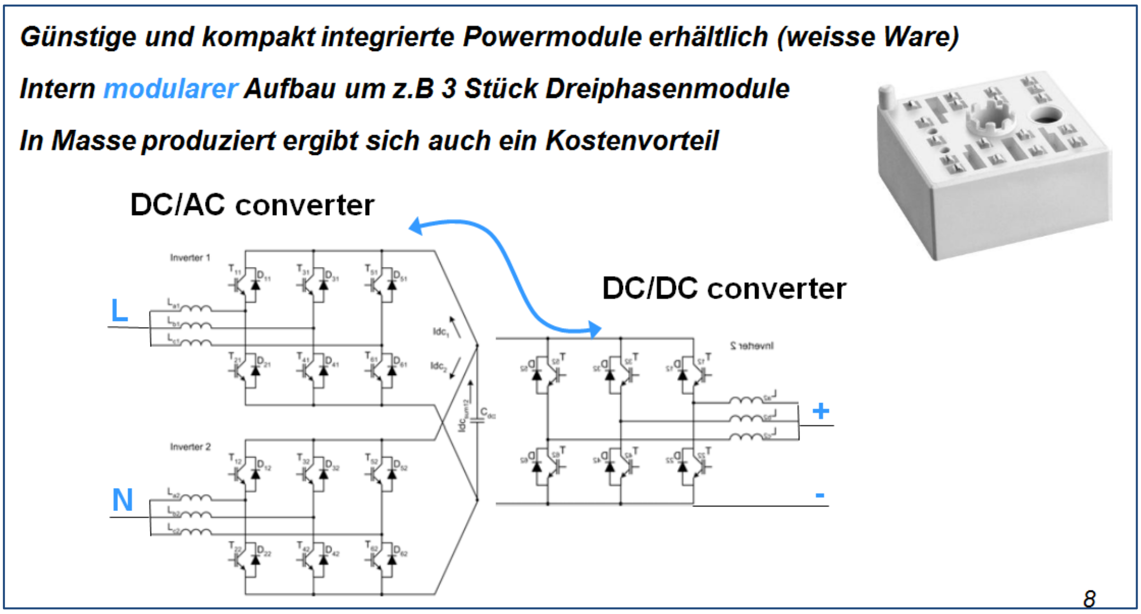


The concept can be adapted for single phase applications easily without connection of the middle point of the DC link.

To minimize the volume and weight an interleaved concept has been choosen:

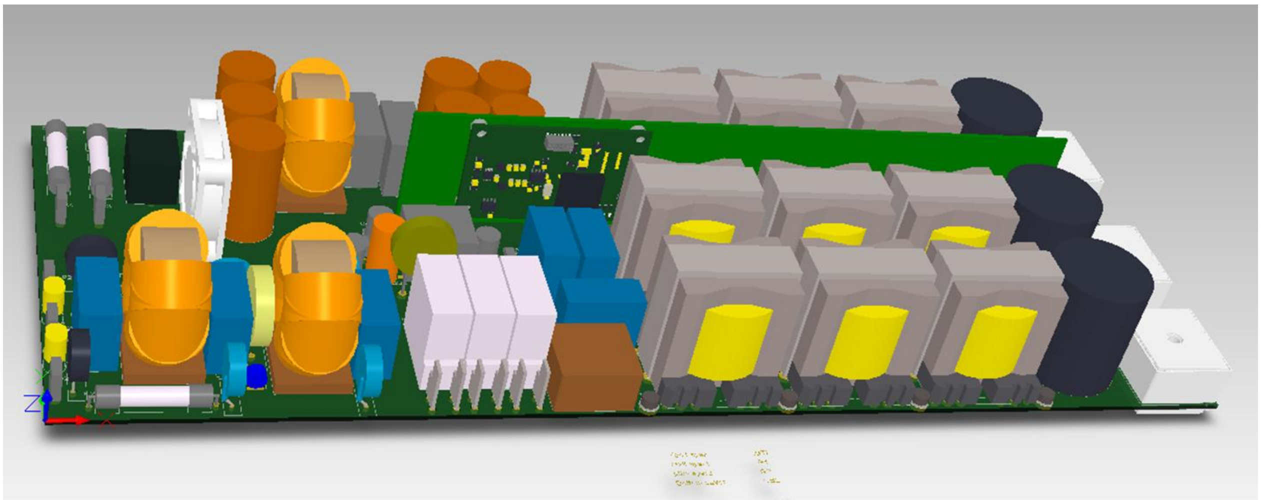


Applying this to the V2G charger the power cell would look like this:



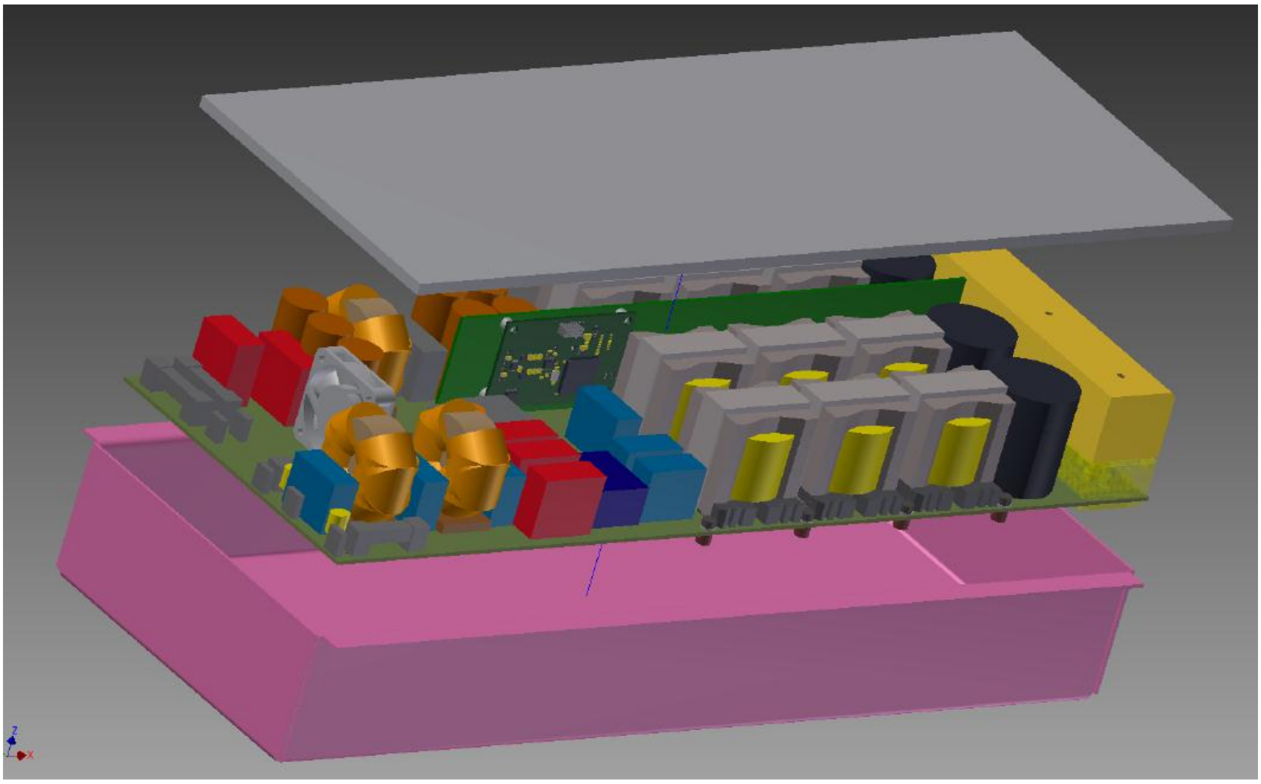
3.3 Electromechanical concept

Based on the analysis of the hardware in document [1] a rough electromechanical concept is proposed.



To achieve lightweight components that are suitable in an automotive environment, an interleaved concept is proposed for the DC/DC converter and the DC/AC converter.

For the cooling it has been agreed to bring the power dissipation of the IGBT modules to the chassis, so cold plate design or an external cooling solution can be used.



Principle chassis construction.

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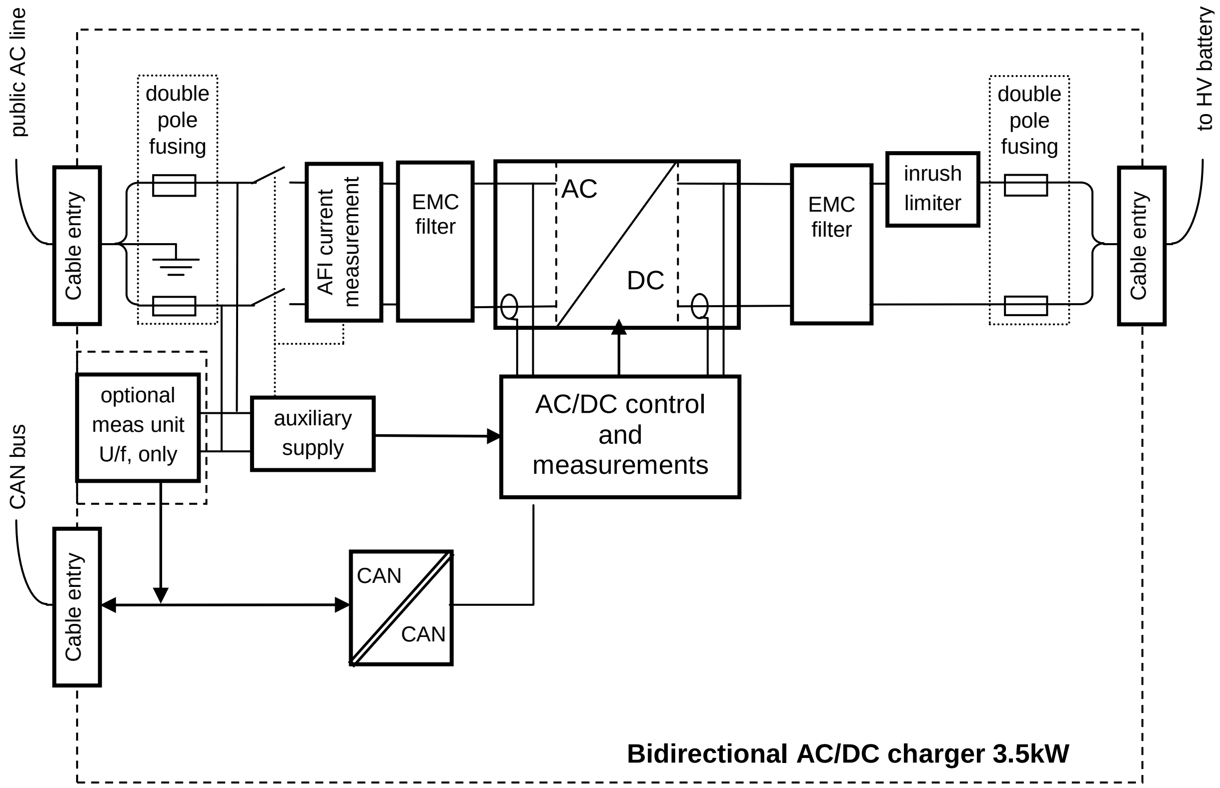
3.4 Block diagram

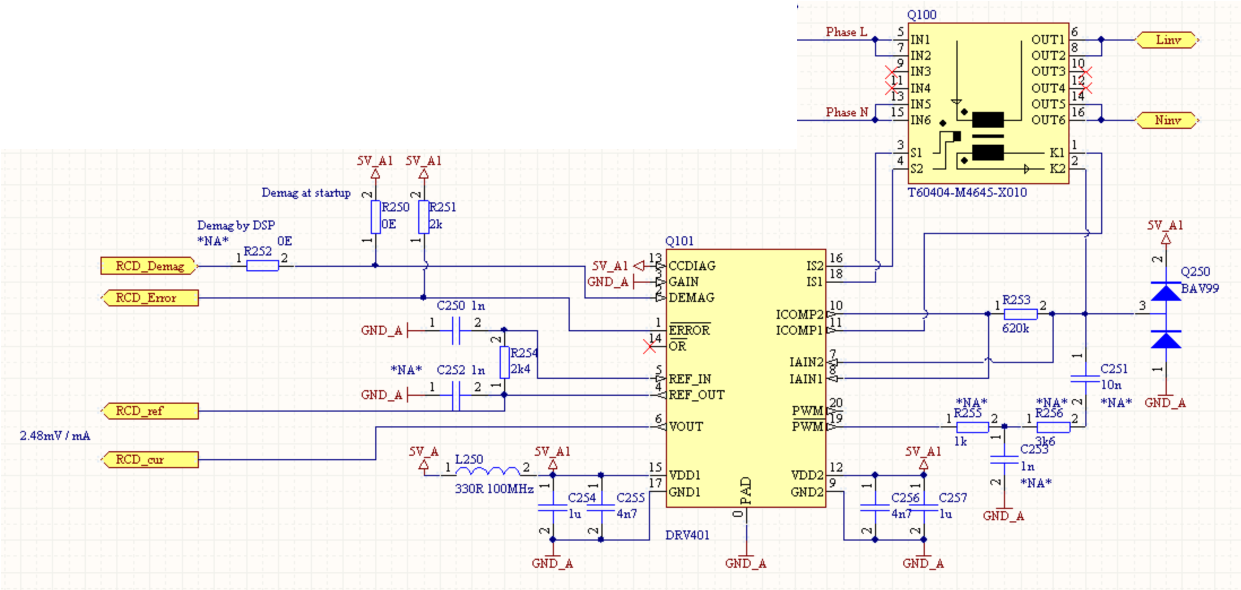
The charger contains the following blocks:



4 Design of blocks

4.1 Residual current device RCD (AFI)

Differential current measurement between L and N phases.



Sensor: VAC T60101-M4645-X010 can be used as DI sensor, if the two middle pins are not used. To have enough creepage on the layout, the two middle pins have no plating at all (additional footprint in Altium).

Driver: TI DRV401. Dimensioning see VAC application note DI sensor.
Measuring range: +/-988mA → 2.5V+/-2.45V (2.48mV / mA)

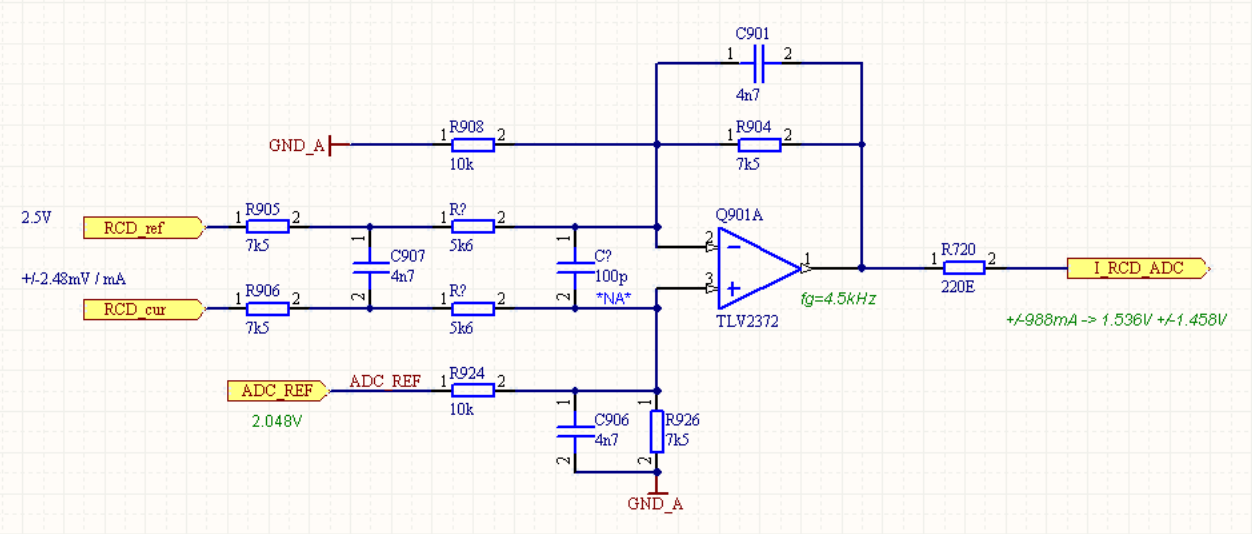
Supply: A separate filtered 5V supply shall be generated from +15V directly to have largest possible independence form supplies around uC (for HW protection). Will be 5V_RCD.

DEMAG: Standard configuration is Demag cycle at startup of 5V_RCD.
Possibility to configure Demag from DSP.

/RCD_Error: Detects winding error of sensor. During Demag cycle, Error is set.

4.1.1 RCD software protection

The RCD current shall be measured by DSP. For this, the signal must be translated from 2.5V ref centered to 1.5V centered (half range of ADC).



Due to limited amount of ADC channels the 1.5V signal is not read back to the ADC. If accuracy (offset) is a problem, the zero current position can be read back before closing of the AC relays.

The DSP will build an RMS value and switch off beyond 30mArms. The DSP will be protected by a hardware watchdog. As additional protection there is also a RCD hardware protection.

4.1.2 RCD hardware protection

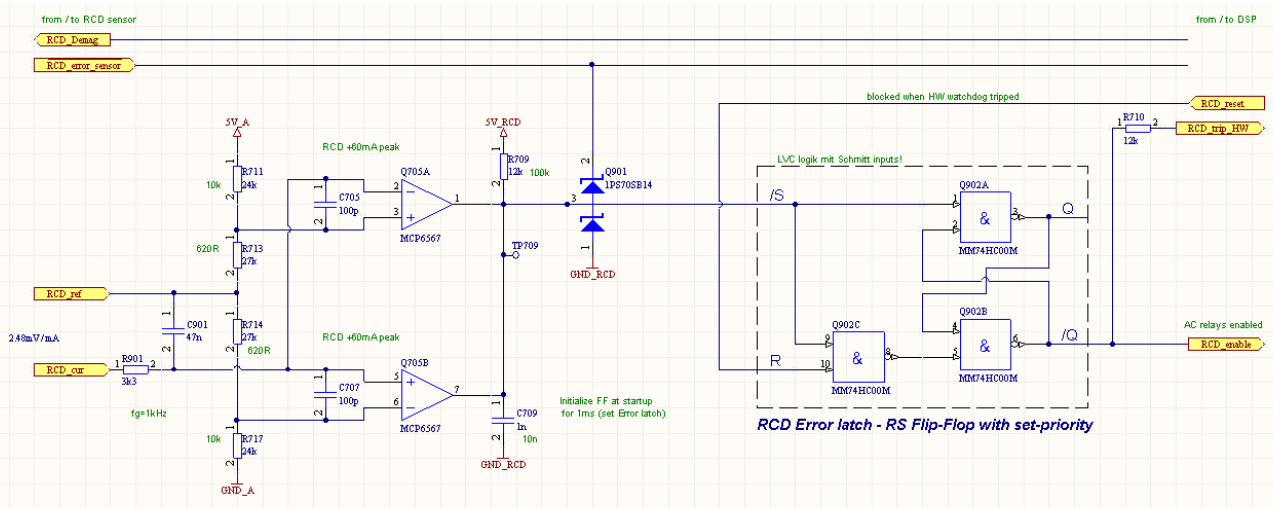
On a trip level of around +/-60mA peak the RCD device shall switch off the AC relays and the error shall be latched. The signal is low pass filtered at around 1kHz to blank out transients (large X-cap and max. grid inductance: sqrt(5mH x 1uF) = 70us equals fres = 2.2kHz).

The error latch is also set at RCD sensor error, the set input is dominant over the reset input.

The error latch is also supplied from 5V_RCD to have independence from the DSP supply.

At startup condition, the error latch shall be set for security reason. The DSP can reset this latch only, if the hardware window watchdog detects error-free operation of the DSP.

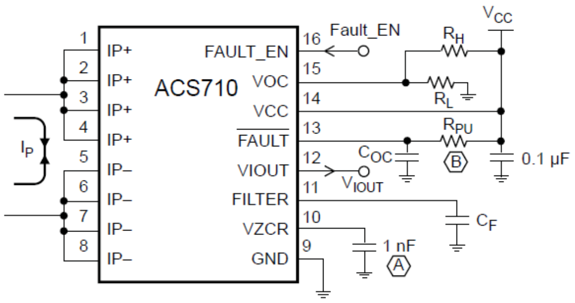
This functionality together with the parallel RCD SW protection leads to a safe system.



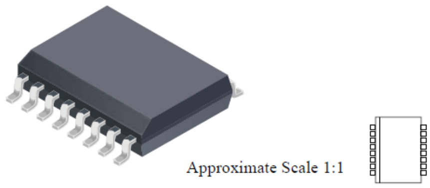
4.2 Current sensors

With the following measurements it shall be verified if the ACS710 sensor family is suitable for this application. The sensors can be placed outside the chokes, no dv/dt requirements!

The ACS710 is available for 6Arms, 12Arms and 25Arms which would be a suitable for this power range and is extremely compact.



Package: 16-pin SOIC Hall Effect IC Package (suffix LA)

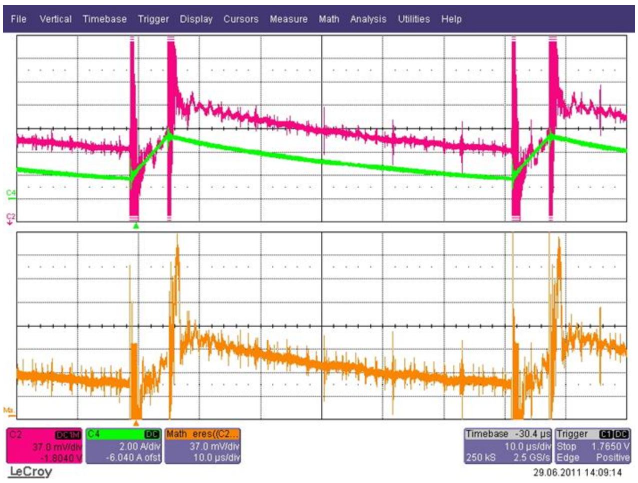


From Allegro semicondutor datasheet ACS710.

4.2.1 Operation of ACS710-25 (25A sensor)

- ➔ Operation of Eval board ASEK710LLA-25CB on SIC MOSFET testbench
- ➔ 18.5mV / A with Vcc =3.3V
- ➔ The MOSFET switches with ~24V/ns, the disturbance is acceptable with this slope

400V, 3.5Arms:



C2: Vout

C4: Phase current with current probe [2A/Div]

Ma: Vout – Vzcr [37mV/Div eq. 2A/Div]

400V, 20Arms:

C2: Vout

C4: Phase current with current probe [5A/Div]

Ma: Vout – Vzcr [92mV/Div eq. 5A/Div]

- ➔ The MOSFET switches with 24V/ns, the disturbance is acceptable with this slope (scope probes with standard GND-strips are used only)

4.2.2 Operation of ACS710-06 (6A sensor)

- ➔ Operation of Eval board ASEK710LLA-25CB on SIC MOSFET testbench
- ➔ 100mV / A with Vcc =3.3V
- ➔ The MOSFET switches with ~24V/ns, the disturbance is acceptable with this slope

400V, 8.25Arms

400V, 6.5Arms, first OC trip

C2: Vout

C3: /Fault (overcurrent level programmed at ~11Apeak)

C4: Phase current with current probe [2A/Div]

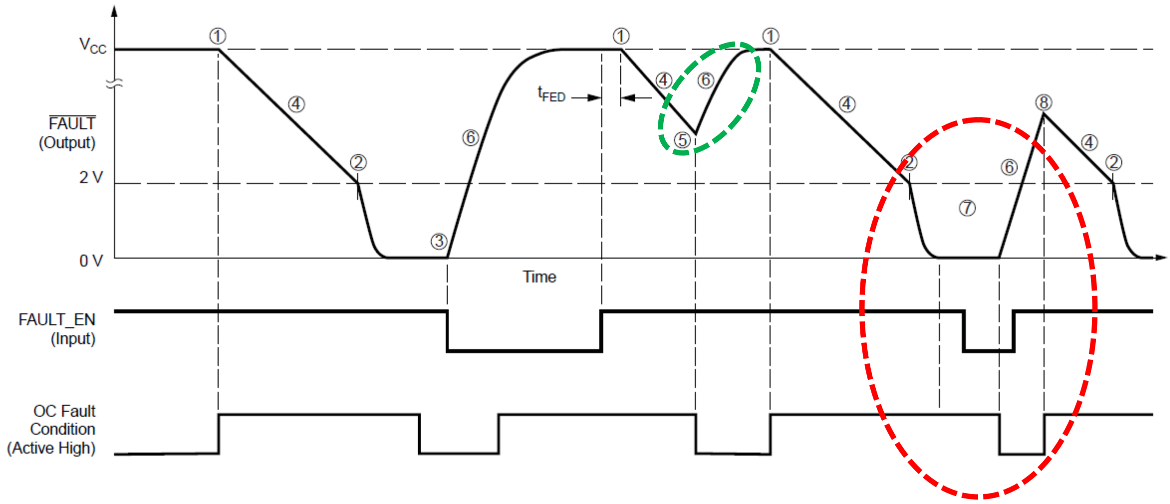
Ma: Vout – Vzcr [200mV/Div eq. 2A/Div]

- ➔ C8 has to be populated for good overcurrent level stability (2.2uF used) on the Eval board
- ➔ On the left, the OC fault is resetted with every turn-on glich → Right picture C=47nF on pin Fault_EN
- ➔ The current signal is still available after OC fault trip
- ➔ Simple and smart circuit needed to reset the OC fault after OC trip

4.2.3 Control logic around current sensor, possibility 1 (not realised)

The current sensor ACS710-x has overcurrent functionality that means the following for the logic around it:

- The current sensor indicates the overcurrent condition by the /FAULT output
- If the /Fault output is set, it has to be enabled again and by a low FAULT_EN pin
    - After the reset overcurrent errors are ignored for 15us typical



To implement a pulse-by-pulse current limit the following strategy could be implemented:

- A first overcurrent path shall block the IGBTs before the current sensor gets latched. For this the trip shall be during the programmable overcurrent delay by Coc.
- Immediately after the overcurrent condition the IGBTs are released again.

For severe overcurrent conditions where the sensor gets latched the following could be implemented:

- The IGBTs shall be blocked immediately.
- To reset the sensor the /FAULT signal is used. Like this the fault is cleared locally.
- The IGBTs shall not be enabled for about 20us to wait for the overcurrent functionality to be enabled again after a latch condition.

The two functions could be realised by detecting the level of the /Fault output pin.

Not good in this solution:

- Switching frequency in peak current mode is controlled by delays, not by a current hysteresis – this will result in a non-optimal current shape in peak mode. This is an important feature in applications with small inductances and large current ripple.
- Severe error is not latched by HW

4.2.4 Control logic around current sensor, possibility 2 (preferred)

The overcurrent signal shall be generated externally of the current sensor and thus a hysteresis on the current fault can be implemented. The latched overcurrent signal of the sensor is therefore only used for severe failures or in applications where the peak current mode is not populated.

The overcurrent signal is latched in every current sensor. If one sensor trips the whole converter (AC or DC) shall be blocked. After release of the failure through the microcontroller the gate signals shall be blocked for further 20us to allow the sensor to be ready again (delay time t_{FED} in the datasheet of ACS710).

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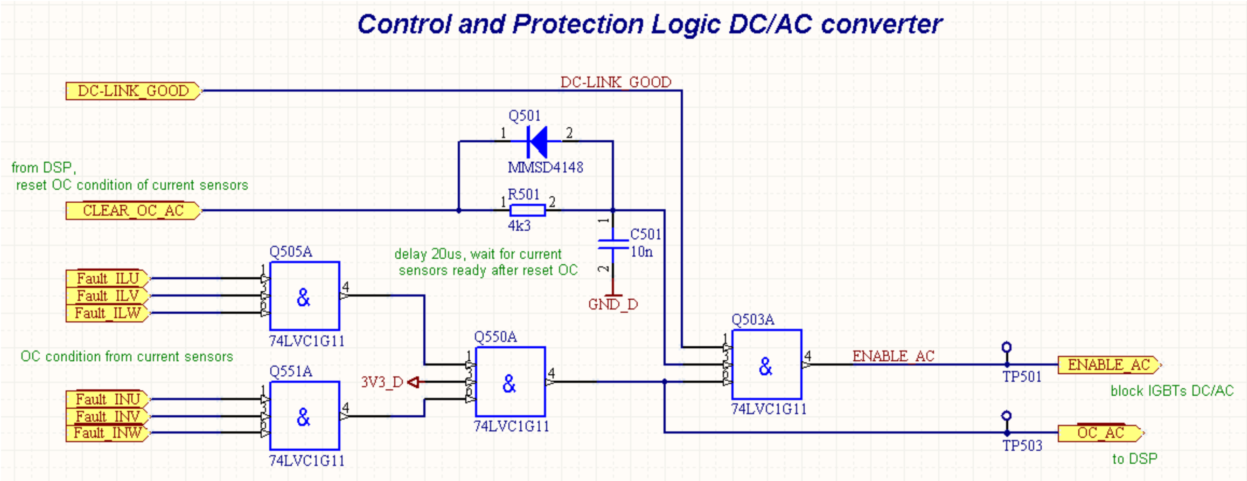


RC Calculation:

$$V_{CC} = 3.3V, V_{IH} = 2.0V,\ V_{IL} = 0.8V$$

with

$$U_C = U_0\left(1 - e^{\frac{-t}{\tau}}\right)$$

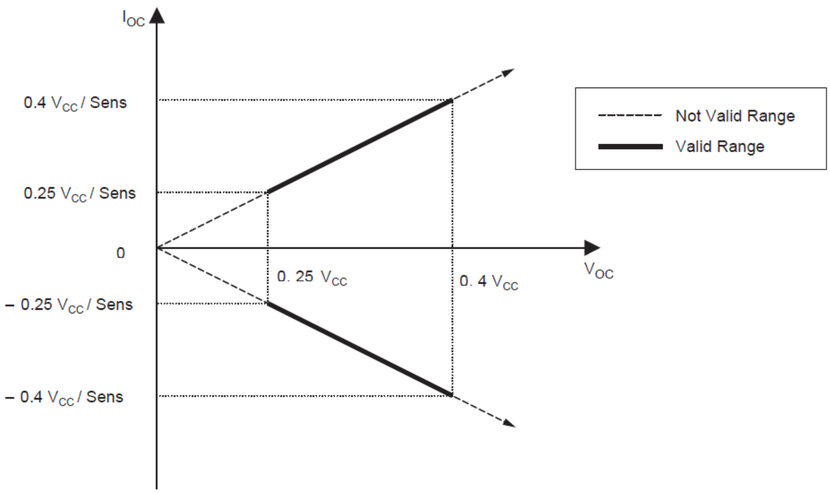
$$\tau = \frac{t}{\ln\left(\frac{V_{IH}}{V_{CC}}\right)} = \frac{20 \cdot 10^{-6}}{\ln\left(\frac{2}{3.3}\right)} \approx 40 \cdot 10^{-6}$$

Choosing

$$C \ = \ 10nF \rightarrow R \geq 4k\Omega$$

The trippoint for the ACS710 sensor can only be set between 0.25…0.4 x Vcc. In our case Vcc is 3.3 V. This leads to tripvoltage of 0.825V…1.32V.

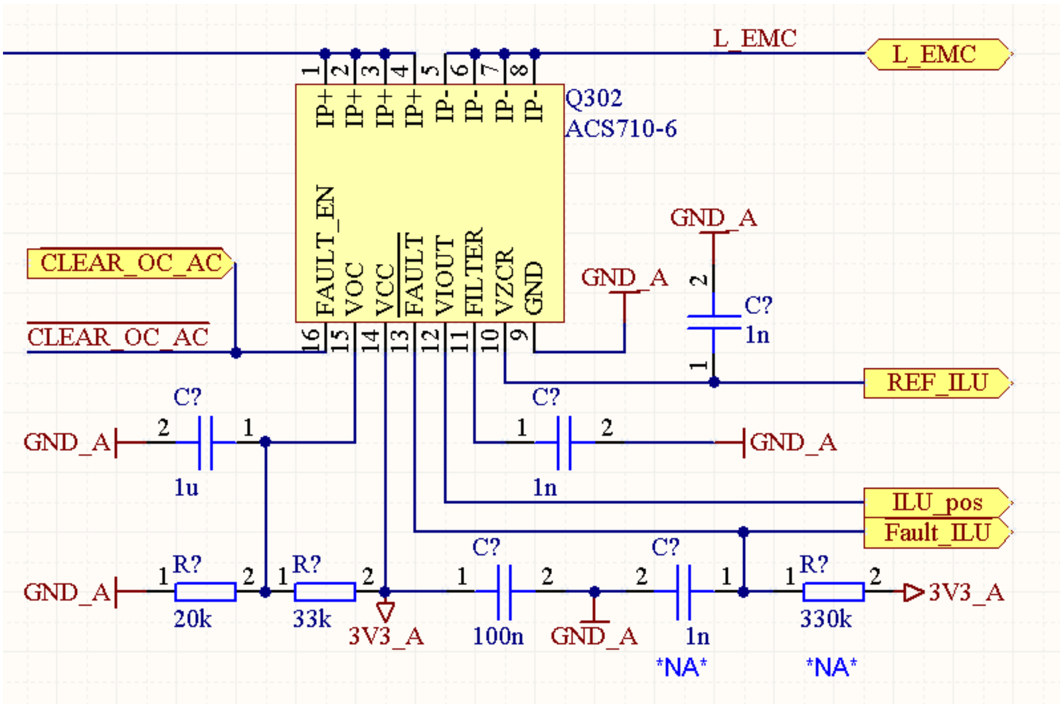
I_{OC} versus V_{OC}



The tripvoltages for the ACS710 are:

$$V_{OC_{severe}} = \pm A_{Peak} \cdot Sensitivity_{@3.3V} = \pm 12.5A \cdot 0.1 = \pm 1.25V \quad \rightarrow 38\%\ of\ VCC \rightarrow\ OK$$

Version	Sensor	Sensitivity @3.3 VCC	OC trip ACS	R divider high	R divider low
1kW	ACS710-6	100 mV/A	12.5Apeak	33k	20k



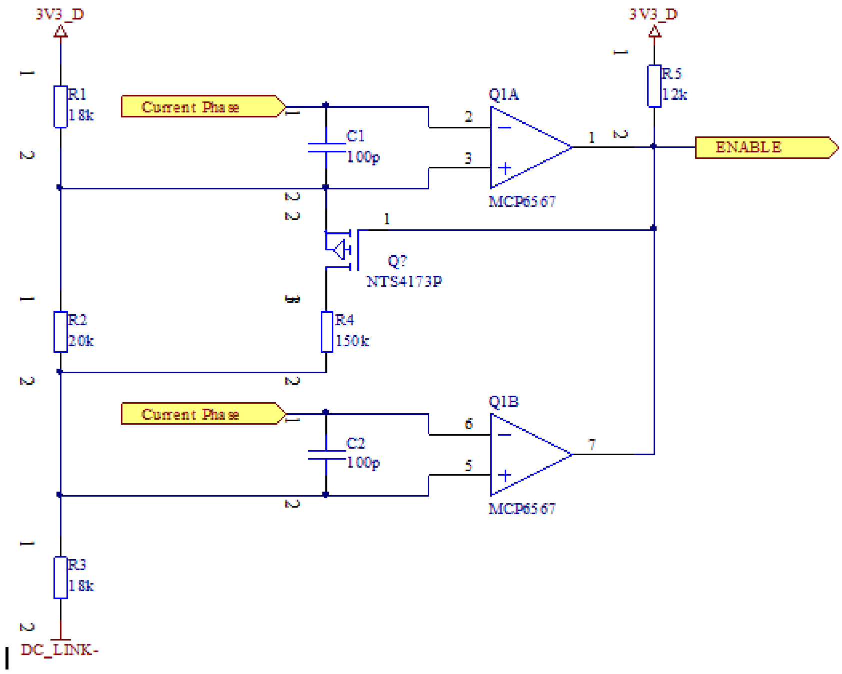
The currents in the L phase and the DC output are measured positive, the currents in the N phase are measured negative. Like this N and L currents from the same PWM outputs can be averaged toghether by resistors only.

All the reference signals of the DC/AC converter are summed together the same way.

4.2.5 Peak current limiting

To realise the pulse-to-pulse current limit the internal overcurrent signal of the current sensor is difficult to use, because there is no hysteresis built in. Therefore, a cost effective double comparator per current sensor shall be used to generate this function.

The MCP6567 is a rail-to-rail open-drain comparator with 10mV maximum offset voltage. The PMOS NTS4173 has a gate threshold voltage that is smaller than 3.3V/2.



The tripvoltages for the window comparator are:

$$V_{OC_{trip}} = \frac{V_{CC}}{2} \pm A_{Peak} \cdot Sensitivity_{@3.3V} = \frac{3.3}{2} \pm 11 \cdot 0.100 = 1.65 \pm 1.1V$$

The releasevoltages for the window comparator are:

$$V_{OC_{rel}} = \frac{V_{CC}}{2} \pm A_{Peak} \cdot Sensitivity_{@3.3V} = \frac{3.3}{2} \pm 8.8 \cdot 0.100 = 1.65 \pm 0.88V$$

Dimensioning resistors for overcurrent thresholds:

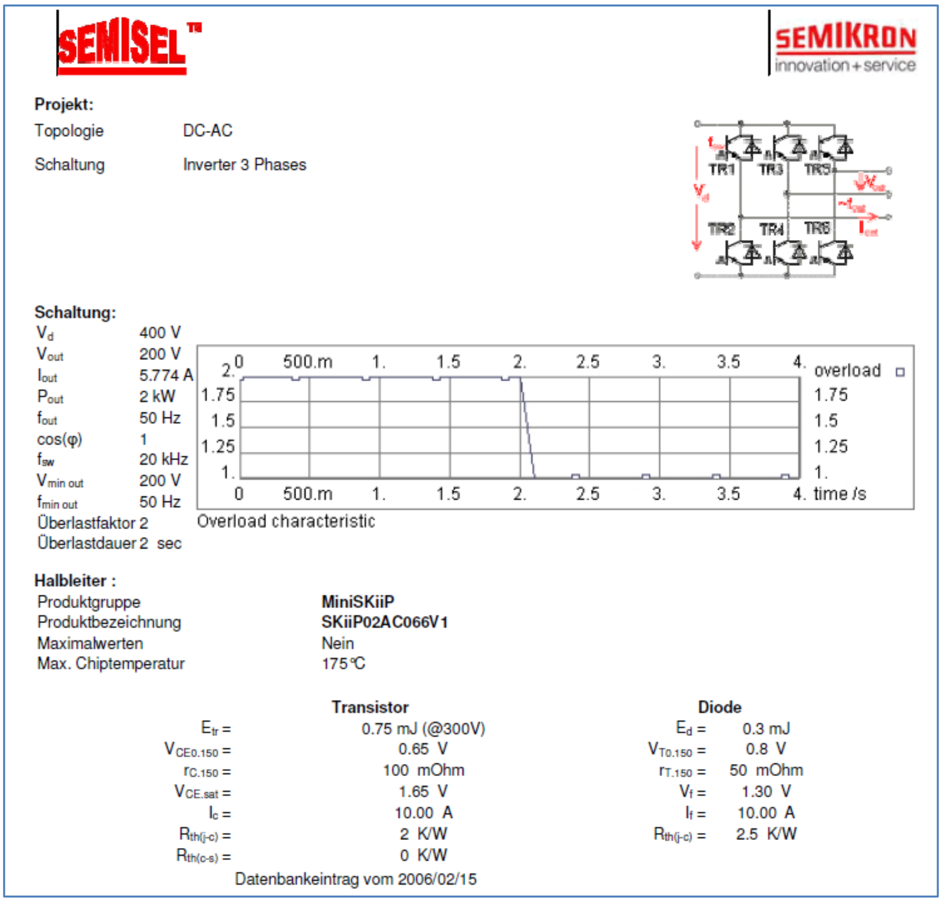
Peak current	Sensor	Sensitivity @3.3 VCC	OC trip Window	OC release (+20% Trip)	R divider high / low	R divider middle	R divider PMOS
11Ap	ACS710-06	100 mV/A	±11Apeak	±8.8Apeak	5k1	20k	27k

Each comparator shall block the corresponding half bridge or optionally also the half bridge of the other phase (L or N). This will lead to a behaviour like slow decay mode or fast decay mode during peak limiting and can be configured by a 0R resistor.

4.3 Losses IGBT modules

The IGBT module has been choosen according to different requirements described in [1], mainly robustness against heavy vibrations.

The losses of this IGBT family can be simulated with the online-simulation tool SemiSel at www.semikron.com. Every module has a current stress similar to a current stress of a standard 3-phase inverter with about 2kW load.

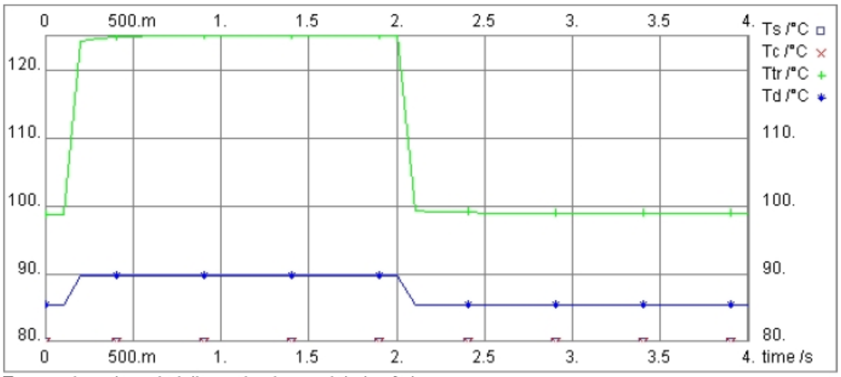


Kühlung:

Umgebungstemperatur	80°C
Anzahl der Schalter auf einem Kühlkörper	6
Anzahl parallel geschalteter Bauelemente auf dem Kühlkörper	1
Zusätzliche Wärmequelle auf dem Kühlkörper	0 W
Maximale Kühlkörpertemperatur	80°C

Berechneten Verluste und Temperaturen bei Nennstrom, bei Überlast und bei $f_{min\ out}$:

	Nennstrom	Überlast	f_{min} bei überlast
$P_{cond\ tr}$	2.74 W	8.04 W	8.09 W
$P_{sw\ tr}$	4.87 W	11 W	11 W
P_{tr}	7.61 W	19 W	19 W
$P_{cond\ d}$	0.51 W	1.25 W	1.25 W
$P_{sw\ d}$	1.33 W	2.10 W	2.12 W
P_d	1.84 W	3.35 W	3.37 W
P_{tot}	57 W	131 W	133 W
	Mittelwerte	Mittelwerte	Maximalwerte
T_h	80 °C	80 °C	80 °C
T_c	80 °C	80 °C	80 °C
T_{tr}	95 °C	117 °C	125 °C
T_d	85 °C	88 °C	90 °C



Temperature characteristic overload current during fmin

Bewertung:
Diese Konfiguration ist optimal.

IGBT Treibervorschlag

Name	Iout(av) /mA	Îout /A	Visol /kV	Vce max /V	Rgmin / Ohm	Kanäle
3x SKHI23/12 R	50	8	2.5	1200	2.7	2
1x SKHI61 R	20	2	2.5	900	10.0	6
3x SKYPER 32 R or SKYPER 32PRO R	50	15	4.0	1200	1.5	2

Zusätzliche Kennlinien für den nominalen Arbeitspunkt in Abhängigkeit vom freien Parameter - X:
Keine Auswahl erfolgt!

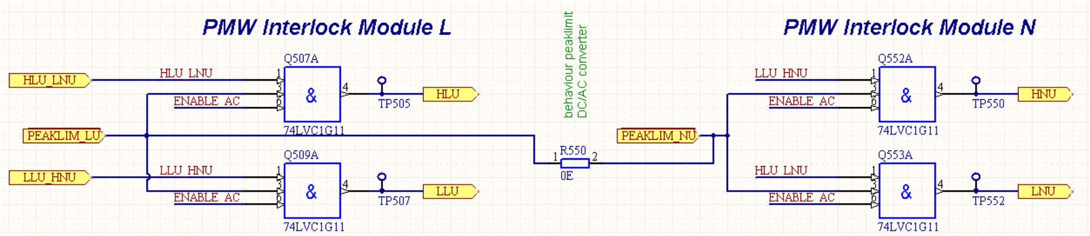
4.4 Protections IGBT modules

4.4.1 Protections related to PWM inputs

The 3 phase driver FAN7388 from Fairchild helps to realize the following protections:

- The dead time is controlled by the DSP, however, a minimal dead time of 400ns is forced by the driver.
- The IGBTs shall be driven from the DSP through a logic buffer to allow some HW-protections. For the current limiting functions the PWM inputs shall be blocked.
- An overcurrent signal from the current sensors shall block the whole IGBT Module directly, the failure shall be latched (in the current sensors) until the DSP clears the OC error.
- The HW supervision of the DC link voltage shall also block the buffer directly in case of a DC link voltage which is out of the valid range
- With the DSP28335 the PWM outputs GPIO0-11 have no pullup resistor activated when the chip is not programmed yet. A high output level of this pin means turn on the IGBT. **Pull-Down Resistor on PWM signals needed!**
- Optionally, a pulse-to-pulse current limit function shall be possible to populate on the PCB. This current limit feature only blocks the affected half bridge of the IGBT Module until the current is back in a valid range.

 drivetek ag, keltenstrasse 1, ch-2563 ipsach, phone +41 32 332 79 32, fax +41 32 332 79 31, www.drivetek.ch



Every IGBT module is driven through a 3-phase fullbridge driver FAN7388 from Fairchild semiconductor, like showed in the datasheet of FAN7388:

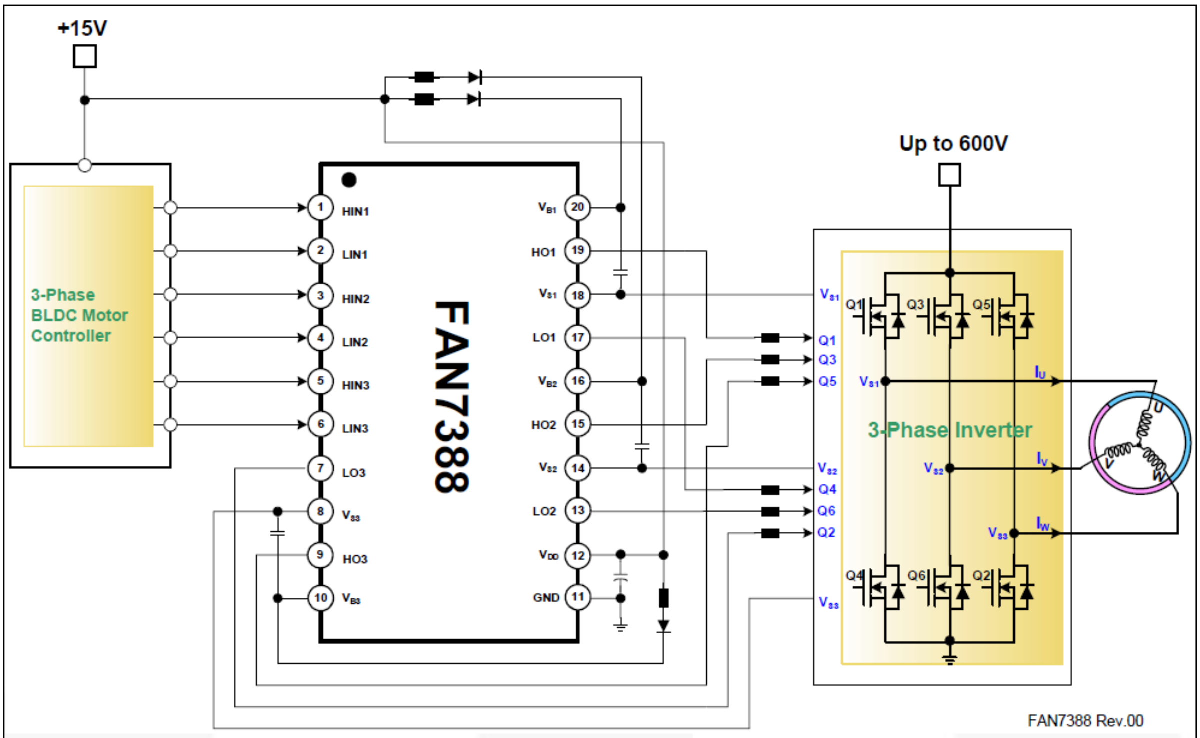


Figure 1. 3-Phase BLDC Motor Drive Application

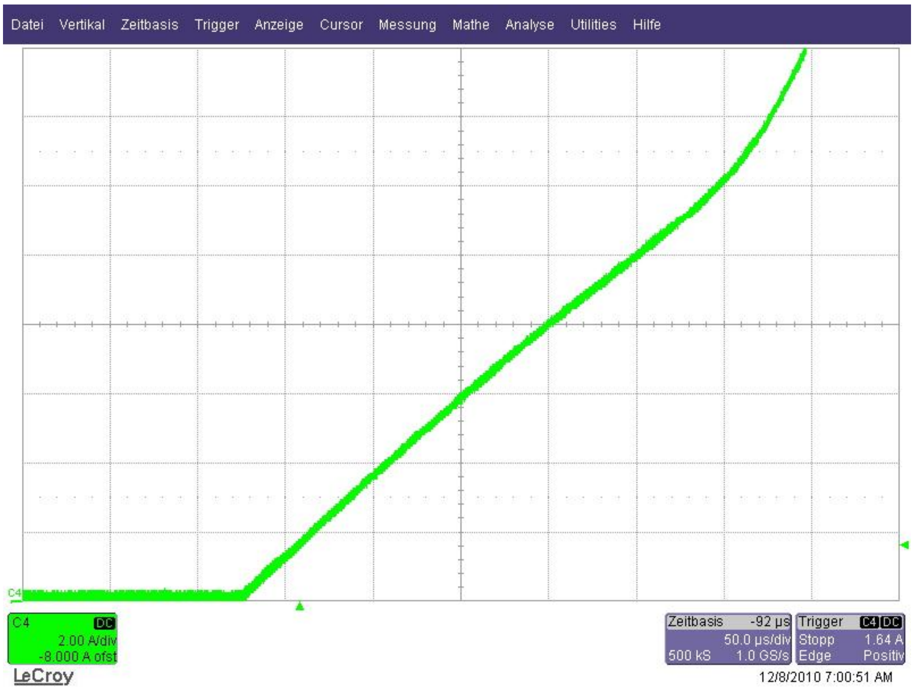
4.5 Chokes DC/DC and DC/AC

According to [1] an inductance of 500uH and >11A peak is required.

Minimal losses can be achieved with the following design:

- PQ40 core
- Litz wire 120x0.1, 80 turns

Measurement of the saturation level ~12Apeak:

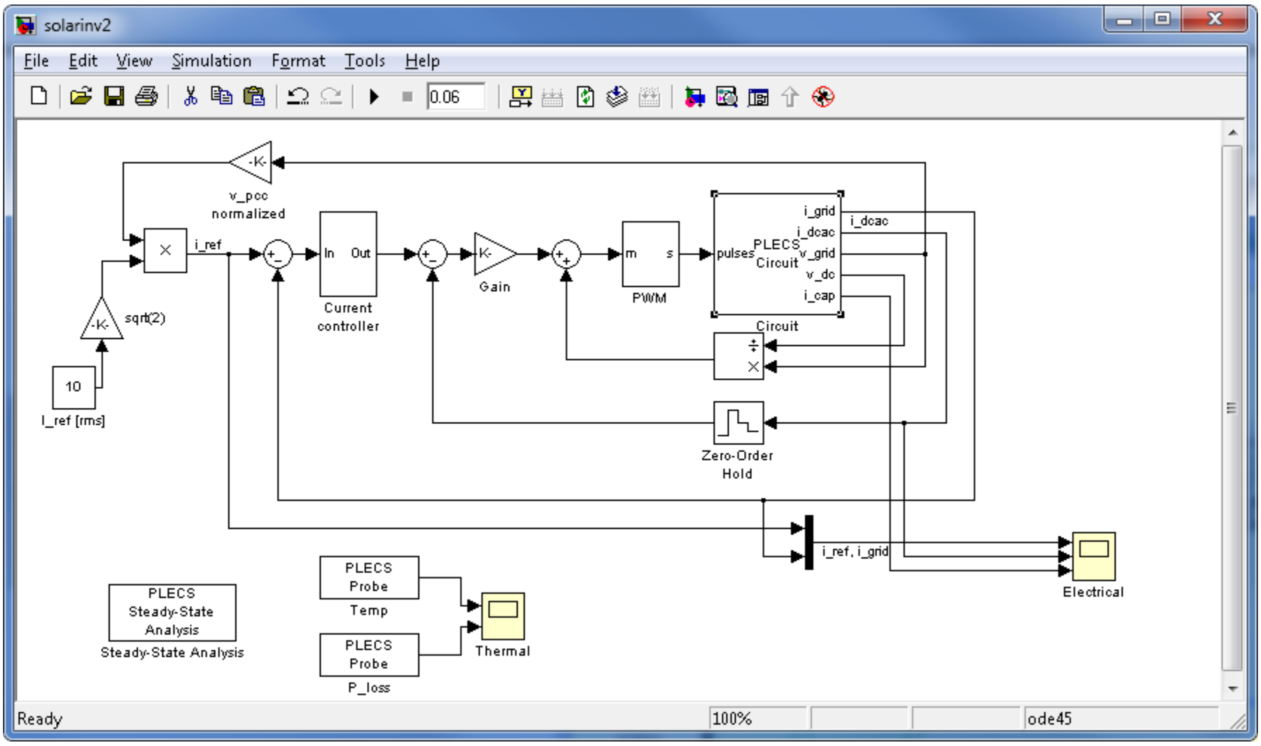


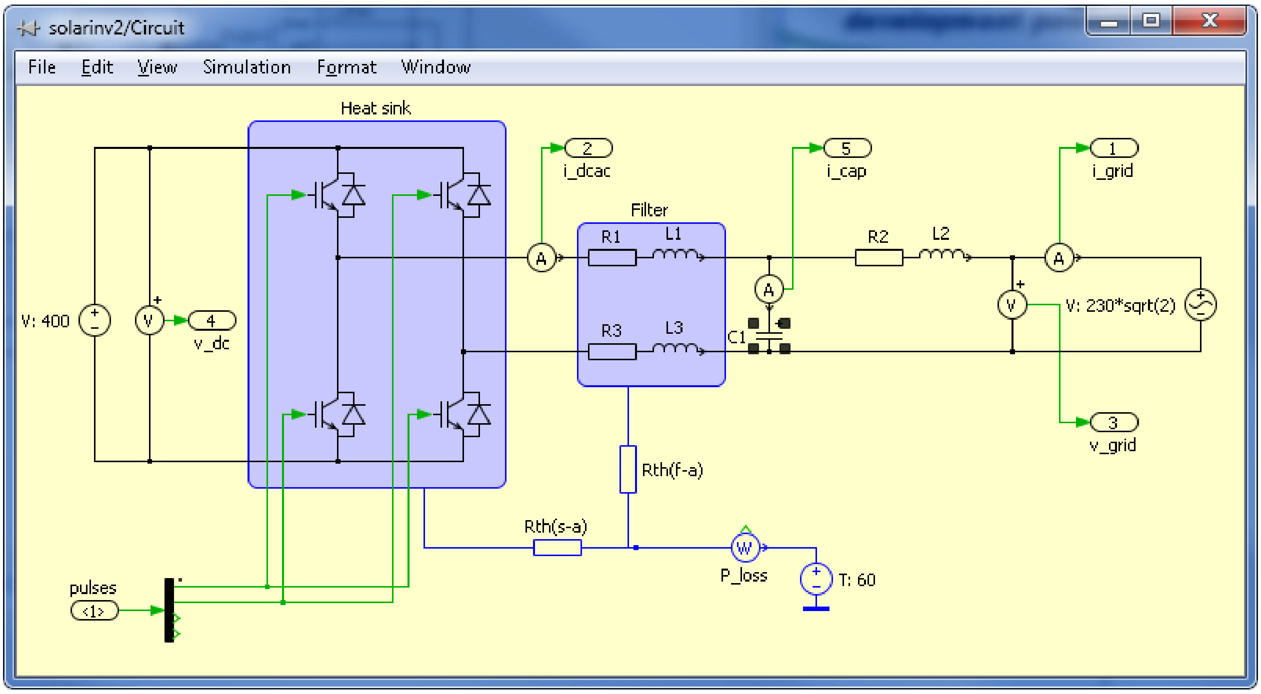
4.6 Output capacitor DC/AC converter

To determine the capacitor current a simulation example of a PLECS simulation software has been adapted to our needs.

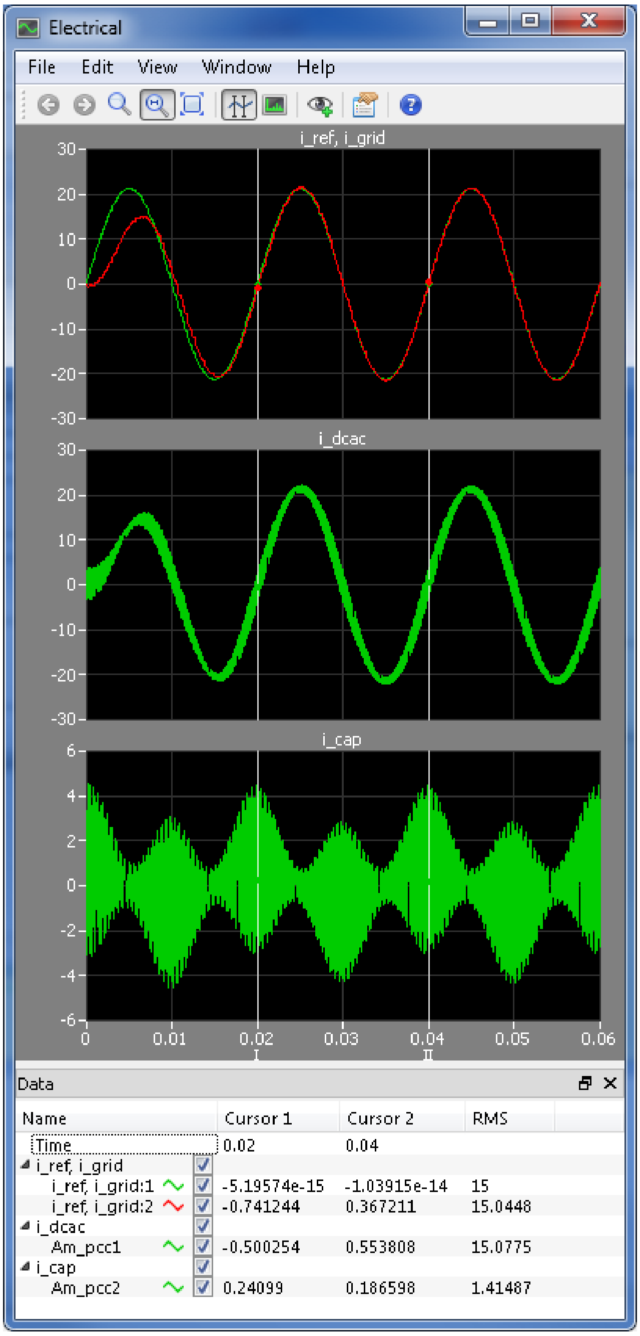
The PV inverter for power feedback to the public grid has been adapted to our needs:

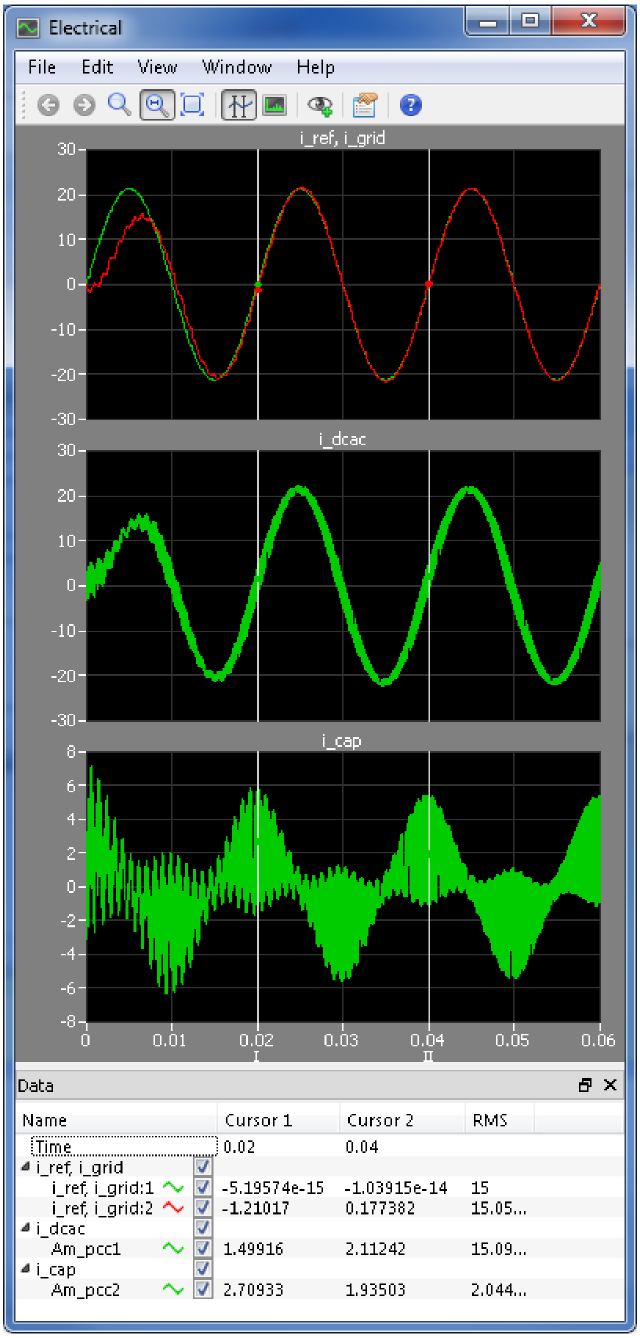
- Modulation scheme is 2-level modulation with 16kHz
- L1 / L3 is 1mH
- To get the maximum capacitor current, the impedance of the public grid has been set to L2=2.4mH, R2=1.2Ohm, see document [2]





3kW / 2x1mH / 6.6uF	3kW / 2x1mH / 20uF
Icap = 1.43Arms	Icap = 2.03Arms





By increasing the cap from 6.6uF to 20uF the calculated 50Hz current of the cap on the public grid increases from 0.48Arms (50Hz) to 1.44Arms (50Hz).

- ➔ Not significantly more ripple current (16kHz) is carried in the larger capacitor, it stays similar. Mainly the reactive current component increases.
- ➔ The capacitor can be choosen in this capacitance range and must be suitable for the above rms currents

4.6.1 Pulse handling capacity of EMI X-capacitors

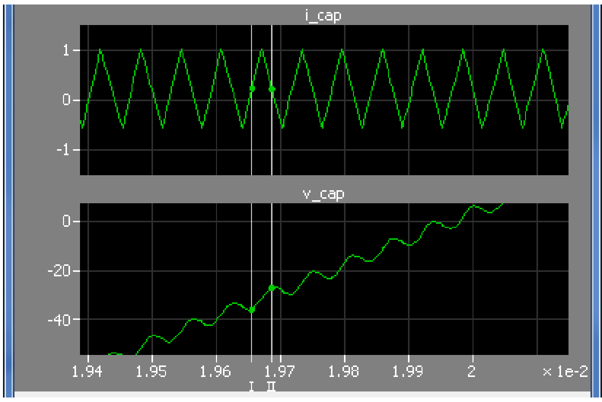
The X-capacitors of the EMI filter could have to carry the ripple current directly without being overloaded.

The X2 Series B32923 from Epcos defines the following maximum pulse values:

dV/dt and k_0 values

Lead spacing	22.5 mm	27.5 mm	37.5 mm	52.5 mm
dV/dt in V/µs	140	100	70	40
k_0 in V²/µs	120 400	86 000	60 200	34 400

The simulation above shows the following dv/dt near the zero crossing of the AC voltage, where the ripple voltage is at its maximum:



Data

Name		Cursor 1	Cursor 2	Delta
Time		0.0196563	0.0196875	3.125e-05
i_ref, i_grid				
i_ref, i_grid:1		-0.762137	-0.693086	-0.0690513
i_ref, i_grid:2		-2.97249	-2.89986	-0.0726279
i_dcac				
Am_pcc1		-2.74609	-2.67924	-0.0668515
i_cap				
Am_pcc2		0.226397	0.220621	0.00577643
v_cap				
Vm_pcc1		-35.9049	-27.0349	-8.87007

dv/dt = 8.9V / 31.25us **= 0.29V / us**

→ single pulse ratings are not critical

According to general technical informations from Epcos the k_0 value expresses the heating due to current applied to the cap. For repetition rates larger than 10kHz an adequate margin is recommended.

On the other hand, k_0 can be calculated by a piecewise linear decomposition, comprising ΔV - Δt segments

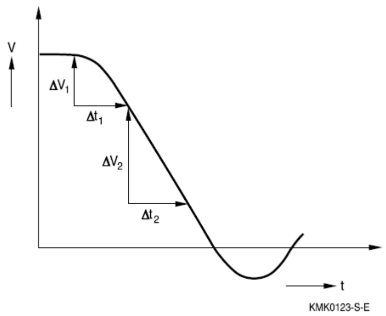


Figure 27
Piecewise linear approximation of a voltage pulse

$$k_0 \approx 2 \cdot \left(\Delta V_1 \cdot \frac{\Delta V_1}{\Delta t_1} + \Delta V_2 \cdot \frac{\Delta V_2}{\Delta t_2} + \ldots\right)$$

Assuming that this dv/dt value is present for about 5ms with 50% duty cycle, k0 can be approximated as a voltage slope:

Voltage change in 5ms:

dt1 = 5ms

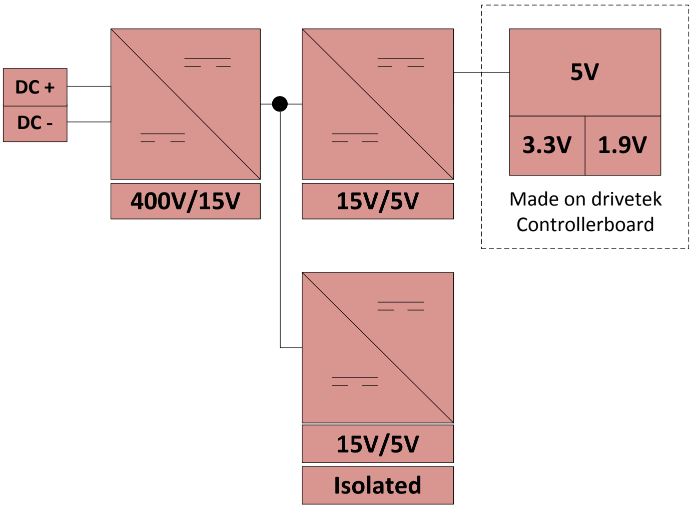
dv1 = 0.29V/us * 5000us = 1450V

k_0 = 2 x1450V x 1450V/5000us = 850V²/us

→ The margin seems to be adequate

- → From these large margins on pulse handling it is assumed that also other brands of MKP X2 capacitors will be suitable to carry this ripple current.
- → The two-stage EMI Filter will be built with 2.2uF X2 capacitors
- → On the output of the Smoothing chokes two additional 2.2uF X2 capacitors will be placed
- → If on the layout the width of 14mm instead of 13.2mm can be left, the 3.3uF type B32924E3335M can be populated also

4.7 Supply Design



4.7.1 Power Consumption Estimation

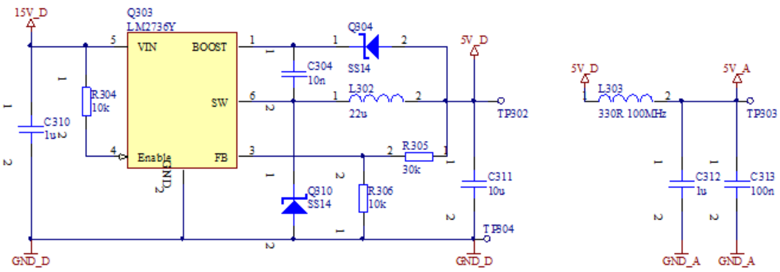
Supply	Output Power	Efficiency	Input Power	Standby Power
15V	5.3W	72%	7.3W	5W
5V	3.0W	85%	3.5W	3W
5V Isolated	100mW	72%	140mW	-
3.3V	1W	80%	1.25W	0.8W
1.9V	0.7W	80%	0.875W	0.7W

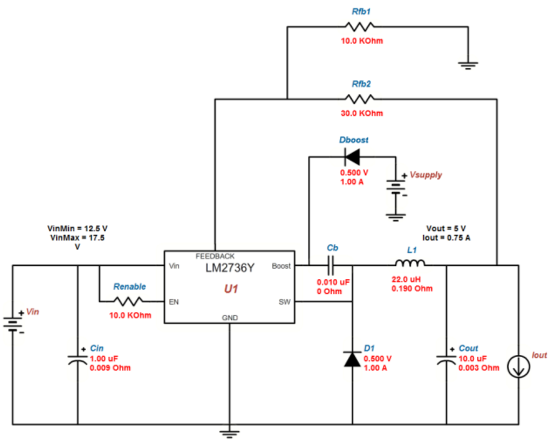
4.8 15V Supply

Details flyback converter see in document [1].

4.9 5V Supply

Design with National Instruments Webench using LM2736Y 750mA Buck Regulator.





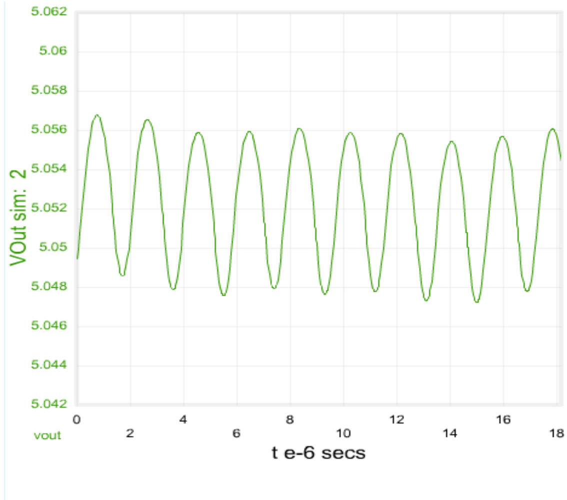
Simulated Circuit

Features:

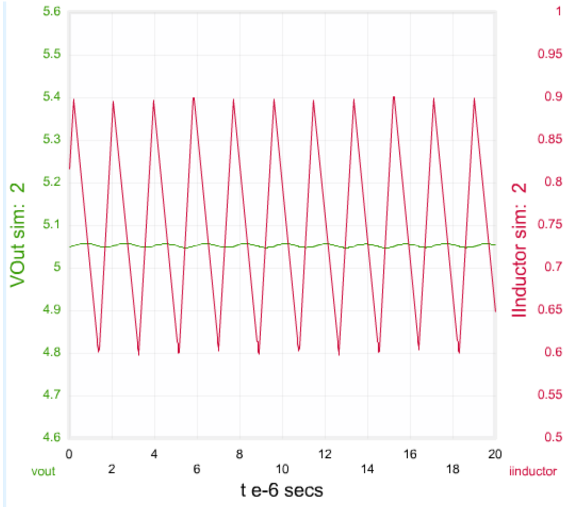
Maximal Input Voltage: <18V

Output Voltage: 5V ± 5%

Output Current: max 750 mA



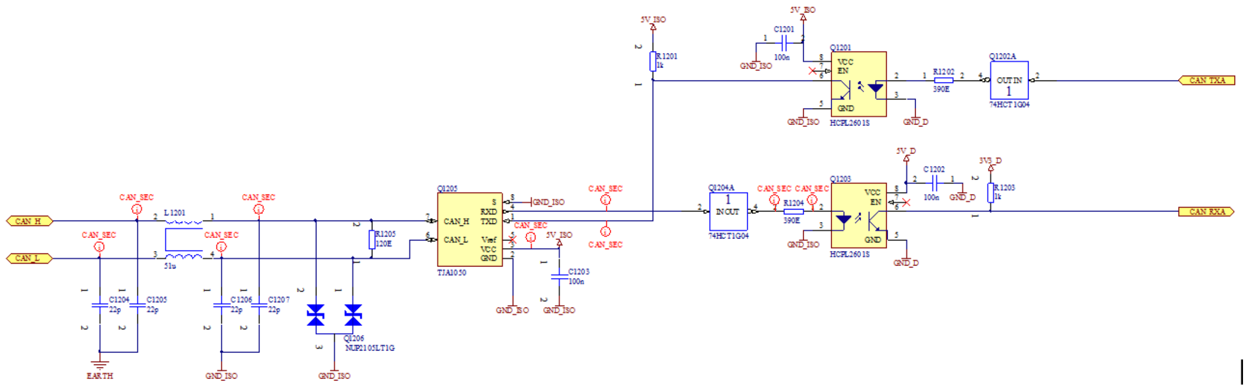
Output Voltage Ripple



Inductor Current

4.10 CAN Interface

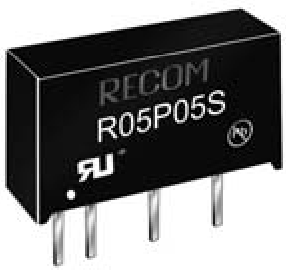
The CAN interface will be implemented with TJA1050 of NXP. The circuit has been used in several projects already:



4.10.1 5V Supply for isolated for interface

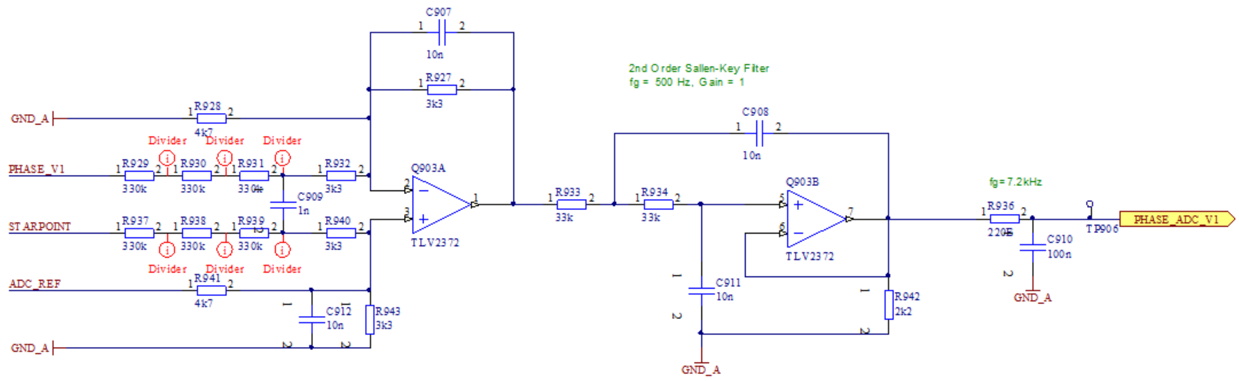
DC/DC-Converter 1 Watt SMD R15P05S/R6.4 from Recom fulfils the requirements:

Key Features:
Input Voltage 15V
Outputvoltage 5V
Outputt Current 200mA
Reinforced Isolation 6.4kVDC
MTBF 2974 x 10^3 hrs @25°C



4.11 Phase Voltage Measurement

4.11.1 Measurement Phase X to DC-



Maximal ADC Voltage is 3 Volt, and the maximum Phase Voltage is

$$230V \cdot 1.2 \cdot \sqrt{2} = +/-390.3V$$

Phase Voltage needs to be divided by a Factor of Minimum 260.

$$Gain = \frac{R_{904}}{(R_{909} + R_{910} + R_{911} + R_{912})} = \frac{3.3k}{(330k + 330k + 330k + 3.3k)} = 3.32 \cdot 10^{-3}$$

$$\frac{1}{Gain} = \frac{1}{3.32 \cdot 10^{-3}} = 301$$

To have a symmetrical output we need to add a offset of 1.5V.

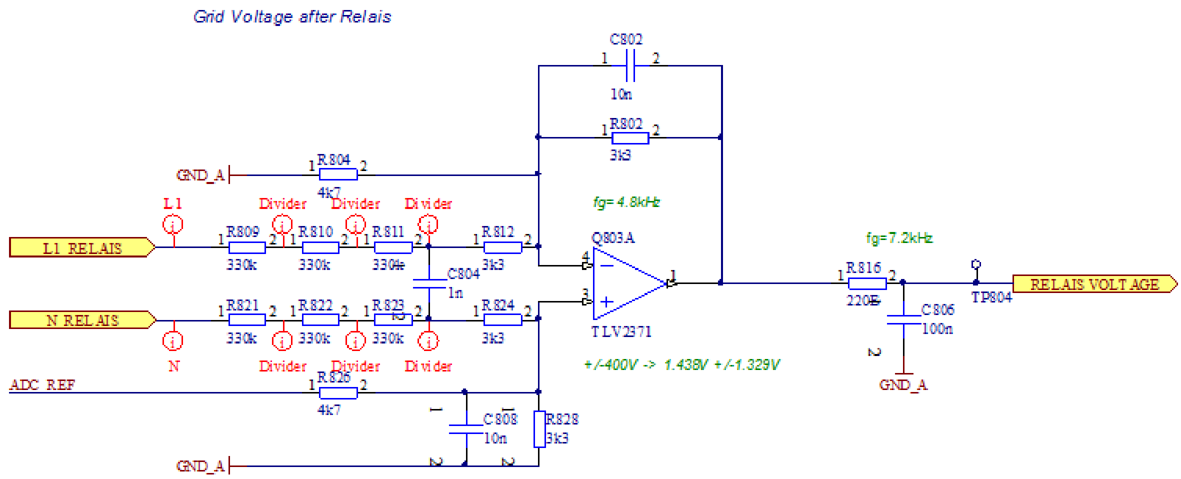
$$R_{924} = R_{926} \cdot \frac{V_{REF}}{1.5} = 3.3k \cdot 1.365 = 4.5k \rightarrow \; E24 = 4.7k$$

+/-400V -> 1.438V +/-1.329V

To fulfil all coefficient conditions in [4] we need to subtract 0V with the same gain

$$\frac{R_{905}}{R_{904}} = \frac{R_{924}}{R_{926}} with\ R_{901} = R_{926} \rightarrow R_{902} = R_{921} = 4.7k$$

4.11.2 AC Relays Voltage Measurement



The same circuit will be implemented after the relays.

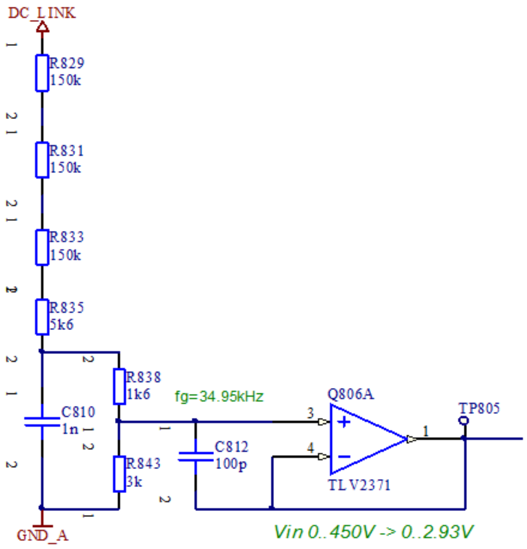
4.12 DC-Link Voltage Measurement

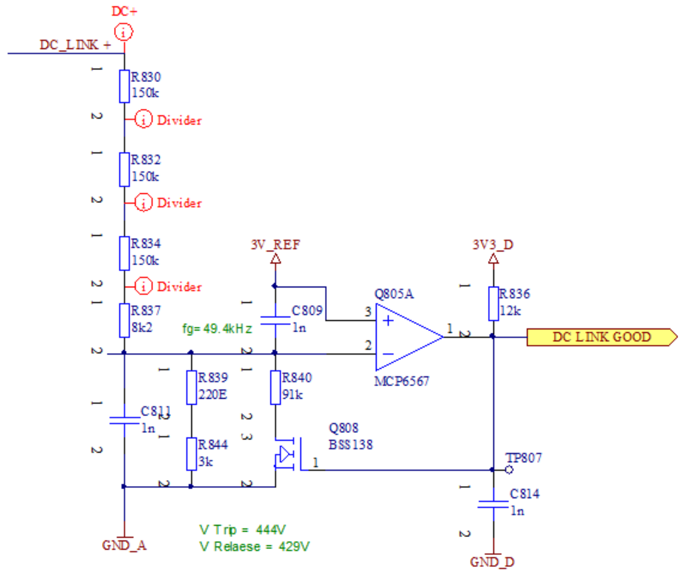
The measurement principal is a simple voltage divider with a voltage follower (see left figure below). The maximal ADC Input value is 3V. The Maximal DC Voltage is 450V.

Calculation:

$$\frac{U_{DC}}{U_{ADC}} = \frac{R_{TOT}}{R_{835}} = \frac{450}{3}$$

The high voltage will be divided with 3x150k in a 1206 Case. The ADC Value for 450VDC is 2.933V





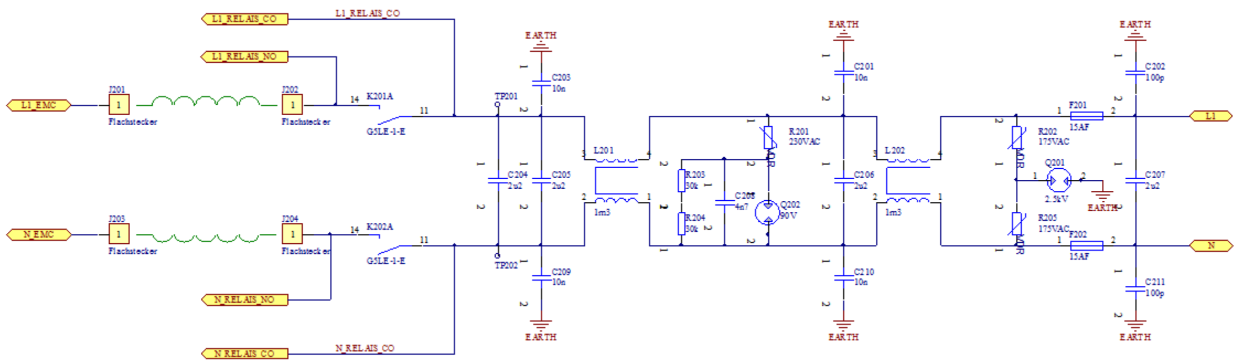
Additionally is a DC-Link Measurement with a overvoltage trip comparator placed. The Levels are:

$$U_{Trip} = 3 \cdot \frac{R_{830} + R_{832} + R_{834} + R_{837} + ((R_{839} + R_{844})//R_{840}))}{((R_{839} + R_{844})//R_{840}))} = 444V$$

$$U_{Release} = 3 \cdot \frac{R_{830} + R_{832} + R_{834} + R_{837} + R_{839} + R_{844}}{R_{839} + R_{844}} = 429V$$

4.13 EMI filter AC connection

To the public grid a two stage common mode EMI filter shall be used for sufficient damping:

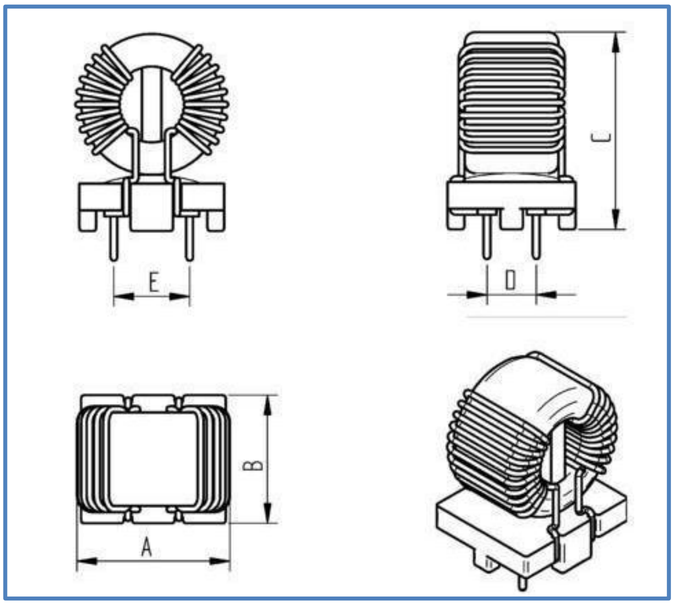


 drivetek ag, keltenstrasse 1, ch-2563 ipsach, phone +41 32 332 79 32, fax +41 32 332 79 31, www.drivetek.ch

4.13.1 Common mode chokes

The CMB-series from Wuerth shall be used due to vibration requirements.

As a maximum configuration the XXL size for 20A is placed on the layout. The footprint shall be flexible to accommodate also the sizes L and XL. If possible, less inductance can be populated to save cost if less dumping is needed:

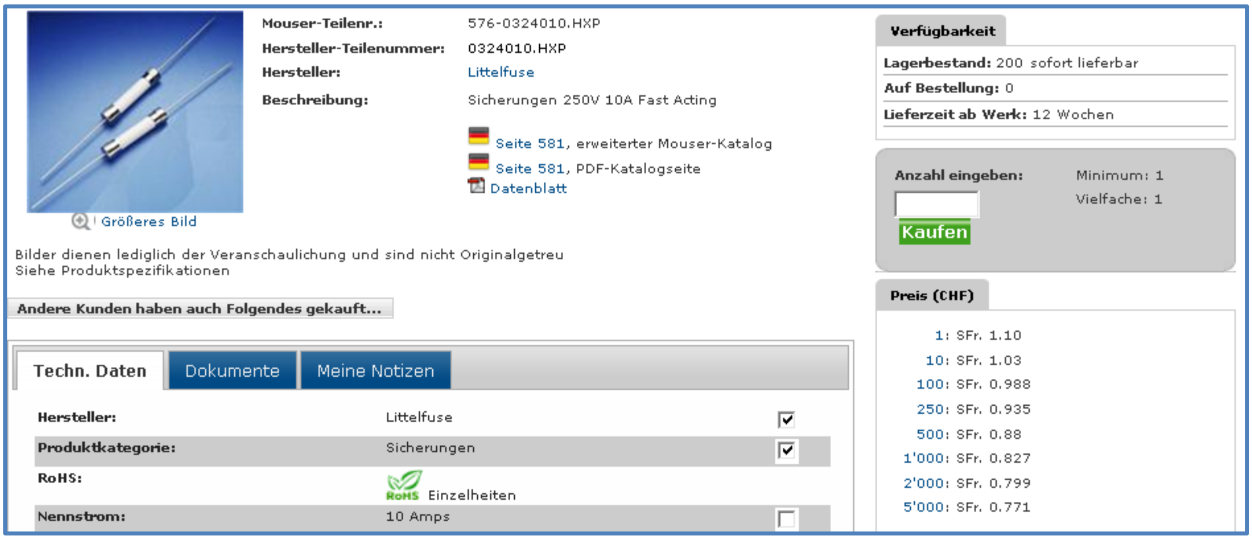


Bauform	A (mm)	B (mm)	C (mm)	D (mm)	E (mm)
Type XS	15.0	7.5	18.0	4.5	10.0
Type S	17.5	13.0	22.0	5.0	7.7
Type M	25.0	17.0	28.0	10.7	7.5
Type L	27.5	18.5	33.0	12.0	10.0
Type XL	30.0	22.0	35.0	15.0	25.0
Typ XXL	42.0	23.5	41.0	18.5	10.5

4.14 Fuses Grid

A fast acting ceramic fuse shall be used to protect the electronics from large short circuit currents. It would be possible to use a 5x20mm fuse, but there is less flexibility at large current values.

Therefore a good and cost effective standard 6.3x32mm fuse is used. The Littelfuse 324 series that can be soldered to the PCB directly.



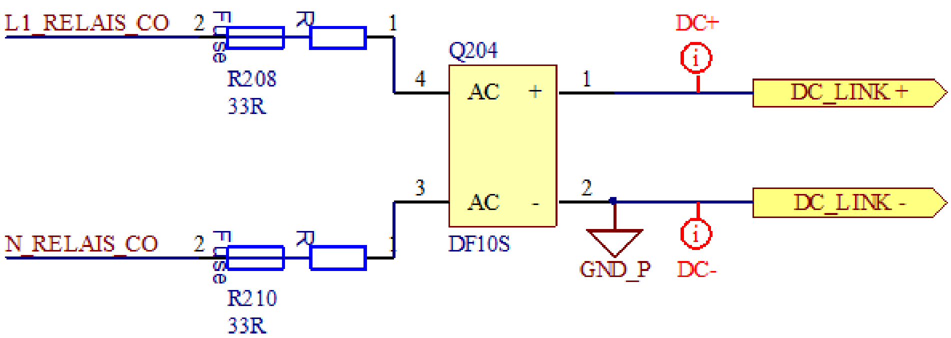
Grid fuses 20A 0324020.HXP

4.15 Inrush limiter

4.15.1 Fused inrush resistor

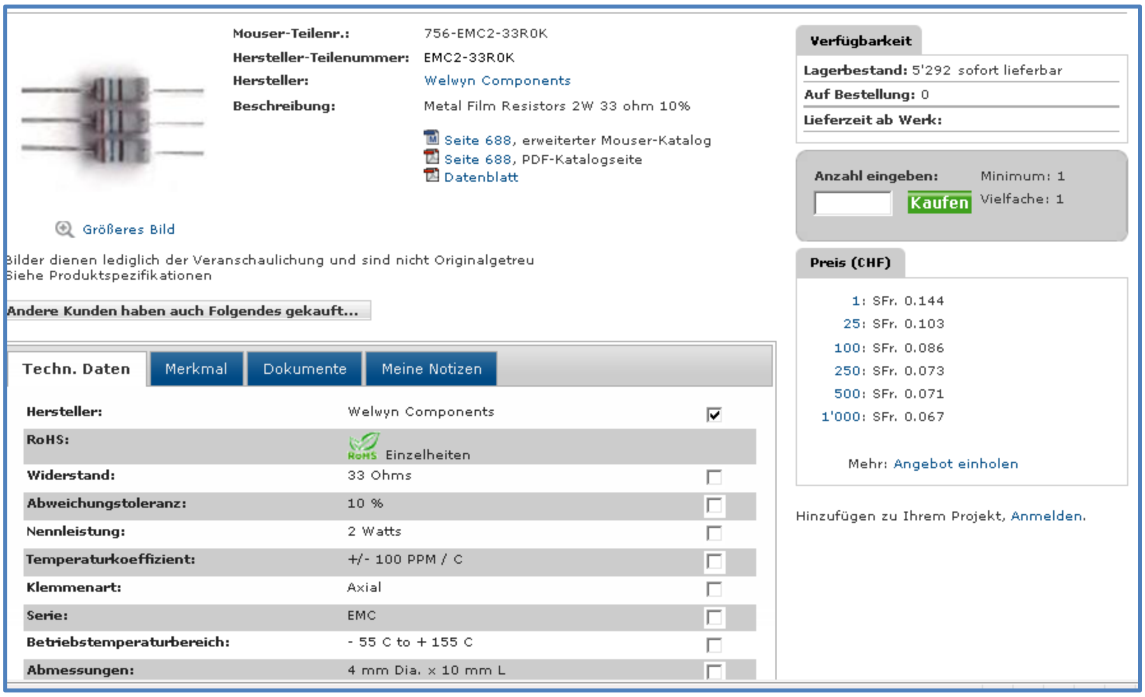
The inrush limiter will charge up the DC link as soon as an AC grid is connected. The auxiliary supply will run permanently. To guarantee safety fusible resistors must be used that will open, if the DC link has a short circuit or the current will increase because of a defect.

A symmetric circuit is preferred to charge up the DC link, because smaller and therefore more cost effective elements can be used.



It would be possible to leave away one resistor, but the peak power will increase.

A cost effective part should be suitable for the pulse handling:


Mouser-Teilenr.: 756-EMC2-33R0K
Hersteller-Teilenummer: EMC2-33R0K
Hersteller: Welwyn Components
Beschreibung: Metal Film Resistors 2W 33 ohm 10%
Seite 688, erweiterter Mouser-Katalog
Seite 688, PDF-Katalogseite
Datenblatt
Größeres Bild
Bilder dienen lediglich der Veranschaulichung und sind nicht Originalgetreu
Siehe Produktspezifikationen
Andere Kunden haben auch Folgendes gekauft...

Verfügbarkeit
Lagerbestand: 5'292 sofort lieferbar
Auf Bestellung: 0
Lieferzeit ab Werk:

Anzahl eingeben: Minimum: 1
Kaufen Vielfache: 1

Preis (CHF)

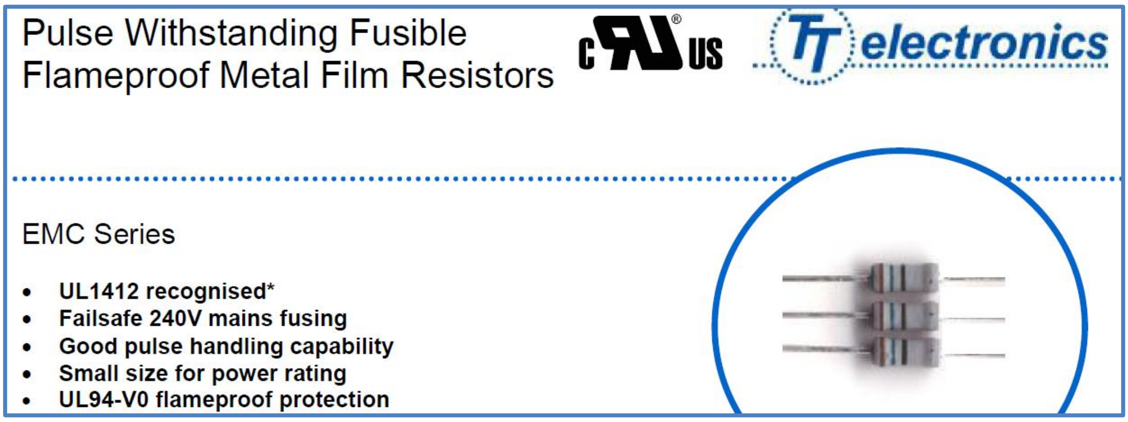
1:	SFr. 0.144
25:	SFr. 0.103
100:	SFr. 0.086
250:	SFr. 0.073
500:	SFr. 0.071
1'000:	SFr. 0.067

Mehr: Angebot einholen
Hinzufügen zu Ihrem Projekt, Anmelden.

Techn. Daten | Merkmal | Dokumente | Meine Notizen

Hersteller:	Welwyn Components
RoHS:	Einzelheiten
Widerstand:	33 Ohms
Abweichungstoleranz:	10 %
Nennleistung:	2 Watts
Temperaturkoeffizient:	+/- 100 PPM / C
Klemmenart:	Axial
Serie:	EMC
Betriebstemperaturbereich:	- 55 C to + 155 C
Abmessungen:	4 mm Dia. x 10 mm L

The part is intended for precharging from the public AC line:


Pulse Withstanding Fusible Flameproof Metal Film Resistors
c UL us TT electronics

EMC Series

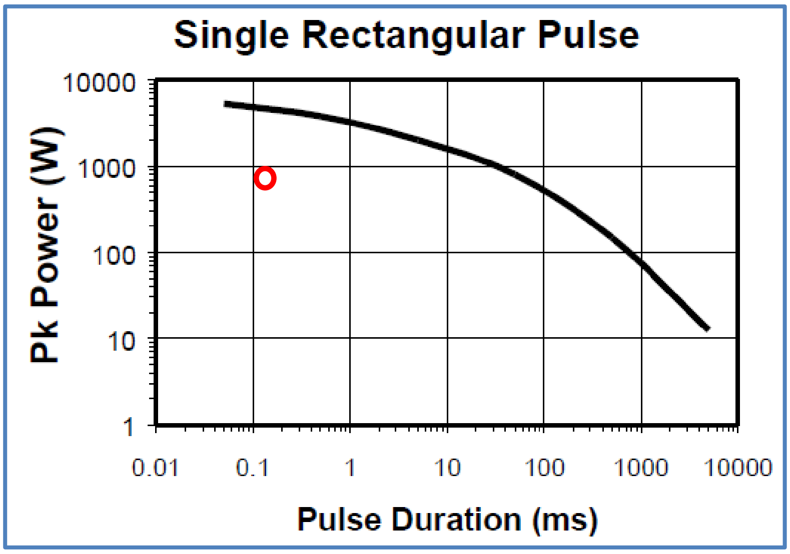
- UL1412 recognised*
- Failsafe 240V mains fusing
- Good pulse handling capability
- Small size for power rating
- UL94-V0 flameproof protection

Charging the DC link from zero to 320V each resistor will see the following peak power:

Pp = 160V2 / 33R = 780Wp (1200Wp @ 400V)

The time constant with 4 x 470uF is

Tc = 2 x 33R x 4 x 470uF = 12.5ms



There seems to be an adequate margin on the pulse handling capability. If needed, a larger resistance value will lower the peak pulse stress.

The stress if the relays are open and only the auxiliary supply is running is well below the power rating of the resistor:

Iauxi_in_max = 5W / 280Vdc = 18mA

Pv = $(18mA)^2$ x 33R = 0.11W

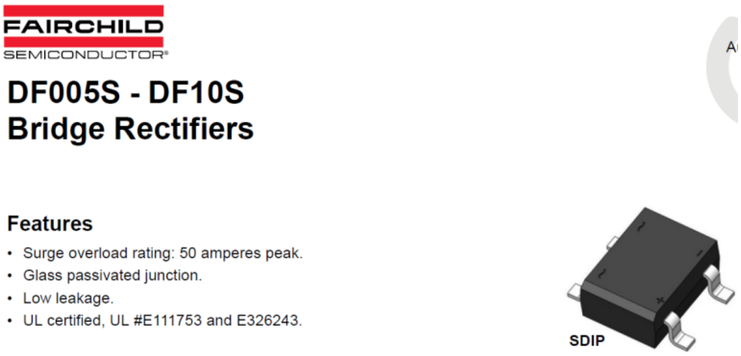
4.15.2 Rectifier inrush limiter

For reliability, a 1000V rectifier is preferred, 800V could be used also.

The peak inrush current is 400V / 66R = 6A

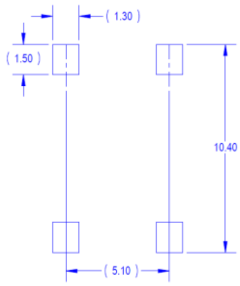
Two diodes SM4007 from Diotec would be suitable as half-wave rectifier.

Without additional cost a full-wave rectifier can be used also. The advantage is a symmetrical inrush current.


FAIRCHILD SEMICONDUCTOR

DF005S - DF10S
Bridge Rectifiers

Features
- Surge overload rating: 50 amperes peak.
- Glass passivated junction.
- Low leakage.
- UL certified, UL #E111753 and E326243.

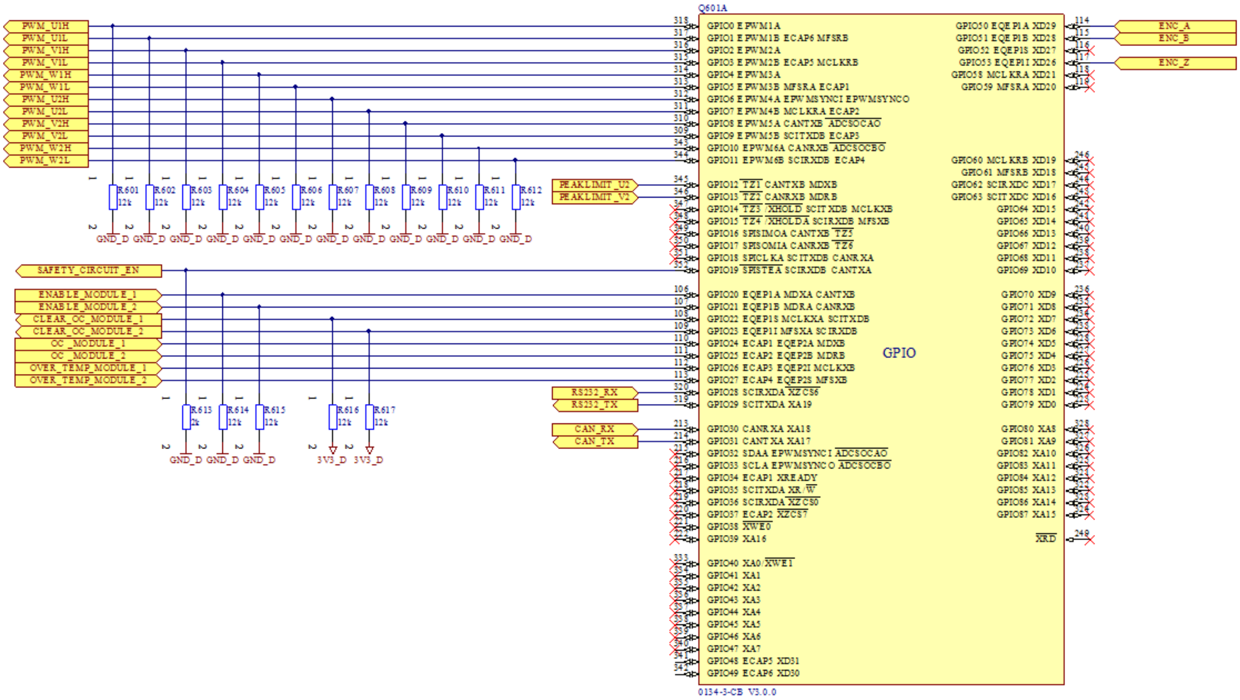


LAND PATTERN RECOMMENDATION

With this size rectifier, 3.2mm creepage distance can be implemented

4.16 Controllerboard

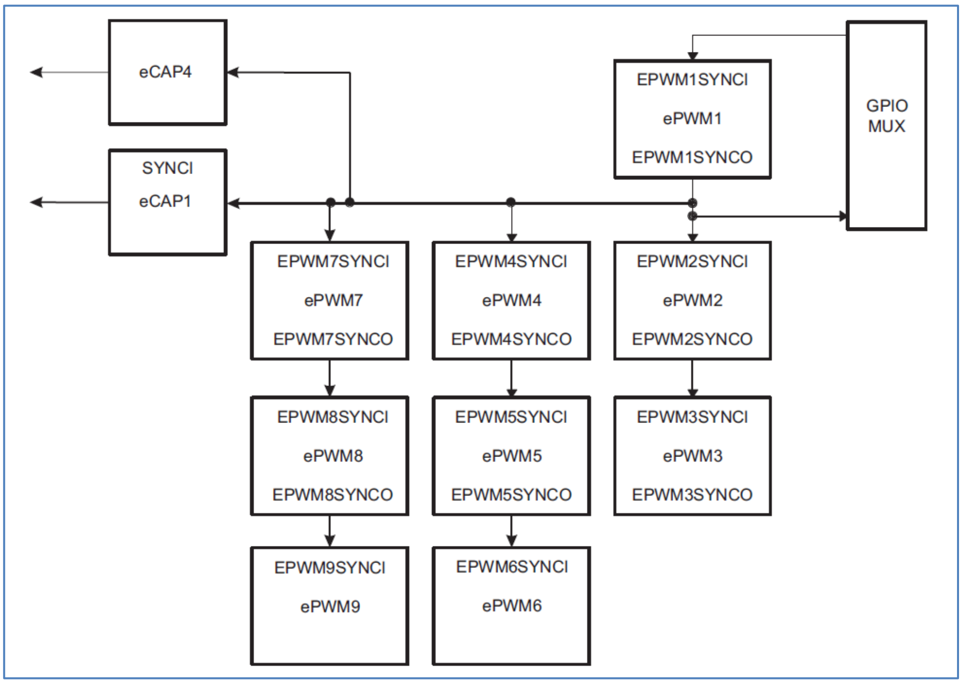
GPIO's



 drivetek ag, keltenstrasse 1, ch-2563 ipsach, phone +41 32 332 79 32, fax +41 32 332 79 31, www.drivetek.ch

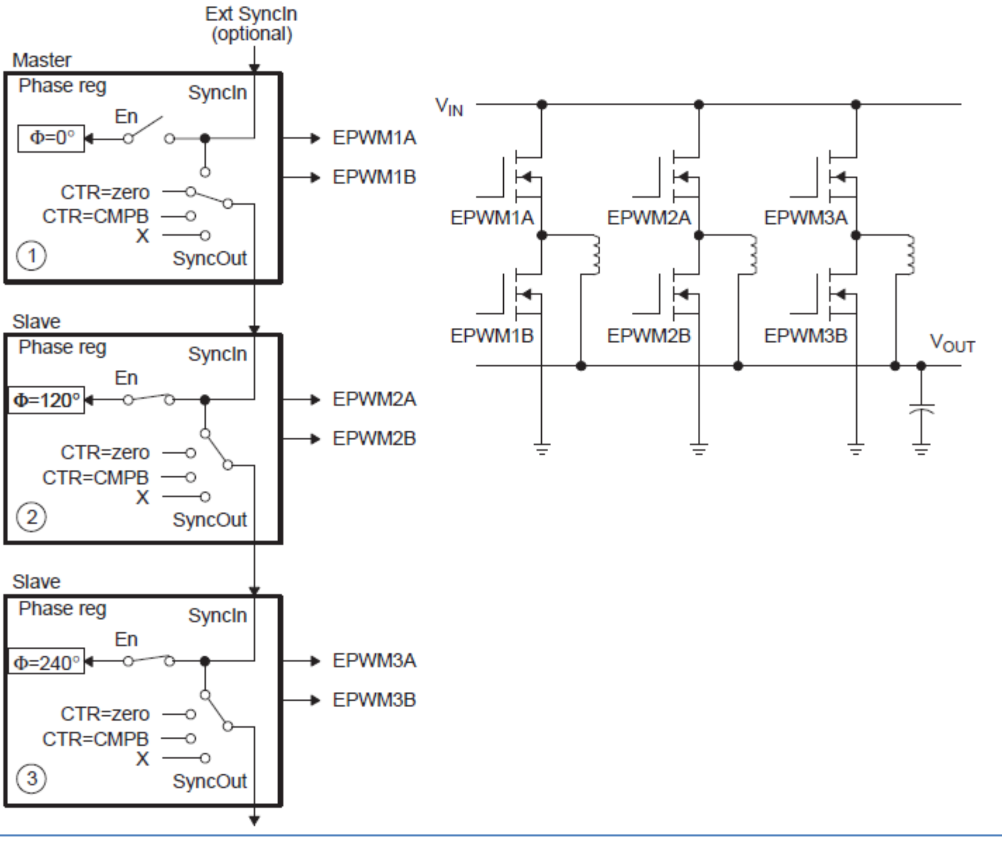
5 Software design

The ePWM module of the DSP TMS320F333 is used to generate all the phase shifted PWM signals for the DC/DC and the DC/AC converter, see Reference guide for design [6].



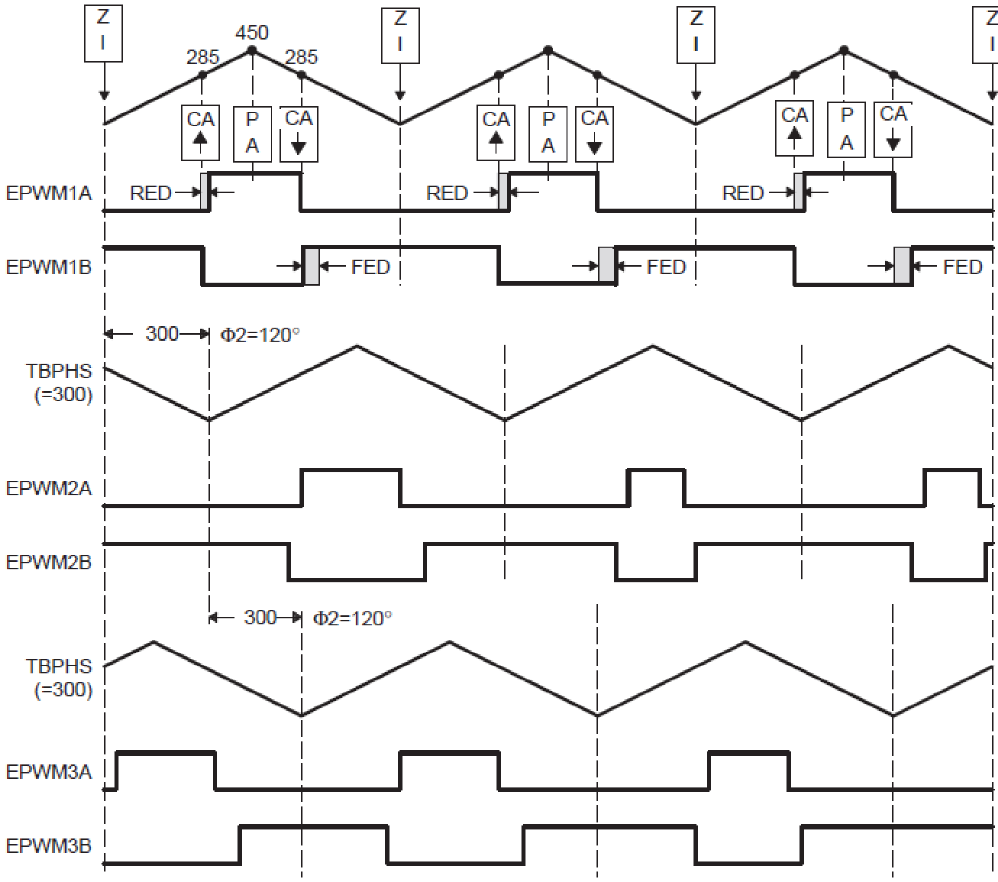
The phase shifting between the half bridges of the power cells is realized similar than example in Fig 59 and 60 of the reference guide [6]:

Figure 59. Control of a 3-Phase Interleaved DC/DC Converter



www.ti.com Applications to Power Topologies

Figure 60. 3-Phase Interleaved DC/DC Converter Waveforms for Figure 59



According to the example description of the 3-phase interleaved DC/DC converter a fast sampling of all ADC channels is possible with phase-shifted center-aligned PWM signals. All channels are oversampled as a result, which is an advantage for the filtered values of the currents.

The ePWM modules are interfaced to the power cell:

- ePWM1 LU / NU Half bridges U on power modules L and N phase 0°
- ePWM2 LV / NV Half bridges V on power modules L and N phase 120°
- ePWM3 LW / NW Half bridges W on power modules L and N phase 240°
- ePWM4 DU Half bridge U on power module DC phase 120°
- ePWM5 DV Half bridge V on power module DC phase 240°
- ePWM6 DW Half bridge W on power module DC phase 360° = 0°

5.1 DSP Interface Overview

Short overview (does not include all I/O‘s)

Signal	DSC Interface	Anzahl Pins	Kommentar
PWM für Gate Drive Phase LU / NU	ePWM1	2	
PWM für Gate Drive Phase LV / NV	ePWM2	2	
PWM für Gate Drive Phase LW / NW	ePWM3	2	
PWM für Gate Drive Phase DU	ePWM4	2	
PWM für Gate Drive Phase DV	ePWM5	2	
PWM für Gate Drive Phase DW	ePWM6	2	

Serial Interface (USB)	SCI A	1	
EEPROM	SPI A	1x4	
Encoder	eQEP 1	1x3	
Main CAN	eCAN A	1x2	

5.2 Pin and Port Mapping Prozessor

5.2.1 Analog Inputs

		PIN NO.				
NAME	**PGF**	**ZHH**	**ZJZ**	**Description**	**Signal Name drivetek**	**Pin Nr. Board**
	PIN #	**BALL #**	**BALL #**			
ADCINA7	35	K4	K1	ADC Group A, Channel 7 input (I)	ADREF	442
ADCINA6	36	J5	K2	ADC Group A, Channel 6 input (I)	Temperature max	443
ADCINA5	37	L1	L1	ADC Group A, Channel 5 input (I)	Phase Voltage V1	444
ADCINA4	38	L2	L2	ADC Group A, Channel 4 input (I)	Phase Voltage U1	445
ADCINA3	39	L3	L3	ADC Group A, Channel 3 input (I)	Current Signal Phase V1	446
ADCINA2	40	M1	M1	ADC Group A, Channel 2 input (I)	Reference Signal Phase V1	447
ADCINA1	41	N1	M2	ADC Group A, Channel 1 input (I)	Current Signal Phase U1	448
ADCINA0	42	M3	M3	ADC Group A, Channel 0 input (I)	Reference Signal Phase U1	449
ADCINB7	53	K5	N6	ADC Group B, Channel 7 input (I)	Relais Voltage	460
ADCINB6	52	P4	M6	ADC Group B, Channel 6 input (I)	Grid Voltage	459
ADCINB5	51	N4	N5	ADC Group B, Channel 5 input (I)	DC Link Voltage	458
ADCINB4	50	M4	M5	ADC Group B, Channel 4 input (I)	Current Signal Phase W2	457
ADCINB3	49	L4	N4	ADC Group B, Channel 3 input (I)	Reference Signal Phase W2	456
ADCINB2	48	P3	M4	ADC Group B, Channel 2 input (I)	Current Signal Phase V2	455
ADCINB1	47	N3	N3	ADC Group B, Channel 1 input (I)	Reference Signal Phase V1	454
ADCINB0	46	P2	P3	ADC Group B, Channel 0 input (I)	Current Signal Phase U2	453

5.2.2 Digital Inputs and Outputs

		PIN NO.				
NAME	**PGF**	**ZHH**	**ZJZ**	**Description**	**Signal Name drivetek**	**Pin Nr. Board**
	PIN #	**BALL #**	**BALL #**			
GPIO0 **EPWM1A**	5	C1	D1	General purpose input/output 0 (I/O/Z) Enhanced PWM1 Output A and HRPWM channel (O)	PWM_U1H	141
GPIO1 **EPWM1B** ECAP6 MFSRB	6	D3	D2	General purpose input/output 1 (I/O/Z) Enhanced PWM1 Output B (O) Enhanced Capture 6 input/output (I/O) McBSP-B receive frame synch (I/O)	PWM_U1L	142
GPIO2 **EPWM2A**	7	D2	D3	General purpose input/output 2 (I/O/Z) Enhanced PWM2 Output A and HRPWM channel (O)	PWM_V1H	143
GPIO3 **EPWM2B** ECAP5 MCLKRB	10	E4	E1	General purpose input/output 3 (I/O/Z) Enhanced PWM2 Output B (O) Enhanced Capture 5 input/output (I/O) McBSP-B receive clock (I/O)	PWM_V1L	144
GPIO4 **EPWM3A**	11	E2	E2	General purpose input/output 4 (I/O/Z) Enhanced PWM3 output A and HRPWM channel (O)	PWM_W1H	145
GPIO5 **EPWM3B** MFSRA ECAP1	12	E3	E3	General purpose input/output 5 (I/O/Z) Enhanced PWM3 output B (O) McBSP-A receive frame synch (I/O) Enhanced Capture input/output 1 (I/O)	PWM_W1L	146
GPIO6 **EPWM4A** EPWMSYNCI EPWMSYNCO	13	E1	F1	General purpose input/output 6 (I/O/Z) Enhanced PWM4 output A and HRPWM channel (O) External ePWM sync pulse input (I) External ePWM sync pulse output (O)	PWM_U2H	147
GPIO7 **EPWM4B** MCLKRA ECAP2	16	F2	F2	General purpose input/output 7 (I/O/Z) Enhanced PWM4 output B (O) McBSP-A receive clock (I/O) Enhanced capture input/output 2 (I/O)	PWM_U2L	148
GPIO8 **EPWM5A** CANTXB ADCSOCAO	17	F1	F3	General Purpose Input/Output 8 (I/O/Z) Enhanced PWM5 output A and HRPWM channel (O) Enhanced CAN-B transmit (O) ADC start-of-conversion A (O)	PWM_V2H	149

GPIO9 **EPWM5B** SCITXDB ECAP3	18	G5	G1	General purpose input/output 9 (I/O/Z) Enhanced PWM5 output B (O) SCI-B transmit data(O) Enhanced capture input/output 3 (I/O)	PWM_V2L	150
GPIO10 **EPWM6A** CANRXB ADCSOCBO	19	G4	G2	General purpose input/output 10 (I/O/Z) Enhanced PWM6 output A and HRPWM channel (O) Enhanced CAN-B receive (I) ADC start-of-conversion B (O)	PWM_W2H	151
GPIO11 **EPWM6B** SCIRXDB ECAP4	20	G2	G3	General purpose input/output 11 (I/O/Z) Enhanced PWM6 output B (O) SCI-B receive data (I) Enhanced CAP Input/Output 4 (I/O)	PWM_W2L	152
GPIO12 **TZ1** CANTXB MDXB	21	G3	H1	General purpose input/output 12 (I/O/Z) Trip Zone input 1 (I) Enhanced CAN-B transmit (O) McBSP-B transmit serial data (O)	\PEAKLIMIT_U2	153
GPIO13 **TZ2** CANRXB MDRB	24	H3	H2	General purpose input/output 13 (I/O/Z) Trip Zone input 2 (I) Enhanced CAN-B receive (I) McBSP-B receive serial data (I)	\PEAKLIMIT_V2	154
GPIO14 **TZ3** /XHOLD SCITXDB MCLKXB	25	H2	H3	General purpose input/output 14 (I/O/Z) Trip Zone input 3/External Hold Request. XHOLD , when active (low), requests the external interface (XINTF) to release the external bus and place all buses and strobes into a high-impedance state. To prevent this from happening when TZ3 signal goes active, disable this function by writing XINTCNF2[HOLD] = 1. If this is not done, the XINTF bus will go into high impedance anytime TZ3 goes low. On the ePWM side, TZn signals are ignored by default, unless they are enabled by the code. The XINTF will release the bus when any current access is complete and there are no pending accesses on the XINTF. (I) SCI-B Transmit (I) McBSP-B transmit clock (I/O)	\OC _MODULE_1	155
GPIO15 / **TZ4** XHOLDA SCIRXDB MFSXB	26	H4	J1	General purpose input/output 15 (I/O/Z) Trip Zone input 4/External Hold Acknowledge. The pin function for this option is based onthe direction chosen in the GPADIR register. If the pin is configured as an input, then TZ4 function is chosen. If the pin is configured as an output, then XHOLDA function is chosen. XHOLDA is driven active (low) when the XINTF has granted an XHOLD request. All XINTF buses and strobe signals will be in a high-impedance state. XHOLDA is released when the XHOLD signal is released. External devices should only drive the external bus when XHOLDA is active (low). (I/0) SCI-B receive (I) McBSP-B transmit frame synch (I/O)	\OC _MODULE_2	156
GPIO16 SPISIMOA CANTXB **TZ5**	27	H5	J2	General purpose input/output 16 (I/O/Z) SPI slave in, master out (I/O) Enhanced CAN-B transmit (O) Trip Zone input 5 (I)	\OVER_TEMP_MODULE_1	157
GPIO17 SPISOMIA CANRXB **TZ6**	28	J1	J3	General purpose input/output 17 (I/O/Z) SPI-A slave out, master in (I/O) Enhanced CAN-B receive (I) Trip zone input 6 (I)	\OVER_TEMP_MODULE_2	324
GPIO18 SPICLKA SCITXDB CANRXA	62	L6	N8	General purpose input/output 18 (I/O/Z) SPI-A clock input/output (I/O) SCI-B transmit (O) Enhanced CAN-A receive (I)	SAFETY_CIRCUIT_EN	323

GPIO19 SPISTEA SCIRXDB CANTXA	63	K7	M8	General purpose input/output 19 (I/O/Z) SPI-A slave transmit enable input/output (I/O) SCI-B receive (I) Enhanced CAN-A transmit (O)		322
GPIO20 EQEP1A MDXA CANTXB	64	L7	P9	General purpose input/output 20 (I/O/Z) Enhanced QEP1 input A (I) McBSP-A transmit serial data (O) Enhanced CAN-B transmit (O)	ENABLE_MODULE_1	301
GPIO21 EQEP1B MDRA CANRXB	65	P7	N9	General purpose input/output 21 (I/O/Z) Enhanced QEP1 input B (I) McBSP-A receive serial data (I) Enhanced CAN-B receive (I)	ENABLE_MODULE_2	302
GPIO22 EQEP1S MCLKXA SCITXDB	66	N7	M9	General purpose input/output 22 (I/O/Z) Enhanced QEP1 strobe (I/O) McBSP-A transmit clock (I/O) SCI-B transmit (O)	\CLEAR_OC_MODULE_1	303
GPIO23 EQEP1I MFSXA SCIRXDB	67	M7	P10	General purpose input/output 23 (I/O/Z) Enhanced QEP1 index (I/O) McBSP-A transmit frame synch (I/O) SCI-B receive (I)	\CLEAR_OC_MODULE_2	304
GPIO24 ECAP1 EQEP2A MDXB	68	M8	N10	General purpose input/output 24 (I/O/Z) Enhanced capture 1 (I/O) Enhanced QEP2 input A (I) McBSP-B transmit serial data (O)		305
GPIO25 ECAP2 EQEP2B MDRB	69	N8	M10	General purpose input/output 25 (I/O/Z) Enhanced capture 2 (I/O) Enhanced QEP2 input B (I) McBSP-B receive serial data (I)		306
GPIO26 ECAP3 EQEP2I MCLKXB	72	K8	P11	General purpose input/output 26 (I/O/Z) Enhanced capture 3 (I/O) Enhanced QEP2 index (I/O) McBSP-B transmit clock (I/O)		307
GPIO27 ECAP4 EQEP2S MFSXB	73	L9	N11	General purpose input/output 27 (I/O/Z) Enhanced capture 4 (I/O) Enhanced QEP2 strobe (I/O) McBSP-B transmit frame synch (I/O)		308
GPIO28 SCIRXDA XZCS6	141	E10	D10	General purpose input/output 28 (I/O/Z) SCI receive data (I) External Interface zone 6 chip select (O)	LED_GREN Led grün (für optische Kontrolle) (On Controller Board)	102
GPIO29 SCITXDA XA19	2	C2	C1	General purpose input/output 29. (I/O/Z) SCI transmit data (O) External Interface Address Line 19 (O)	LED_RED Led rot (für optische Kontrolle) (On Controller Board)	103
GPIO30 **CANRXA** XA18	1	B2	C2	General purpose input/output 30 (I/O/Z) Enhanced CAN-A receive (I) External Interface Address Line 18 (O)	CAN__RX	215
GPIO31 **CANTXA** XA17	176	A2	B2	General purpose input/output 31 (I/O/Z) Enhanced CAN-A transmit (O) External Interface Address Line 17 (O)	CAN__TX	216
GPIO32 SDAA EPWMSYNCI ADCSOCAO	74	N9	M11	General purpose input/output 32 (I/O/Z) I2C data open-drain bidirectional port (I/OD) Enhanced PWM external sync pulse input (I) ADC start-of-conversion A (O)		217
GPIO33 SCLA EPWMSYNCO ADCSOCBO	75	P9	P12	General-Purpose Input/Output 33 (I/O/Z) I2C clock open-drain bidirectional port (I/OD) Enhanced PWM external synch pulse output (O) ADC start-of-conversion B (O)		218
GPIO34 ECAP1 XREADY	142	D10	A9	General-Purpose Input/Output 34 (I/O/Z) Enhanced Capture input/output 1 (I/O) External Interface Ready signal		219
GPIO35 **SCITXDA** XR/W	148	A9	B9	General-Purpose Input/Output 35 (I/O/Z) SCI-A transmit data (O) External Interface read, not write strobe	RS232_TX	220
GPIO36 **SCIRXDA** XZCS0	145	C10	C9	General-Purpose Input/Output 36 (I/O/Z) SCI receive data (I) External Interface zone 0 chip select (O)	RS232_RX	221

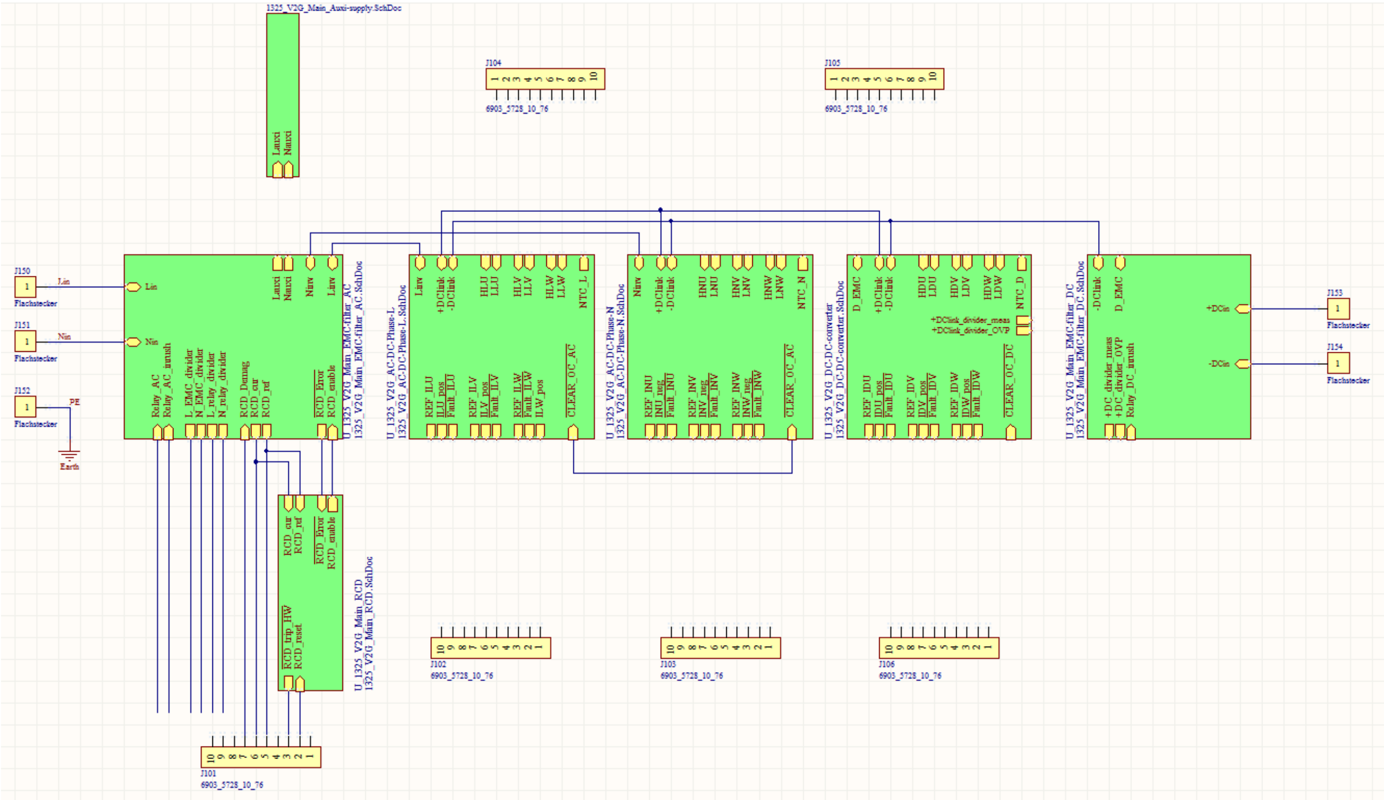
GPIO37 ECAP2 XZCS7	150	D9	B8	General-Purpose Input/Output 37 (I/O/Z) Enhanced Capture input/output 2 (I/O) External Interface zone 7 chip select (O)		222
GPIO38 XWE0	137	D11	C10	General-Purpose Input/Output 38 (I/O/Z) External Interface Write Enable 0 (O)		223
GPIO39 XA16	175	B3	C3	General-Purpose Input/Output 39 (I/O/Z) External Interface Address Line 16 (O)		224
GPIO40 XA0/XWE1	151	D8	C8	General-Purpose Input/Output 40 (I/O/Z) External Interface Address Line 0/External Interface Write Enable 1 (O)		225
GPIO41 XA1	152	A8	A7	General-Purpose Input/Output 41 (I/O/Z) External Interface Address Line 1 (O)		226
GPIO42 XA2	153	B8	B7	General-Purpose Input/Output 42 (I/O/Z) External Interface Address Line 2 (O)		227
GPIO43 XA3	156	B7	C7	General-Purpose Input/Output 43 (I/O/Z) External Interface Address Line 3 (O)		228
GPIO44 XA4	157	A7	A6	General-Purpose Input/Output 44 (I/O/Z) External Interface Address Line 4 (O)		229
GPIO45 XA5	158	D7	B6	General-Purpose Input/Output 45 (I/O/Z) External Interface Address Line 5 (O)		230
GPIO46 XA6	161	B6	C6	General-Purpose Input/Output 46 (I/O/Z) External Interface Address Line 6 (O)		231
GPIO47 XA7	162	A6	D6	General-Purpose Input/Output 47 (I/O/Z) External Interface Address Line 7 (O)		232
GPIO48 ECAP5 XD31	88	P13	L14	General-Purpose Input/Output 48 (I/O/Z) Enhanced Capture input/output 5 (I/O) External Interface Data Line 31 (I/O/Z)		233
GPIO49 ECAP6 XD30	89	N13	L13	General-Purpose Input/Output 49 (I/O/Z) Enhanced Capture input/output 6 (I/O) External Interface Data Line 30 (I/O/Z)		234
GPIO50 **EQEP1A** XD29	90	P14	L12	General-Purpose Input/Output 50 (I/O/Z) Enhanced QEP 1input A (I) External Interface Data Line 29 (I/O/Z)	ENC_A	311
GPIO51 **EQEP1B** XD28	91	M13	K14	General-Purpose Input/Output 51 (I/O/Z) Enhanced QEP 1input B (I) External Interface Data Line 28 (I/O/Z)	ENC_B	312
GPIO52 EQEP1S XD27	94	M14	K13	General-Purpose Input/Output 52 (I/O/Z) Enhanced QEP 1Strobe (I/O) External Interface Data Line 27 (I/O/Z)		313
GPIO53 **EQEP1I** XD26	95	L12	K12	General-Purpose Input/Output 53 (I/O/Z) Enhanced CAP1 Index (I/O) External Interface Data Line 26 (I/O/Z)	ENC_Z	314
GPIO54 SPISIMOA XD25	96	L13	J14	General-Purpose Input/Output 54 (I/O/Z) SPI-A slave in, master out (I/O) External Interface Data Line 25 (I/O/Z)	SPI EEPROM (On Controller Board)	
GPIO55 SPISOMIA XD24	97	L14	J13	General-Purpose Input/Output 55 (I/O/Z) SPI-A slave out, master in (I/O) External Interface Data Line 24 (I/O/Z)		
GPIO56 SPICLKA XD23	98	K11	J12	General-Purpose Input/Output 56 (I/O/Z) SPI-A clock (I/O) External Interface Data Line 23 (I/O/Z)		
GPIO57 SPISTEA XD22	99	K13	H13	General-Purpose Input/Output 57 (I/O/Z) SPI-A slave transmit enable (I/O) External Interface Data Line 22 (I/O/Z)		
GPIO58 MCLKRA XD21	100	K12	H12	General-Purpose Input/Output 58 (I/O/Z) McBSP-A receive clock (I/O) External Interface Data Line 21 (I/O/Z)	CPLD_RES_1	319
GPIO59 MFSRA XD20	110	H14	H11	General-Purpose Input/Output 59 (I/O/Z) McBSP-A receive frame synch (I/O) External Interface Data Line 20 (I/O/Z)	CPLD_RES_2	320
GPIO60 MCLKRB XD19	111	G14	G12	General-Purpose Input/Output 60 (I/O/Z) McBSP-B receive clock (I/O) External Interface Data Line 19 (I/O/Z)	CPLD_RES_4	331
GPIO61 MFSRB XD18	112	G12	F14	General-Purpose Input/Output 61 (I/O/Z) McBSP-B receive frame synch (I/O) External Interface Data Line 18 (I/O/Z)	CPLD_RES_3	332
GPIO62 SCIRXDC XD17	113	G13	F13	General-Purpose Input/Output 62 (I/O/Z) SCI-C receive data (I) External Interface Data Line 17 (I/O/Z)	RES_GD_ERROR	333
GPIO63 SCITXDC XD16	114	G11	F12	General-Purpose Input/Output 63 (I/O/Z) SCI-C transmit data (O) External Interface Data Line 16 (I/O/Z)	RES_CPLD_ERROR	334
GPIO64 - XD15	115	G10	E14	General-Purpose Input/Output 64 (I/O/Z) - External Interface Data Line 15 (I/O/Z)		335

GPIO65 - XD14	116	F14	E13	General-Purpose Input/Output 65 (I/O/Z) - External Interface Data Line 14 (I/O/Z)		336
GPIO66 - XD13	119	F11	E12	General-Purpose Input/Output 66 (I/O/Z) - External Interface Data Line 13 (I/O/Z)		337
GPIO67 - XD12	122	E13	D14	General-Purpose Input/Output 67 (I/O/Z) - External Interface Data Line 12 (I/O/Z)		338
GPIO68 - XD11	123	E11	D13	General-Purpose Input/Output 68 (I/O/Z) - External Interface Data Line 11 (I/O/Z)		339
GPIO69 - XD10	124	F10	D12	General-Purpose Input/Output 69 (I/O/Z) - External Interface Data Line 10 (I/O/Z)		340
GPIO70 - XD9	127	D12	C14	General-Purpose Input/Output 70 (I/O/Z) - External Interface Data Line 9 (I/O/Z)		201
GPIO71 - XD8	128	C14	C13	General-Purpose Input/Output 71 (I/O/Z) - External Interface Data Line 8 (I/O/Z)		202
GPIO72 - XD7	129	B14	B13	General-Purpose Input/Output 72 (I/O/Z) - External Interface Data Line 7 (I/O/Z)		203
GPIO73 - XD6	130	C12	A12	General-Purpose Input/Output 73 (I/O/Z) - External Interface Data Line 6 (I/O/Z)		204
GPIO74 - XD5	131	C13	B12	General-Purpose Input/Output 74 (I/O/Z) - External Interface Data Line 5 (I/O/Z)		205
GPIO75 - XD4	132	A14	C12	General-Purpose Input/Output 75 (I/O/Z) - External Interface Data Line 4 (I/O/Z)		206
GPIO76 - XD3	133	B13	A11	General-Purpose Input/Output 76 (I/O/Z) - External Interface Data Line 3 (I/O/Z)		207
GPIO77 - XD2	134	A13	B11	General-Purpose Input/Output 77 (I/O/Z) - External Interface Data Line 2 (I/O/Z)		208
GPIO78 - XD1	135	B12	C11	General-Purpose Input/Output 78 (I/O/Z) - External Interface Data Line 1 (I/O/Z)		209
GPIO79 - XD0	136	A12	B10	General-Purpose Input/Output 79 (I/O/Z) - External Interface Data Line 0 (I/O/Z)		210
GPIO80 - XA8	163	C6	A5	General-Purpose Input/Output 80 (I/O/Z) - External Interface Address Line 8 (O)		211
GPIO81 - XA9	164	E6	B5	General-Purpose Input/Output 81 (I/O/Z) - External Interface Address Line 9 (O)		212
GPIO82 - XA10	165	C5	C5	General-Purpose Input/Output 82 (I/O/Z) - External Interface Address Line 10 (O)		213
GPIO83 - XA11	168	D5	A4	General-Purpose Input/Output 83 (I/O/Z) - External Interface Address Line 11 (O)		214
GPIO84 - XA12	169	E5	B4	General-Purpose Input/Output 84 (I/O/Z) - External Interface Address Line 12 (O)	Bootmode Select 0 (On Controller Board)	158
GPIO85 - XA13	172	C4	C4	General-Purpose Input/Output 85 (I/O/Z) - External Interface Address Line 13 (O)	Bootmode Select 1 (On Controller Board)	159
GPIO86 - XA14	173	D4	A3	General-Purpose Input/Output 86 (I/O/Z) - External Interface Address Line 14 (O)	Bootmode Select 2 (On Controller Board)	160
GPIO87 - XA15	174	A3	B3	General-Purpose Input/Output 87 (I/O/Z) - External Interface Address Line 15 (O)	Bootmode Select 3 (On Controller Board)	101
XRD	149	B9	A8	External Interface Read Enable		260

6 Schematics

6.1 Mainboard

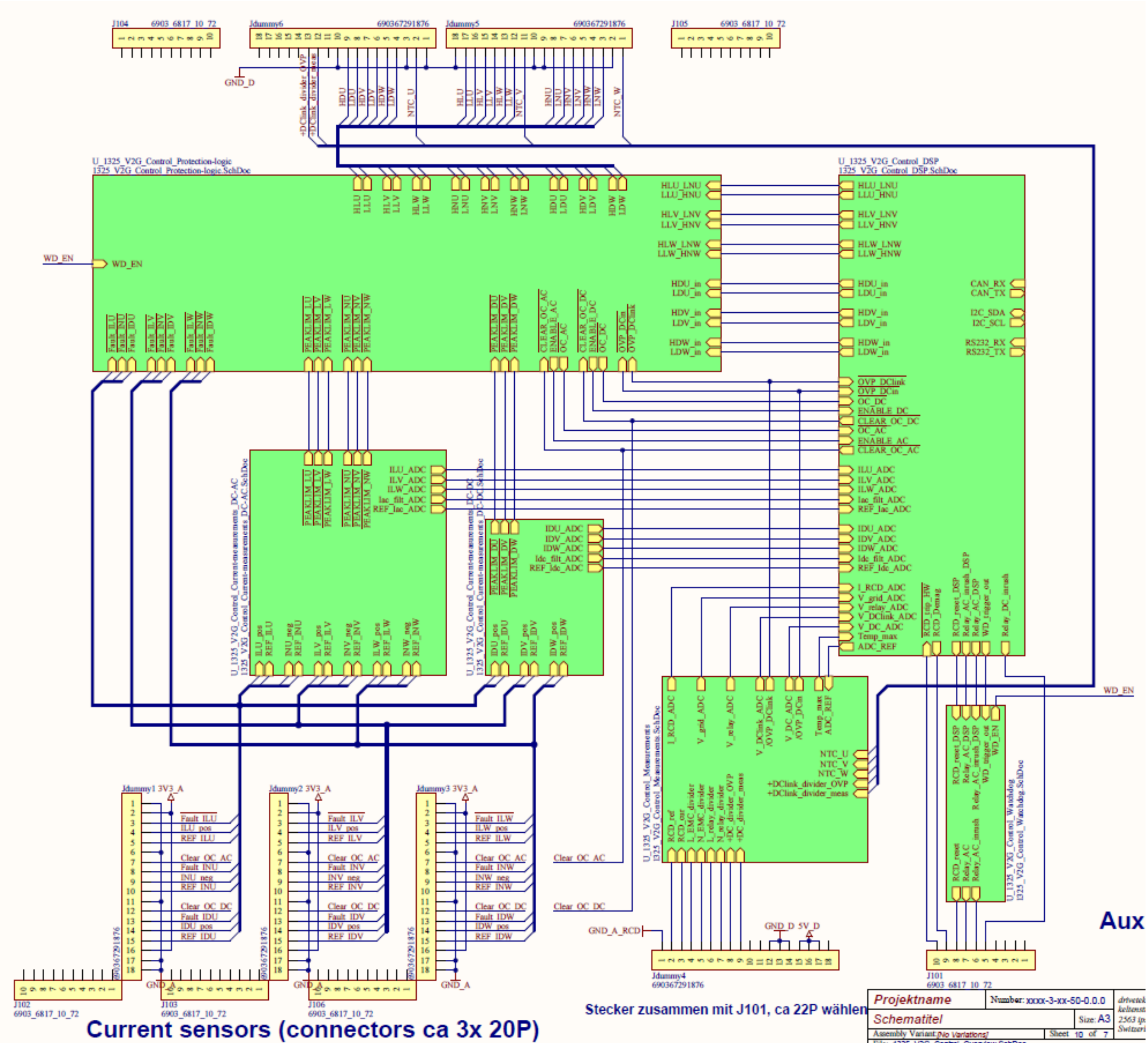
Overview schematics:



complete schematics see [4]

6.2 Controlboard

Overview schematics:



Complete schematics see [5].

7 Printet circuit boards (PCBs)

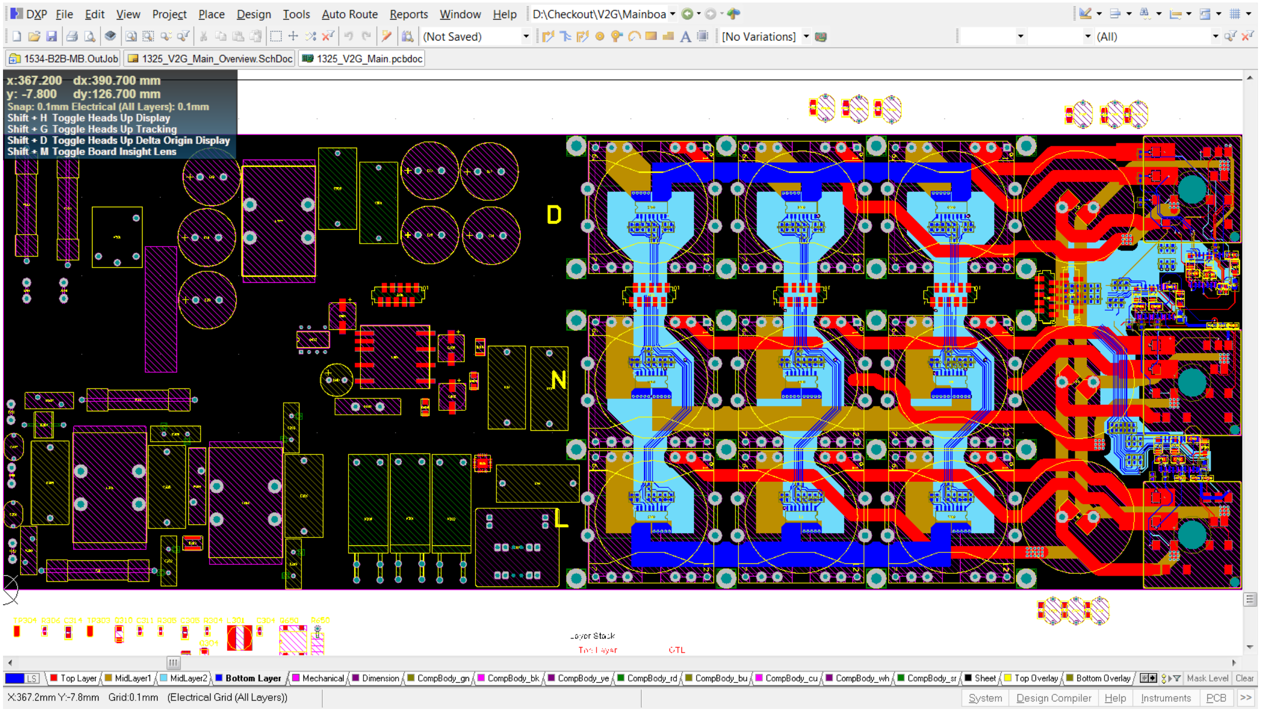
7.1 Mainboard

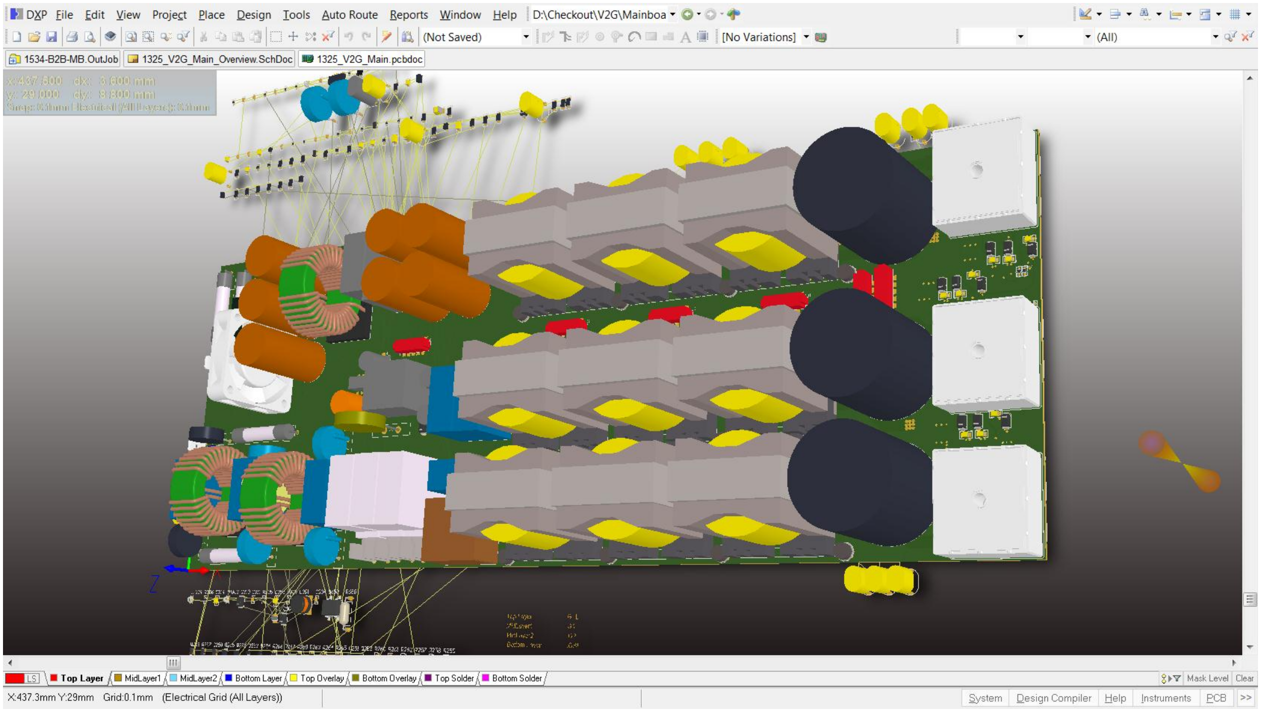
A 4-layer 70um PCB will be sufficient to implement the power board.

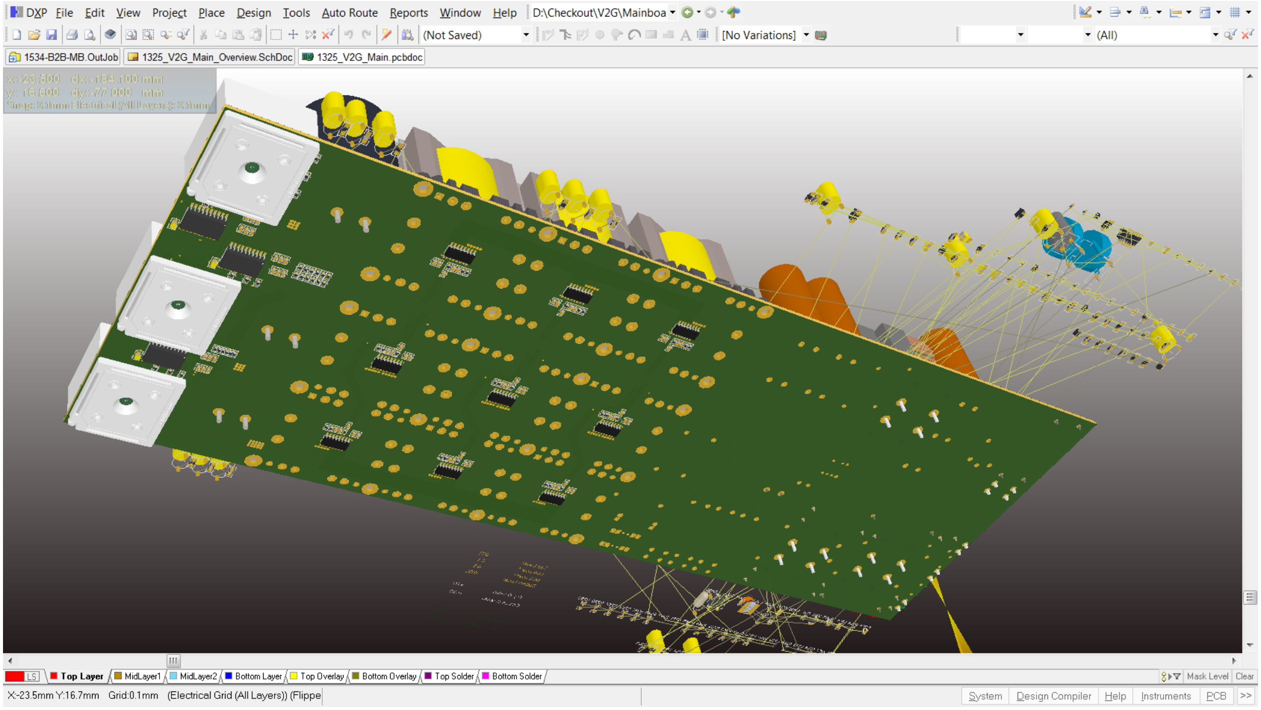
The connectors to the control PCB have a 0.65mm pitch and are suitable to mount on this copper thickness.

7.1.1 Status of the PCB layout

- Power cell around the IGBTs, smoothing chokes and current measurements is realized around 80%, the driver signals are implemented completely
- Auxiliary supply / RCD / interface – open
- EMC filters – open (placement done 90%)





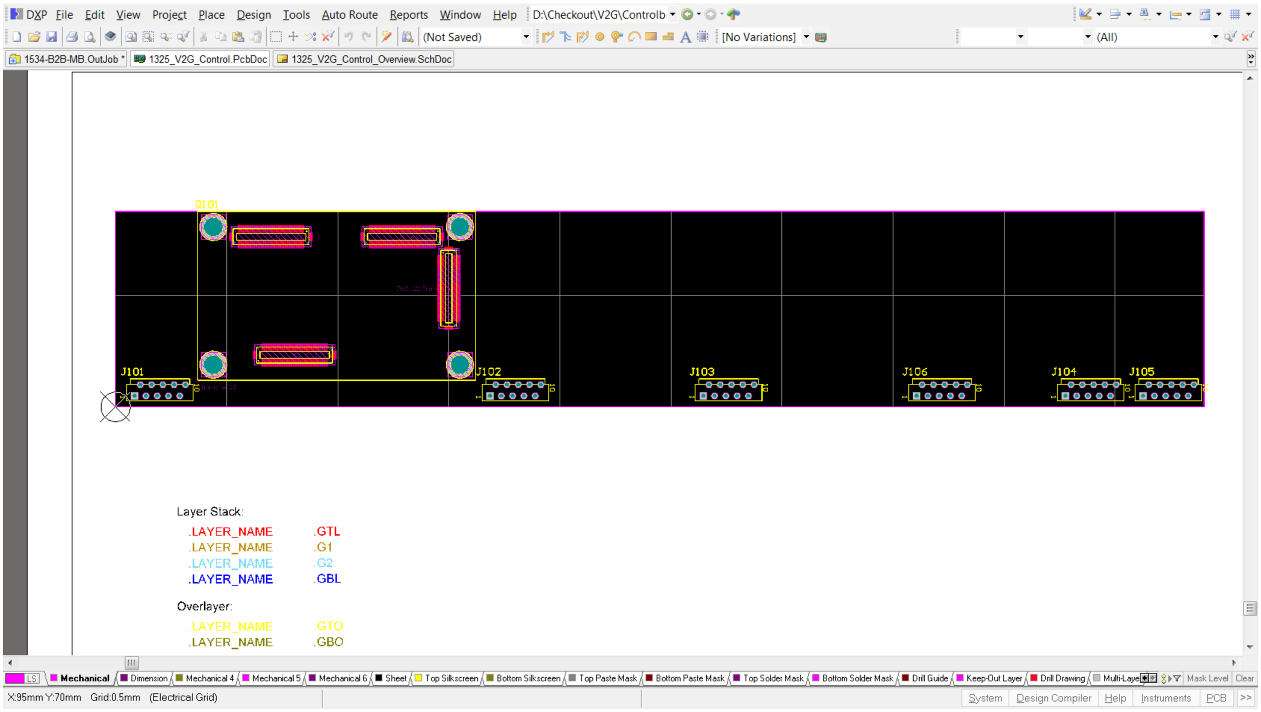


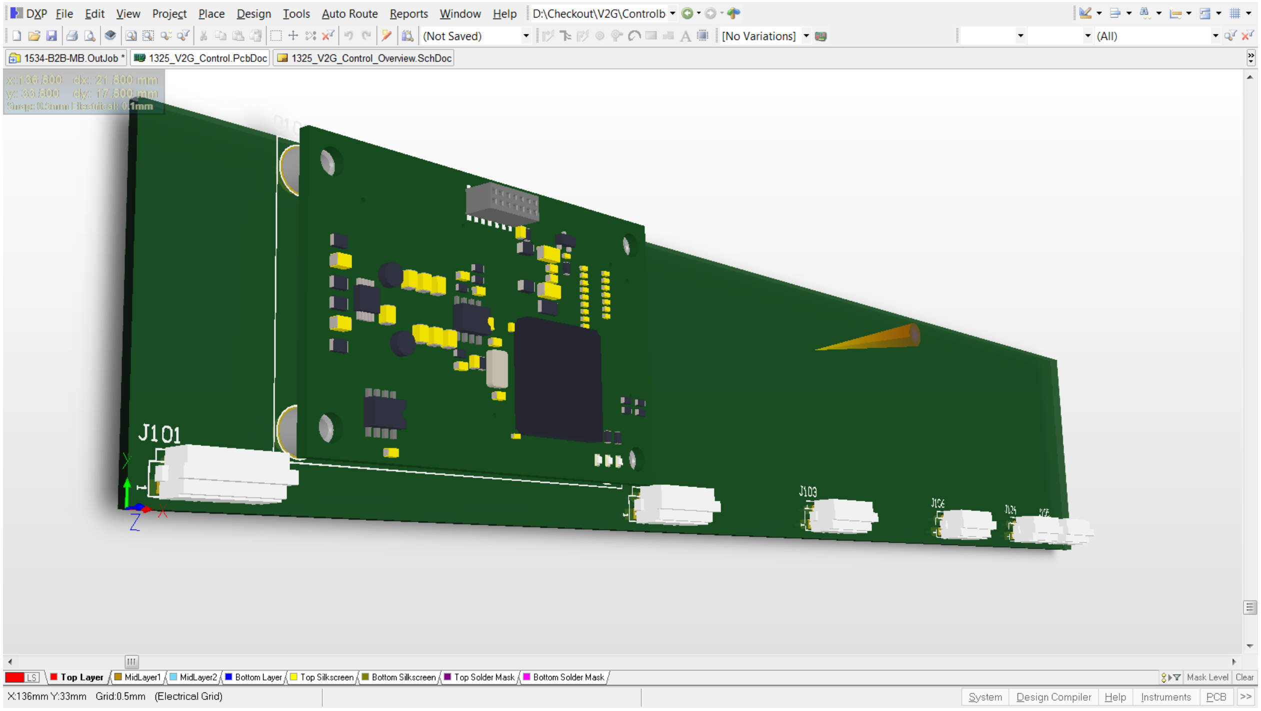
7.2 Controlboard

A 4-layer 35um PCB has been choosen.

7.2.1 Status of the PCB layout

- Shape of PCB and placement of the DSP board is done





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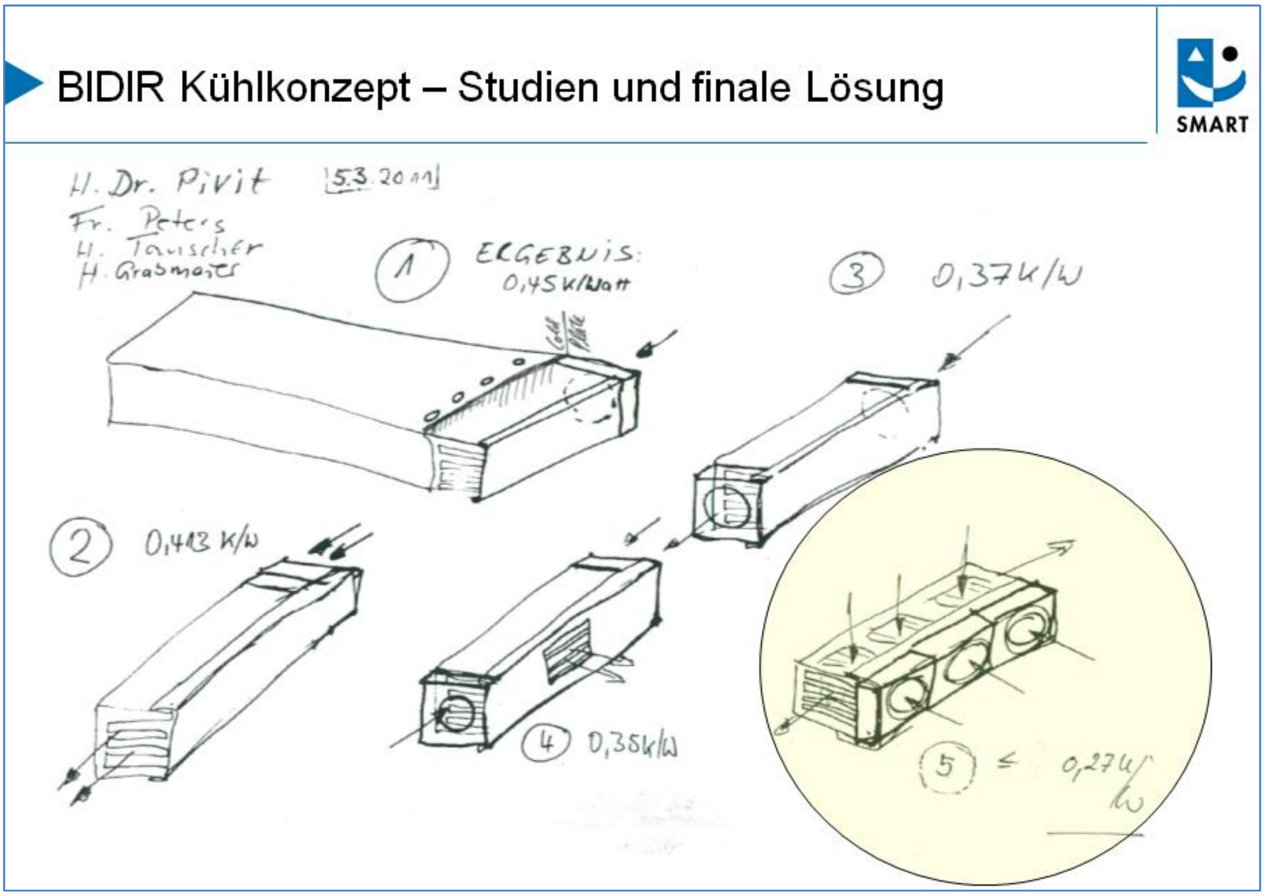
8 Mechanics

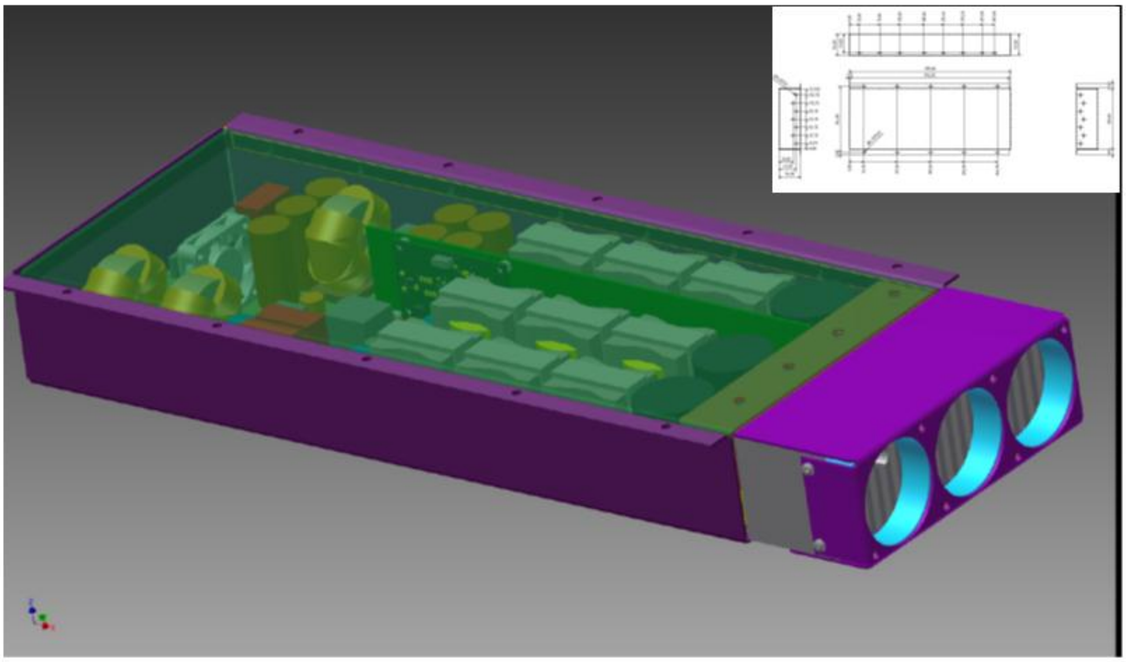
8.1 Cooling concept (by SMART GmbH)



8.2 Chassis construction (by SMART GmbH)

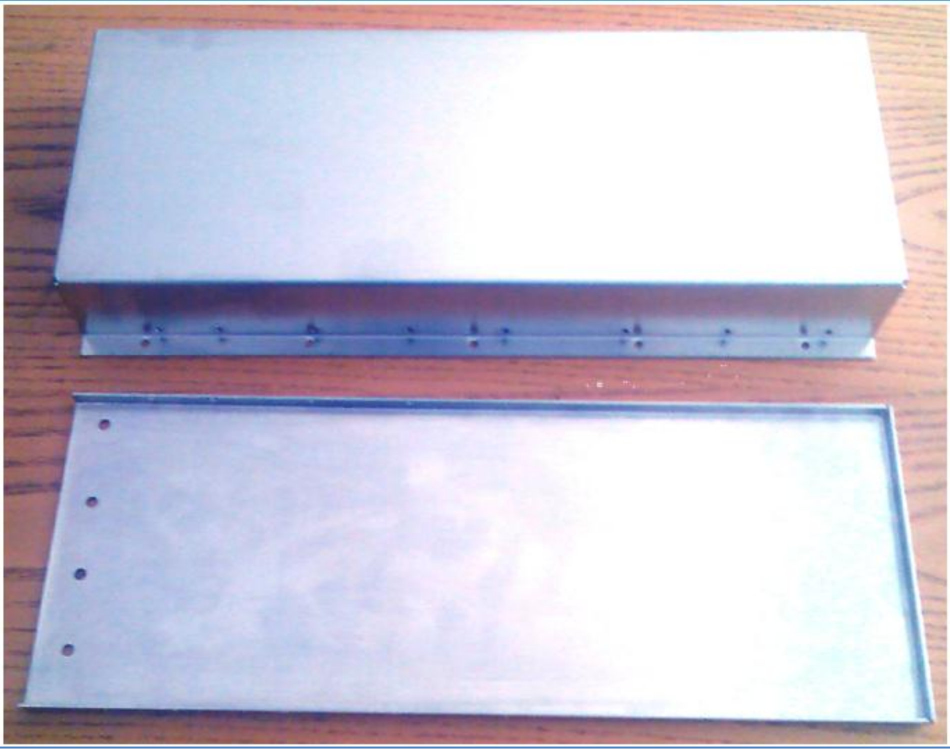
BIDIR – Gehäusekonstruktion incl. SMARTcooler

SMART



BIDIR Prototyp Gehäuse

SMART



9 Conclusion

In this first part of the project phase a technical concept to realize an A-sample of a bidirectional charger for V2G applications has been created. The implementation of the concept has been started.

In our opinion this concept would be appropriate to realize a compact and cost effective bidirectional charger for vehicule to grid applications and for the S2G project.

Unfortuantely the project could not been finished due to difficulties in the project setup and the resulting delays, see chapter 2.

The hardware design, the software design and the layout work of the printed circuit boards have been started in parallel to speed up the process. Most of the workpackages are not finished yet, the status can be seen in this document.

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