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Swiss Inno-HJT

Pilot production and demonstration of innovative high performance silicon hetero-junction PV cells, modules & systems

SWISS INNO HJT

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ABSTRACT

The Photovoltaics market has been driven in the last decade by strong increase of module production per year, with > 50 GW in 2015 and predictions for 100 GW after 2020. State-of-the-art products demonstrate efficiencies of 17–18 % and 19–20 % respectively, while increasing market share of high performance silicon technologies are expected, targeting the competitive production of > 22.5 % cells. In that respect, the Silicon Heterojunction Technology (HJT) developed and matured in Switzerland by Meyer Burger is of key relevance, owing to its high conversion efficiency achieved with limited number of production steps (a pre-requisite for keeping reduced costs). In this context, the *Swiss-Inno HJT* project focused on the demonstration at the pilot scale of cost-competitive manufacturability of high performance silicon solar cells, modules and systems, based on the key processes and technologies expertise of the Meyer Burger group and of CSEM, with the objective to transfer this high power output technology with low production costs to the photovoltaic market.

Pilot lines were installed and ramped-up for HJT cells manufacturing, with innovations conducted at material, processes and design levels. The project enabled going from 21 % cell efficiency using lab-tools to 22.2 % average efficiency achieved with Meyer Burger mass-production equipment, and with efficiencies up to 22.8 % achieved with CSEM metallization R&D pilot line. This was achieved on bifacial cells and with > 30 % cell manufacturing costs reduction (only 0.4 CHF/wafer for the last cell generation). These achievements in a mass-production relevant environment demonstrate the feasibility of manufacturing high efficiency HJT cells at extremely competitive costs. The innovative SmartWire module technology was demonstrated to enable for high performance, with 330 Wp record module. Two generations of modules were manufactured in 2016 using bifacial heterojunction cells produced in the pilot lines, showing performance in the 300 Wp range, with potential for enhancement to 310-320 Wp class based on the achieved cell efficiency and module developments. The third module generation demonstrated materials cost reduction enabling to achieve down to 40 CHF/module. The cumulated wafers, cells and modules costs using technologies demonstrated in this project result in a minimum calculated cost of 0.41 CHF/Wp for the demonstrated silicon heterojunction technology, achieving strong reduction in comparison to the initial project targets, enabling for high competitivity. Finally, two-monitoring sites were completed in the project, with the 3 generations of produced modules installed on the publicly visible site next to the port and Latenium site in Hauterive, NE. The modules were successfully installed and performance monitoring initiated. First data collected indicate performance ratio potential for the developed technology in par with the project targets of > 91 %. The data analysis typically requires averaging of 1-year data for reliable performance analysis, and will be finalized therefore for the second and third generations of modules in the course of 2017.

The project achievements provided high visibility of the outstanding results achieved in Switzerland on these technology developments. The pilot lines enabled for acceleration of the developments for competitive HJT cells manufacturing, and for demonstration to potential clients. First industrial projects for silicon heterojunction cells manufacturing could be concluded by Meyer Burger in Europe, Russia and Asia. The Meyer Burger Silicon HJT technology is today further placed on the roadmap of most of the cells manufacturers worldwide. The remaining hurdles for wider integration are today linked to the initial CAPEX expenditure to be realized. Further developments in that direction will be key to achieve full industrial success.

Project goals

The goal of the *Swiss Inno-HJT* project was to demonstrate the superior performance of photovoltaic systems based on silicon heterojunction solar cells and modules manufactured on mass-production equipment at competitive costs. This fully integrated R&D project dealt with all processing steps including the monocrystalline wafer sawing using diamond wire technology, high efficiency silicon heterojunction solar cell processing, advanced cell metallization, advanced module integration using Smart Wire Technology and finally outdoor testing and demonstration. Key to the project goals, all these steps were made on pilot lines with mass production relevant processes and tools to demonstrate the commercial viability of the demonstrated technologies. This directly supports the world-wide dissemination of the silicon heterojunction technology using Swiss made equipment and technologies.

At the project initiation, efficiency up to 21 % could be demonstrated on 6 inches-commercial wafers in the premises of Meyer Burger Research, on R&D fabrication equipment. The first key goal of the project was related to the installation of a “core process” pilot line for the manufacturing of silicon heterojunction solar cells, using mass-production PECVD and PVD equipment and to the demonstration at this pre-industrial production stage of solar cells with up to 22.5 % efficiency. The second key objective of the project was linked to the development and demonstration of alternative metallization and interconnection technologies enabling to drastically reduce the costs related to the cell metallization, while guaranteeing the achievement of > 22.5 % conversion efficiency. More particularly, the development of plating technology for bifacial cells, manufactured in a R&D pilot line, was targeted at CSEM in that respect. The third key objective was then set to manufacture different cells and modules generations (from Gen1 to Gen3), and enabling to achieve up to 21 % module efficiency, keeping production costs below 0.65 CHF/W_p. The fourth key goal was finally the installation and monitoring for each module generation of 3 kW_p capacity, to demonstrate > 91 % performance ratio with the developed technologies. Overall the Swiss Inno HJT therefore targeted the acceleration of the pilot development of the silicon heterojunction cells and modules technologies, with focus on pre-industrial manufacturing, cell efficiency increase, cost reduction achievement, and on module monitoring for the demonstration of the high performance of the developed technologies.

Summary

During the *Swiss Inno-HJT* project, a fully integrated research and development structure has been set-up at CSEM and Meyer Burger. This pilot production has been used to demonstrate the economical relevance of silicon heterojunction solar cells and modules manufactured with Swiss technologies. Along the project duration, developments have led to 3 different generations of HJT solar cell and modules starting from the traditional monofacial structure, up to a high performance bifacial structure. The solar cell efficiency has been increased from 21.5% at the start-up of the pilot line up to 22.8% at the end of the project and thus with a switch from monofacial to bifacial design. This achievement was accompanied with a cell manufacturing cost reduction of more than 30 %.

A total of 39 modules have been manufactured during the project and have been installed for outdoor monitoring. The manufacturing cost of these modules has been reduced drastically by the use of new materials and innovative technologies. The first module generation made in 2015 were manufactured at an estimated cost of 0.64 CHF/Wp, reaching already the project target. In 2016, it has been demonstrated that the manufacturing cost per module can be decreased by about 40% while keeping the high power output of 300 W per module, hence reaching 0.4 CHF/W_p. This achievement done in a mass production relevant environment demonstrates the feasibility of silicon heterojunction manufacturing at extremely competitive costs. Moreover, we can forecast a further drop in cost down

to 0.3 CHF/Wp by 2020 by the introduction of thin wafers and cheaper manufacturing technologies and processes.

Work undertaken and findings obtained

2016 focus was on the production of cells and modules with technologies and processes developed during 2015 on the HJT cell and module pilot lines.
In the first section of this chapter, the Gen 2 cells and modules produced in spring 2016 and the Gen 3 cells and modules produced in fall 2016 are presented. Detailed manufacturing cost analysis is as well presented.
In a second section, more details about the development of the technologies and processes incorporated in Gen 2 and Gen 3 cells and modules are given.

1. Cell and module production

During the *Swiss Inno-HJT* project, 3 generations of cells and modules were planned. Originally only the 3rd generation of cells and modules were planned to be bifacial, but an increased market interest in bifacial systems for utility scale installation pushed us to accelerate our development in this direction. The table below presents the product features from Gen 1 to Gen 3.

	Gen 1	Gen 2	Gen 3
Wafer thickness	180 µm (as cut)	150 µm (as cut)	180 µm (as cut)
Cell	HJT monofacial	HJT bifacial	*New* HJT bifacial
module	Monofacial, Indium wire	Bifacial, indium wires	Bifacial bismuth wires

The monofacial Gen 1 cells produced in 2015 right after the ramp-up of the cell R&D line in Hauterive were reaching 21.5%^{GT} [1] conversion efficiency. The resulting Gen 1 monofacial modules were hitting 280 W at a total manufacturing cost calculated at 0.65 CHF/W_p, right on the project target. However, since the market is much more dynamic than expected, we had to revise the product design and cost targets in order to keep ahead. This Gen 1 is our starting point to develop the Gen 2 and 3 generations to boost module power at reduced manufacturing cost. The product features and results obtained are described in more details in the followings sections.

1.1 Cell production

1.1.1 Gen 2 silicon heterojunction cell production

Gen 2 cells were planned to be monofacial, but increased market interest into bifacial devices pushed us to modify the original plan. Therefore, instead of waiting until Gen 3 cells and modules to introduce bifacial structure, it has been decided to accelerate the development and work on the back side of Gen 1 HJT solar cells to make them bifacial by the substitution of the full metal blanket by a screen

[1] %^{GT} denotes the cell conversion efficiency when measured with the PASAN Grid^{TOUCH} contacting unit. This measure is mandatory when using busbar less cells and do not take into account the shading of light induced by the contacting wires. This measuring method has been introduced in the *Swiss Inno-HJT* 2014 annual report.

printed metal grid as shown in the process flow in Figure 1.1. As shown in Figure 1.2, the resulting cell structure is symmetric with ITO and screen printed metal grid on both sides of the solar cell.
Because of this modification of cell structure from monofacial to bifacial, the efficiency target for Gen 2 cells, i.e. 22.5%^{GT}, is not relevant anymore. Therefore, the target of Gen 3 bifacial cells, i.e. 21.5%^{GT}, has to be used as the new target for Gen 2 cells as well.

Figure 1.1: process flow of Si-HJT Gen 2 cells

The produced cells have the following specifications:

- *n* type CZ wafers 156x156 mm, 200 mm diameter (239 cm^2)
- cut by diamond wire ~**150 μm thick**
- rear side emitter (*p* layer on back side)
- **bifacial design** with ITO on both sides.
- busbar less screen printed **front and back grid.**
- measured with Grid^{TOUCH} contacting unit with a black non-reflective background.

The most important features of these cells compared to the Gen 1 cells are:

1. The wafer thickness has been reduced considerably from as cut thickness of 180 μm to 150 μm to reduce wafer costs and evaluate the impact of thinner wafer on bifacial device performance. This has been made possible thanks to work conducted in 2015 on the sawing development that has been described in the 2015 report of the *Swiss Inno-HJT* project.
2. The rear side Ag/NiV full area metallization deposited by PVD of the Gen 1 cells has been replaced by a screen printed silver grid. The rear side grid design used for the production has been selected out of the development work carried out by CSEM (see section on conducted developments). In addition, the rear side ITO layer has been adapted to optimize cost without major impact on performance. This optimization has been performed on the R&D pilot sputtering tool at Meyer Burger Research.

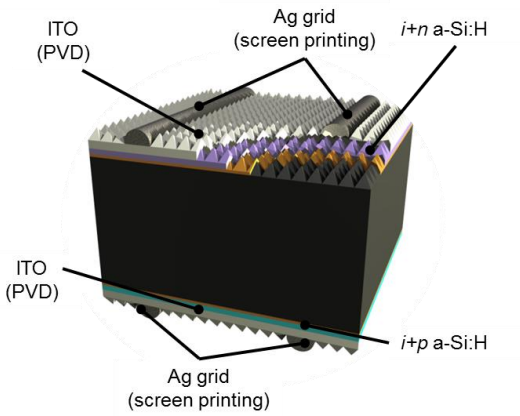


Figure 1.2: HJT solar cell structure used for Gen 2 cells.

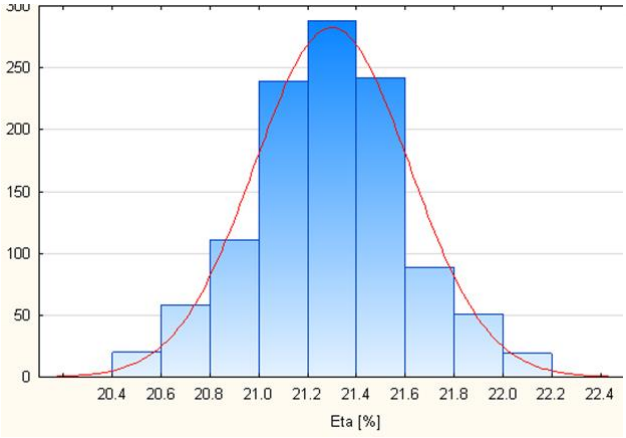


Figure 1.3: efficiency distribution of >1'100 Gen2 cells as measured with the Grid^{TOUCH} contacting unit..

Figure 1.3 shows the efficiency distribution of the 1'117 Gen 2 bifacial cells produced in spring 2016. It exhibits a nice Gaussian distribution with a median efficiency of 21.3 %^{GT} and best cell at 22.1 %^{GT}. Cell parameters are summarized in Table 1.1 together with Gen 1 median values for comparison. Gen2 revised target efficiency of 21.5%^{GT} has not been reached for this first generation of bifacial devices. However, best measured efficiency are far above the target showing the potential of this structure. Analyzing the Table 1.1 more in details, we can conclude that the achieved mean efficiency suffers from passivation issues. Indeed, the V_{oc} even if at the same level as Gen 1 cells was expected to be higher because of the thinner wafer used for Gen 2 cells. Moreover, the FF is as well showing some weaknesses compared to Gen 1, suggesting as well some passivation limitation. However, high values for both V_{oc} (739 mV) and FF (80.3%) have been reached on the champion Gen 2 cell showing that there is no physical limitation behind the limited median values. This will be the focus for the Gen 3 cells presented later in this report.
On the other hand, the short circuit current values are very close between Gen 1 (37.6 mA/cm^2) and Gen 2 (37.4 mA/cm^2) cells. This is a very impressive achievement given the fact that the Gen 2 cells have two major drawbacks compared to Gen 1 in terms of photocurrent generation: they are bifacial and made with thinner wafers. Therefore, they are more transparent to infrared light than Gen 1 cells. This achievement has been made possible by the development done on the back side ITO properties but also thanks to the reduction in plasmonic absorption at the ITO/Ag interface of Gen 1 cells. Indeed, Gen1 cells have been optimized in terms of \$/W_p and the back side reflector performance was not the best in class.

Table 1.1: Gen2 cell median and best IV parameters, measured using the PASAN Grid^{TOUCH} technology.

	eff (%^{GT})	Voc (mV)	FF (%)	Jsc (mA/cm^2)
best	22.14	739	80.27	37.34
median	21.29	728	78.1	37.41
Gen 1 median	21.5	725	78.9	37.6

Despite the lower efficiency of Gen 2 cells than the 21.5%^{GT} target, we have seen that the bifaciality of a device does not mean that high efficiency cannot be reached. Of course, the best bifacial device will always suffer from lower photo-generated current than well optimized monofacial device, but it has

been shown that there is no physical limitations prohibiting bifacial devices with efficiencies above 22.5%^{GT}, if not even higher.

1.1.2 Gen 3 silicon heterojunction cell production

Gen 3 cells have been produced during the second half of 2016 and consist, as for Gen 2 cells, in bifacial devices. Cells have been produced in 3 groups introducing in each group a new technology or process evolution, if not revolution. Focus for Gen 3 cells, as well as module as it will be shown later, has been made on cost reduction. Indeed, the market prices of PV cells and modules have dropped significantly during 2016 and the *Swiss Inno-HJ*T cost target of 0.65 CHF/Wp is today not sufficient to have a competitive technology with todays' market prices of about 0.4 CHF/Wp.

All groups have been manufactured with similar base specifications:

- *n* type CZ wafers 156x156 mm, 200 mm diameter (239 cm^2)
- cut by diamond wire **~180 µm thick**
- rear side emitter (*p* layer on back side)
- **bifacial** design
- busbar less design.
- measured with Grid^{TOUCH} contacting unit with a black non-reflective background.

Compared to Gen 2 cells, only the wafer thickness has been changed to favor high efficiency bifacial devices. The 3 groups are described briefly in the Table 1.2. Each of them addresses a specific cost driver:

- Group 1 introduces a new front side transparent conductive oxide and antireflective concept with a new material bill for lower light parasitic losses and costs. All other processes are identical to Gen 2 cells. This new structure is named Si-HJT 2.0.
- Group 2 introduces new PECVD processes that reduce significantly the amorphous silicon deposition costs. This is done in combination with the Si-HJT 2.0 cell structure.
- Group 3 uses copper plated metallization grids at the front and back side of the solar cells. Plating is achieved in the plating pilot line at CSEM as described in the development section of this report. This group combines plating and low cost PECVD processes, but not the Si-HJT 2.0 cell structure.

Table 1.2: the 3 different groups of Gen 3 cells.

	Group 1 (873 cells)	Group 2 (187 cells)	Group 3 (130 cells)
Front side TCO	New low cost materials and structure	New low cost materials and structure	Standard
PECVD	standard	New low cost processes	New low cost processes
Metallization	Ag screen printing	Ag screen printing	Cu plating

Group 1: Si-HJT 2.0 cell structure

The first group of the Gen 3 cells tackles the high front side ITO cost and photon losses. Indeed, the front side ITO is one of the drawback of Si-HJT cells because of its cost since it is made from Indium and as well because of light absorption losses because of its high carrier density. Several approaches have been proposed in the recent years but all of these new technologies improve one or the other of these drawbacks but in general never both at the same time. We can even say that when one is improved the other one is degraded. This can be described into 2 examples:

- Front side ITO can be replaced by Indium oxide doped with various element such as hydrogen, tungsten oxide or cerium oxide. By doing so, the carrier density can be significantly reduced increasing then the photo-generated current. The electrical properties of the TCO is kept constant by an improvement of the carrier mobility usually observed in such king of TCOs. However, TCOs still contains Indium and therefor are not cheaper. Moreover, these materials are very brittle compared to ITO and more complicated to manufacture. Therefore manufacturing costs increase and the deposition technique have to be adapted to the new materials generating additional costs since these techniques are generally more complicated than magnetron sputtering.
- Another option is to substitute ITO by low cost TCOs, such as Zinc Oxide doped with element such as aluminium. Definitively the cost can be reduced considerably by this way since Zinc oxide sputtering targets are about 3 times less expensive than ITO targets and both materials can be deposited by the same low cost sputtering equipment. However, Zinc oxide based TCO have not the same electrical and optical performance than ITO and the cell efficiency drops at least by 0.5% absolute.

The Si-HJT 2.0 cell structure (Figure 1.4) solves both of these drawbacks of ITO at the same time by only separating the TCO processes for front and back side with the only disadvantage to add one processing step as sketched in Figure 1.5. Since the IP protection of this new process and cell structure is still ongoing, no further details about this technology can be shared in the present report.

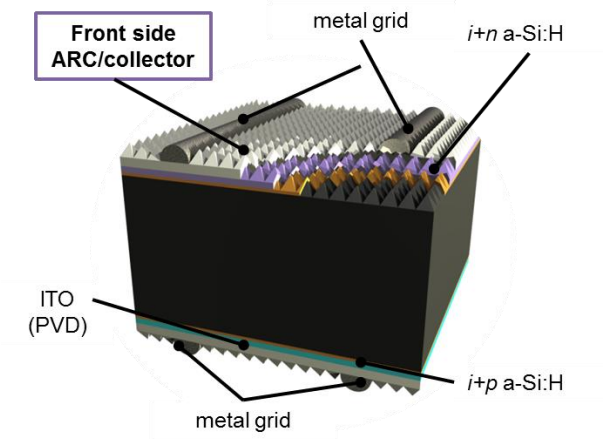


Figure 1.4: Si-HJT 2.0 solar cell structure used for Gen 3.1 cells.

However, what can be disclosed is the effect of such structure on the cell performance as well as the cost reduction. As shown in Figure 1.6, the efficiency of such device surpasses the classical Si-HJT structure and thus mostly by an increase in short circuit current. Indeed, in this example the short circuit current density increases by more than 1 mA/cm^2. Not all of this increase can be attributed to the Si-HJT 2.0 structure, but based on other experimental results we can state that 0.4 to 0.5 mA/cm^2 can be attributed to the change of material bill at the front side. The remaining gain comes from the increased wafer thickness as well as to optimized metallization to reach a trade-off between J_{sc} and FF.

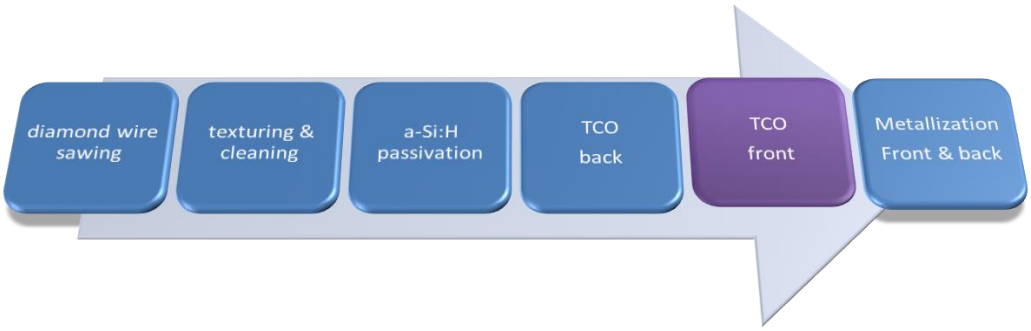
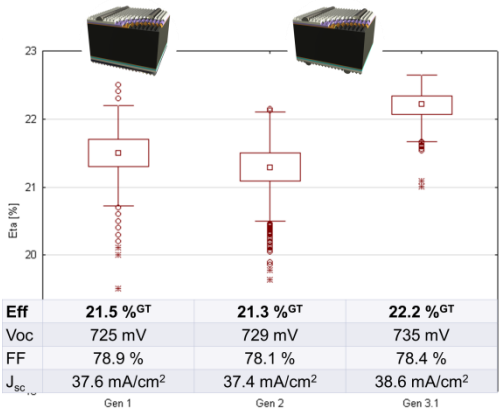


Figure 1.5: process flow of Si-HJT 2.0 Gen 3 cells

Concerning the passivation quality, we can see that the V_{oc} is increased when compared to Gen 1 and Gen 2 cells despite the thicker wafers used in the case of Gen 3 cells. This demonstrates that the passivation quality issues pointed for Gen 2 (and Gen 1) cells have been solved, at least partially. This is confirmed by the lower spread in data as shown in Figure 1.7 where the distribution is no longer a Gaussian. Moreover, the difference between best device and median cell parameters is significantly reduced as shown in Table 1.3 compared to Gen 2 cells, demonstrating once more the improved quality and uniformity of the cell process in the pilot line.



Eff	21.5 %^{GT}	21.3 %^{GT}	22.2 %^{GT}
Voc	725 mV	729 mV	735 mV
FF	78.9 %	78.1 %	78.4 %
J_{sc}	37.6 mA/cm^2	37.4 mA/cm^2	38.6 mA/cm^2

Figure 1.6: Si-HJT 2.0 cell performance compared to monofacial Gen 1 and bifacial Gen 2 cells.

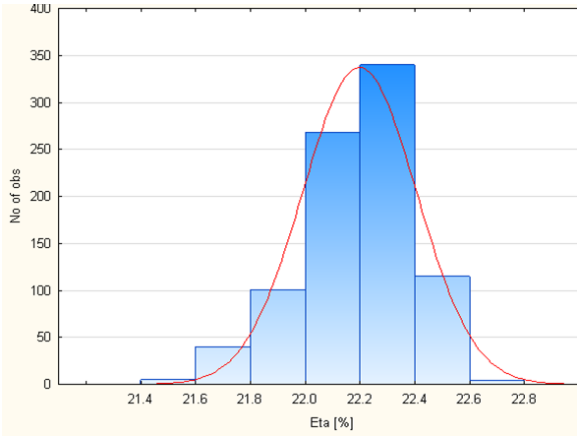


Figure 1.7: efficiency distribution of >850 Gen3.1 cells as measured with the Grid^{TOUCH} contacting unit..

Table 1.3: Gen3.1 cell median and best IV parameters, measured using the PASAN Grid^{TOUCH} technology.

	eff (%^{GT})	V_{oc} (mV)	FF (%)	J_{sc} (mA/cm^2)
best	22.65	737	79.3	38.76
median	22.2	734	78.4	38.56

The median cell efficiency is 22.2 %^{GT} and exceeds the target for bifacial device by 0.7%^{GT} absolute. The best device breaks the 22.5% mark with a recorded 22.65%^{GT} efficiency, mostly thanks to a high FF than the median cell efficiency. This achievement paves the way towards mean efficiencies higher than 22.5% with bifacial devices manufactured in production conditions.

Group 2: Si-HJT 2.0 with low cost a-Si processes

The group 2 of Gen 3 cells is similar to the group 1 in term of solar cell structure, but in addition to the Si-HJT 2.0 front side light management structure comprises new processes for the amorphous silicon layers as shown in Figure 1.8. The goal of these new layers is to reduce the manufacturing costs without impacting the conversion efficiency. Indeed, up to now the silicon layers have been developed to deliver the highest passivation quality without any compromise. These new layers are the results of questioning about what is mandatory or not to provide this excellence in surface passivation. The final process flow is not changed compared to the Si-HJT 2.0 structure as shown in Figure 1.9 and modifications compared to previous processes are mostly in recipes and hardware configuration. For obvious reasons, these modifications cannot be disclosed in the present document.

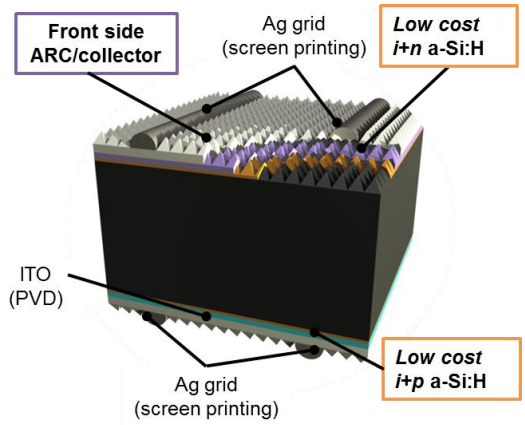


Figure 1.8: HJT solar cell structure used for Gen 3.2 cells.

Figure 1.9: process flow of Si-HJT Gen 2 cells

Figure 1.10 shows comparative cell conversion efficiencies between Si-HJT 2.0 cells with (left) and without (right) these new lost cost a-Si processes. We can see that from a statistical point of view there is no impact of these low cost processes on the efficiency that stands to median value of 22.4 $\%^{GT}$ in both cases. Figures 1.11 shows the efficiency distribution over more than 150 cells with these new processes. It shows that the profile is not a perfect Gaussian as for the Si-HJT 2.0 case (Figure 1.7) and that process uniformity is good. This is confirmed by the small gap between the median and champion cell parameters as shown in Table 1.4.

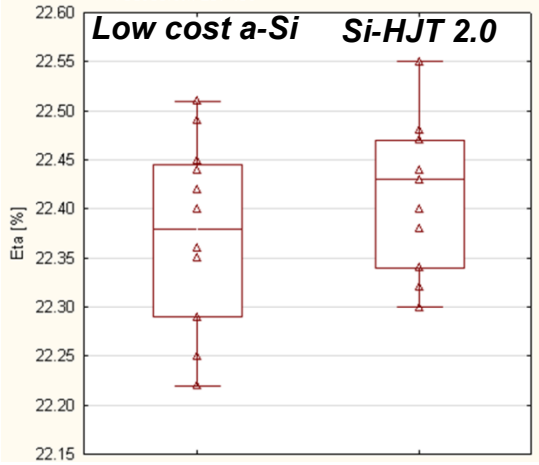


Figure 1.10: efficiency of low cost a-Si process (left) and regular a-Si processes (right). Both are made with the Si-HJT 2.0 structure.

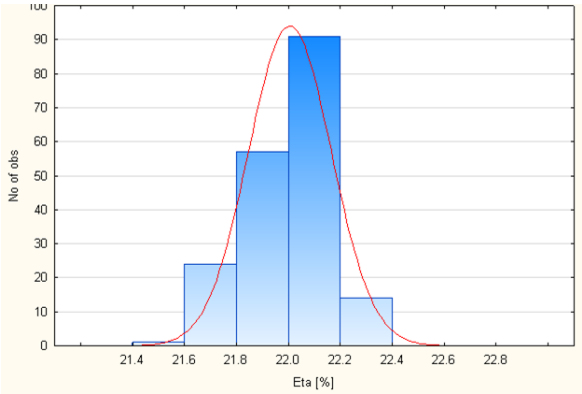


Figure 1.11: efficiency distribution of >150 Gen3 .2 cells as measured with the Grid^{TOUCH} contacting unit..

Table 1.4: Gen3.2 cell median and best IV parameters, measured using the PASAN Grid^{TOUCH} technology.

	eff (%^{GT})	V_{oc} (mV)	FF (%)	J_{sc} (mA/cm^2)
best	22.37	733	79.46	38.39
median	22.0	728	78.5	38.4

The produced Gen 3 cells with low cost a-Si processes have a slightly lower efficiency than the cells from Group 1 (22.2 %^{GT}) but are 0.5% absolute above the bifacial efficiency target. Without further notice, these new processes are integrated in all cells manufactured from this point in time.

Group 3: silver free Si-HJT cells

The third and last group of Gen 3 cells is made with the regular Si-HJT structure with front side ITO and the low cost a-Si processes of group 2. The special feature of these cells resides in the metal grids on front and back side. Indeed, as shown in Figure 1.12, the regular screen printed grids made of silver are replaced by copper grids made by electro-plating resulting in high aspect ratio metallic structures (Figure 1.13). The developed process is described in details in a dedicated section in the next chapter but is schematically represented in Figure 1.14.

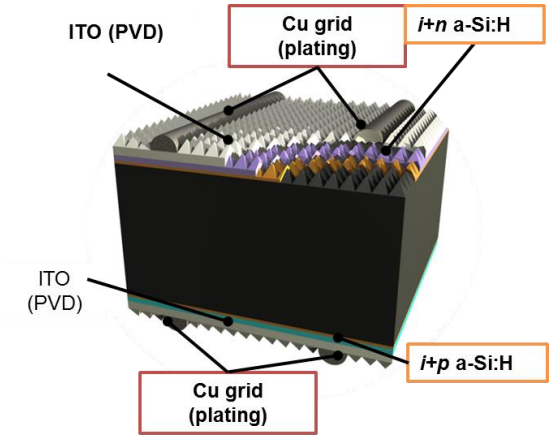


Figure 1.12: HJT solar cell structure used for Gen 3.3 cells.

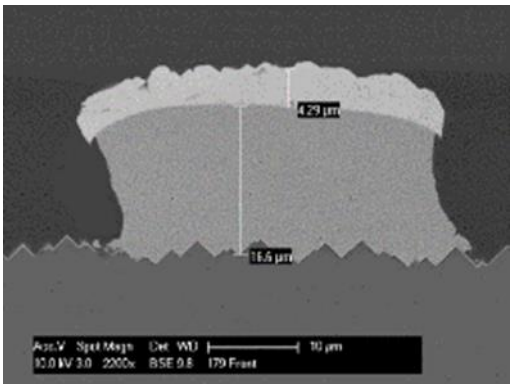


Figure 1.13: SEM micrograph of a plated finger made of copper and Sn.

We can see that the back end process flow is made of more process steps than regular screen printed grids. Indeed, the one tool process consisting in back side screen printing, paste drying, front side screen printing & paste curing is replaced by a four tool process.

- Metal blanket deposition on both sides by sputtering. This is done together with the front and back side ITO layers in an additional sputtering chamber.
- Negative masking of the blankets by inkjet deposition of hotmelt on both sides.
- Copper and tin electro plating
- Hotmelt lift-off and cell cleaning in chemical bathes
- Metallic blanket removal by wet-chemical etching

All these processes have been developed and demonstrated at the pilot scale (>20 wafers per hour) by CSEM.

From this very brief description, we can already see that the battle field between silver screen printing and copper plating will be material cost versus processing costs unless there is a significant cell performance advantage for one or the other.

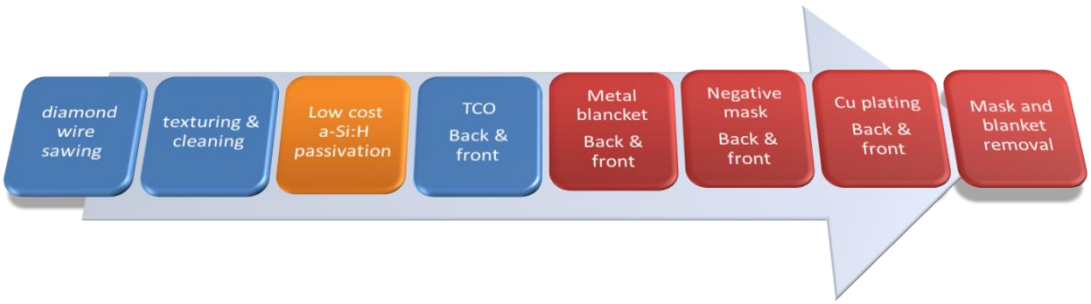


Figure 1.14: process flow of Si-HJT Gen 3.3 plated cells

Figure 1.15 presents the efficiency distribution of more than 130 bifacial cells made with copper plating in the pilot line of CSEM. It shows that the distribution is almost Gaussian with a quite narrow spread with all cells with 1% efficiency range. Median efficiency (Table 1.5) is of 22.3 $\%^{GT}$ and best efficiency is as high as 22.8 $\%^{GT}$. Despite the very similar efficiencies compared to Group 1 (Si-HJT 2.0) we can

see that the FF is higher by more than 1 %abs for the copper plated cells while the photo-generated current is very similar and V_{oc} lower by 5 mV for the copper plated cells. Tentative explanations to these differences may be:

- The higher FF is due to the better electrical conductivity of copper plated fingers as well as possibly better contact resistances of seed layer to ITO than screen printed silver. Plated fingers avoid the trade-off between photo-generated current and FF.
- The current are very similar and can be explained by the lower shadowing losses thanks to the narrower achieved lines by copper plating than with screen printing. This again without a trade-off between electrical and optical properties. Therefore, the current density gained by the Si-HJT 2.0 concept (group 1) is here compensated by narrower lines.
- The slightly lower V_{oc} of the copper plated cells may arise from plating process impact. Indeed, the cells are immerged into various chemicals (acidic, alkaline, and solvent) and one of these may impact the unprotected cell edge.

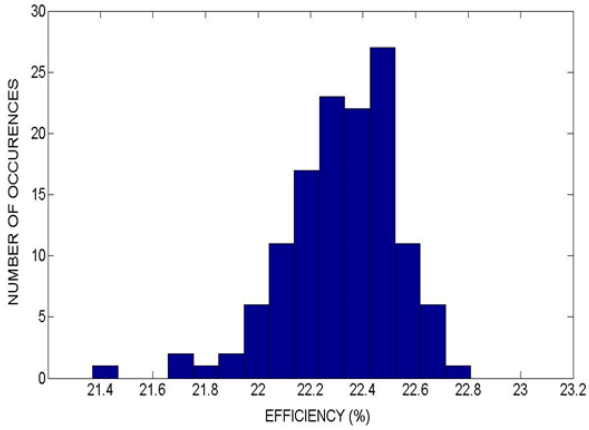


Figure 1.15: efficiency distribution of >130 Gen3.3 cells as measured with the Grid^{TOUCH} contacting unit..

Table 1.5: Gen3.3 cell median and best IV parameters, measured using the PASAN Grid^{TOUCH} technology.

	eff (%^{GT})	V_{oc} (mV)	FF (%)	J_{sc} (mA/cm^2)
best	22.8	734	81	38.4
median	22.3	729	80.1	38.2

Performance from Gen 1 to Gen3 HJT cells

Table 1.6 summarizes the production data from Gen 1 to Gen 3 cells. In general, along the duration of the project the efficiency has been improved from 21.5% ^{GT} to 22.3%^{GT} mean efficiency. More importantly, these results have been achieved while switching from monofacial (Gen 1 @ 21.5%^{GT}) to bifacial devices (Gen 3 @ 22.3 %^{GT}) that are not the ideal optical structure for champion cell manufacturing. Surprisingly, the main driver for this increase in efficiency has been the photo-generated current that rose by 1 mA/cm^2 and this despite the bifacial structure. In terms of pure performance, 2 major progresses have been integrated into these solar cells: i) the Si-HJT 2.0 structure and ii) copper plated grids. Both have shown individually their capacity to increase cell

efficiency with mass production compatible processes. These two innovations have not been combined yet, but if technicaly possible, this may lead to mean efficiency in the 23%^{GT} range by combining high FF (81%) and both benefits in terms of light management (J_{sc}= 38.8 mA/cm^2) and good passivation (V_{oc} = 735 mV).

Table 1.6: Gen 1 to Gen 3 cell median efficiencies

		Eff (%^{GT})	V_{oc} (mV)	FF (%)	J_{sc} (mA/cm^2)
Gen1	monofacial	21.5	725	78.9	37.6
Gen2	bifacial	21.29	728	78.1	37.41
Gen3.1	Si-HJT 2.0	22.2	734	78.4	38.56
Gen3.2	Si-HJT 2.0 low cost a-Si	22.0	728	78.5	38.4
Gen3.3	Low cost a-Si + Cu plating	22.32	729	80.1	38.2

1.2 Module production

1.2.1 Gen 2 SmartWire Module production

As described earlier in this report, the Gen 2 cells have been manufactured with a bifacial design as opposite to the Gen 1 cells which were exhibiting a full area sputtered metallization on the back side. Even though the Gen 2 cells are bifacial, they can be used either in monofacial modules with a white (or black) back sheet or in a bifacial module with a glass at the back side. In order to evaluate the module power and outdoor performance dependence on module back side design (backsheet or glass) Gen 2 cells have been divided in two groups and integrated in either glass/glass (G/G) bifacial modules or glass/white back sheet (G/BS) modules.

Both modules have a comparable bill of material (BOM) to Gen 1 modules as shown in Figure 1.16:

- ARC glass at front side
- TPO encapsulant
- 18 interconnecting wires with 200 μm core diameter
- InSn low temperature melting alloy coating on the wires
- PET foils to hold the interconnecting wires
- **White backsheet with aluminium or glass at back side.**
- Centralized junction box

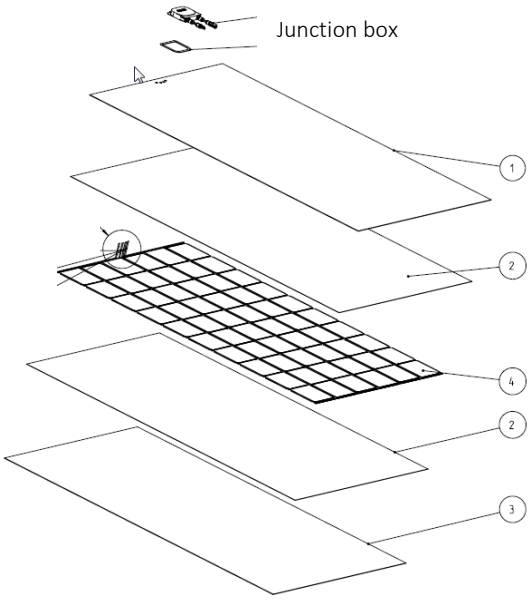


Figure 1.16: Gen 1 module layout with white back sheet (1), encapsulant (2), front glass (3) & cell matrix (4).

Figure 1.17: bifacial 60 cell module

Table 1.7 presents the measurement data of the 14 modules manufactured in the SmartWire pilot line at Meyer Burger in Thun. The 10 monofacial modules have been measured under STC using the Dragon Back technique. The remaining 4 bifacial modules have been measured in the same condition but in adding a black background at the back side of the module during measurement, to prevent surrounding light to enter the module and generate extra current.

Table 1.7: Gen 2 module performance under STC

Module ID	Remark	Cell P_{max} (W)	Module P_{max} (W)	V_{oc} (V)	I_{sc} (A)	FF (%)	CtM loss
15332	G/BS	5.04	297.3	43.65	9.10	74.8%	-1.7%
15333		5.08	300.7	43.79	9.12	75.3%	-1.3%
15334		5.14	301.0	43.79	9.13	75.3%	-2.3%
15335		5.08	297.7	43.93	9.12	74.3%	-2.3%
15336		5.12	298.9	44.02	9.16	74.1%	-2.7%
15337		5.17	303.1	44.28	9.14	74.9%	-2.3%
15338		5.08	294.2	43.67	9.11	74.0%	-3.4%
15339		5.09	295.1	43.8	9.08	74.2%	-3.4%
15340		5.13	297.3	43.84	9.10	74.5%	-3.4%
15341		5.15	299.1	44.03	9.13	74.4%	-3.2%
		average	**298.4**	**43.88**	**9.12**	**74.6%**	**-2.6%**
		median	**298.3**	**43.82**	**9.12**	**74.5%**	**-2.5%**
15344	G/G	5.09	287.7	43.92	8.72	75.1%	-5.8%
15345		5.04	286.9	43.84	8.70	75.2%	-5.2%
15346		5.04	283.3	43.53	8.73	74.5%	-6.4%
15347		~~5.04~~	~~218.2~~	~~42.41~~	~~8.75~~	~~58.8%~~	~~-27.9%~~
		average	**286.0**	**43.76**	**8.72**	**75.0%**	**-5.8%**
		median	**286.9**	**43.84**	**8.72**	**75.1%**	**-5.8%**

Without surprise, the highest module power has been achieved with the highest cell power class (5.17W) integrated in a monofacial module. The measured power was as high as 303 W!
Overall, the average module power with white back sheet is of 298 W and of 286 W with a transparent glass backside. One of the Glass/Glass modules has been removed from the analysis because of the presence of cracked cells after lamination.

More interesting than the average module power with the 2 different BOM, we should look to the module power output as a function of the cell output power. Indeed, as shown in Figure 1.18, as expected there is a linear dependency between module power and cell power and the glass/glass are well separated from the glass/back sheet modules, but present the same slope. As for bifacial cells, bifacial modules present a pretty low module power since they are measured with a black background without any reflection, either in the module, nor on the cell back side. This results in cell to module (CTM) power losses of about -6% (Table 1.7). The CTM power losses are reduced to -2.5% in the case of white back sheet modules since cell are measured with a black background (pejoration of current density) and a white reflector is added in the module, boosting the photo-generated current. This type of modules with white back reflector is perfect for high power density with single side illumination typically used for roof top integration. On the other hand, when evaluating the performance of bifacial module we have to take into account their bifacial character, i.e. their capability to convert diffused light into electric power, that is not taken into account so far in the standard testing conditions that impose black as a background.
As proposed earlier in this project (see 2015 Report), an easy and well accepted method is to take into account a 20% albedo (20% of AM1.5g illumination at back side) multiplied by the bifaciality of the module (ratio of power generation under STC back:front side):

$$Isc_{comp} = (1 + 0.2 \times \text{Bifaciality}) \times Isc_{front}$$

The bifaciality compensated module power by this means is presented in green in Figure 1.18 and represents an average module power of 338 W if integrated in a system with a 20% albedo factor. This power accounts for a module bifaciality of 89% that was measured under STC.

The Gen 2 modules presented here have demonstrated that even if only bifacial cells are used, two types of products can be manufactured: monofacial and bifacial modules. These two types of products even if having the same solar cell engine can target two different markets: i) private rooftop installation with monofacial design and ii) large commercial or utility field with bifacial modules. Both have outstanding performance with either high peak power or very high bifaciality compensated power.

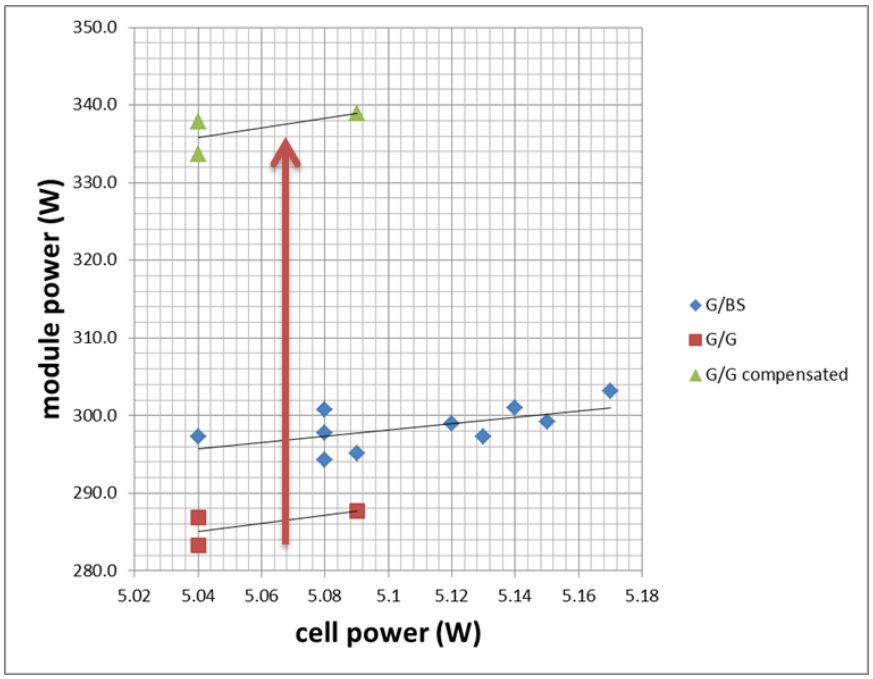


Figure 1.18: module power as a function of cell power class for (blue) G/back sheet modules, (red) Glass/Glass modules measured with black back ground and (green) bifaciality compensated glass/glass modules taking into account a 20% albedo and 89% measured bifaciality.

1.2.2 Gen 3 SmartWire Module production

The aim of Gen 2 modules was to introduce the first bifacial modules with a rather standard module balance of material (BOM). For Gen 3 modules, beside novelties at the cell level as described above, new module components are introduced with the aim to reduce the manufacturing costs while increasing the bifacial module power output.

First of all, in order to increase the benefit of the bifacial structure of these modules new junction boxes have been used. These decentralized junction boxes shown in Figure 1.19 present the advantage to reduce the cell overlapping area and hence increase the module bifaciality thanks to reduced light shadowing. The measured bifaciality using these decentralized junction boxes was increased up to 93 %, from the 89% measured with single centralized junction box. All Gen 3 modules are manufactured using this new type of junction boxes.

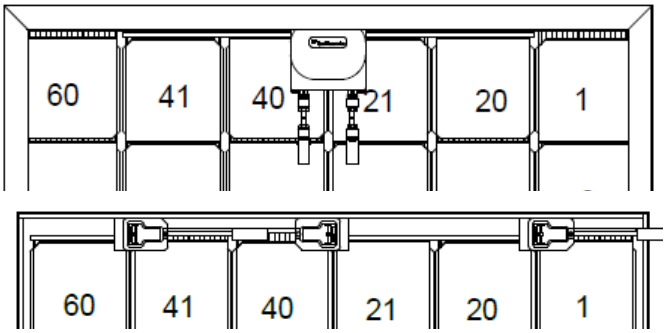


Figure 1.19: (top) single centralized junction box used for Gen 1 and Gen 2 modules and (bottom) multiple decentralized junction box used for Gen 3 modules.

Another module power limitation in the case of Gen 1 and Gen 2 modules is the interconnection wire core diameter. Indeed, the 200 μm diameter used for these modules limits the current extraction and impacts the module FF. However, this wire diameter is optimizing the cost to power ratio since the indium based coating of the wire is too costly when used on larger diameter wires. Gen 3 modules are all made with 300 μm wires either coated with indium tin (InSn) layer or tin bismuth (SnBi) layer. The SnBi coating makes economically feasible the introduction of 300 μm wires (see cost section below) and the goal here is to demonstrate that the low cost SiBn coating can replace the indium based coating without module power loss.
Additionnaly, some monofacial modules with a white back sheet have been manufactured as reference to be compared to Gen 1 and Gen 2 modules.

The module BOM for Gen 3 modules can be then summarized as following:

- ARC glass at front side
- TPO encapsulant
- 18 interconnecting wires with **300 μm** core diameter
- **InSn or SnBi** low temperature melting alloy coating on the wires
- PET foils to hold the interconnecting wires
- Glass at back side or white backsheet with Aluminium.
- **De-centralized junction boxes.**

Table 1.8 summarizes the combination between the different cell structures and module configuratios. A total of 14 modules have been manufactured including 2 glass / back sheet modules. As shown, no module integrating the copper plated cells has been manufactured so far because of time constrains. However, these modules will be described and analyzed in the complementary report end of 2017 together with the reporting about the long term outdoor monitoring of all module generations.

Table 1.8: Gen 3 modules description for the 4 groups

	Cells	module	wires
1	Si-HJT 2.0	bifacial	InSn 18x300 μm
2	Si-HJT 2.0	White backsheet	InSn 18x300 μm
3	Si-HJT 2.0	Bifacial	SnBi 18x300 μm
4	Si-HJT 2.0 Low cost a-Si	bifacial	InSn 18x300 μm

Table 1.9 displays the measurement data under STC of all modules manufactured with Gen 3 cells. Measurements of bifacial modules have been performed using a white reflecting background and therefore the data cannot be compared to the Gen 2 bifacial.

Table 1.9: Gen 3 modules parameters under STC.

Module ID	cells	module	Cell power (W)	Module power (W)	V_{oc} (V)	I_{sc} (A)	FF	CtM
15371	Si-HJT 2.0	GG InSn 300	5.22	292.54	44.12	8.92	74.31%	-6.64%
15372			5.23	293.12	44.10	8.95	74.23%	-6.66%
15373			5.27	294.57	44.16	8.93	74.72%	-6.84%
15374			5.27	295.62	44.18	8.94	74.85%	-6.51%
15375			5.27	294.52	44.14	8.95	74.55%	-6.86%
Average – 1			**5.25**	**294.07**	**44.14**	**8.94**	**0.75**	**-6.7%**
Median – 1			**5.27**	**294.52**	**44.14**	**8.94**	**0.75**	**-6.7%**
15377	Si-HJT 2.0	GBS InSn 300	5.28	296.00	44.23	8.92	75.09%	-6.60%
15379			5.29	298.20	44.25	8.94	75.40%	-6.03%
Average – 2			**5.28**	**294.53**	**44.05**	**8.93**	**0.75**	**-7.1%**
Median – 2			**5.28**	**296.00**	**44.23**	**8.94**	**0.75**	**-6.6%**
15380	Si-HJT 2.0	GG SnBi 300	5.33	297.1	44.256	8.887	75.54%	-7.09%
15381			5.33	297.52	44.256	8.91	75.45%	-6.96%
15382			5.33	299.70	44.34	8.95	75.52%	-6.28%
15383			5.32	298.95	44.33	8.91	75.67%	-6.30%
Average – 3			**5.33**	**298.32**	**44.30**	**8.91**	**0.76**	**-6.7%**
Median – 3			**5.33**	**298.24**	**44.29**	**8.91**	**0.76**	**-6.6%**
11405	Si-HJT 2.0 low cost a-Si	GG InSn 300	5.28	297	43.89	8.95	75.51%	-6.25%
21405			5.28	298	43.91	8.98	75.49%	-5.93%
31405			5.23	295.0	43.75	8.97	75.08%	-5.99%
Average – 4			**5.26**	**296.7**	**43.85**	**8.97**	**0.7536**	**-6.05%**
Median – 4			**5.28**	**297**	**43.89**	**8.97**	**0.7549**	**-5.99%**

As all modules were measured with a white reflecting background, no differences can be observed between glass/glass bifacial modules and glass/back-sheet monofacial modules. This is shown in Figure 1.20 where all the output power of all modules stand on the same line as a function of the cell power.

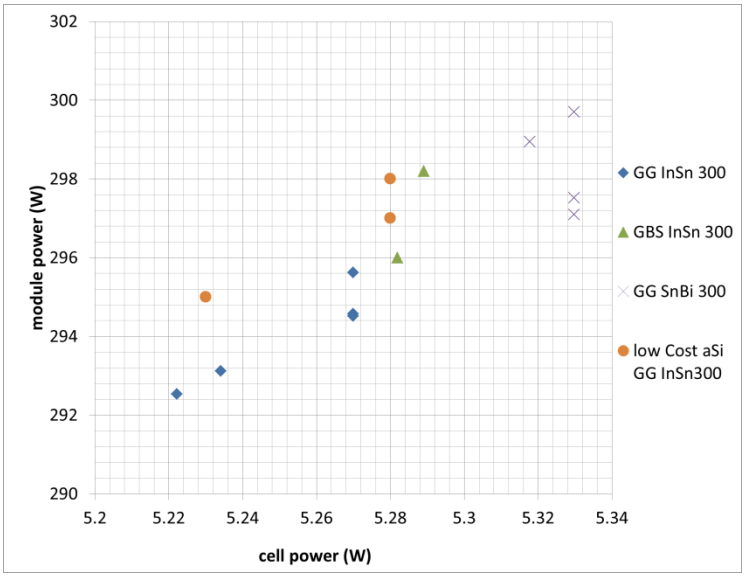


Figure 1.20: Gen 3 module output power as a function of average cell output power. All modules have been measured with a white reflecting background.

However, when looking closer to the data we can see that the CTM power losses are all about -6.4%, higher than for the Gen 2 glass white back sheet modules (-2.5%), even though comparable to the glass/glass module (-5.8%). But remember that the Gen 2 bifacial modules were measured with black unreflective back ground and the Gen 3 with a white reflecting background. Therefore, we would expect to have CTM power losses comparable to Gen 2 monofacial modules. Moreover, as the interconnecting wires for the Gen 3 modules are thicker (300 vs 200 μm) than for Gen 2, we would expect an additional reduction in the FF CTM losses. Unfortunately, this is not observed and the FF CTM losses are in both cases about -4% (relative).
Today, no reasonable explanation can be given to explain this difference between Gen 2 and Gen 3 module CTM losses. These differences have not been observed on the test modules manufactured before this Gen 3 large module series. Investigations are still ongoing and only hypothesis can be drawn for the time being:

- The difference in wafer thickness may be at the origin of the difference in I_{sc} CTM losses between Gen 2 (+2%rel with 150 μm thick wafers) and Gen 3 (-3%rel, 180 μm thick wafers).
- However, we have to take into account that the wire diameter is not the same for Gen 2 (200 μm) and Gen 3 (300 μm) modules, introducing extra shading losses for the second.
- The missing gain in FF when switching from 200 to 300 μm thick wires has no explanation so far. Wire to cell metallization contact could be one possible cause but again, pretests have shown that this was not the case.

To summarize, as shown in Figure 1.12 the measured module power is not as high as expected. Indeed, the cell power improvement from ~5.1 W to ~5.3 W was not transformed into module power improvement. With CTM power losses similar to Gen 2 the module power should have been around 310 W (green area in Figure 1.12) and taking into account for the switch from 200 to 300 μm thick wires the module power should have be even higher, in the range of 320 W (red area in Figure 1.12). As already said, investigations are ongoing and new modules with similar BOM will be manufactured again to demonstrate these expected power levels.

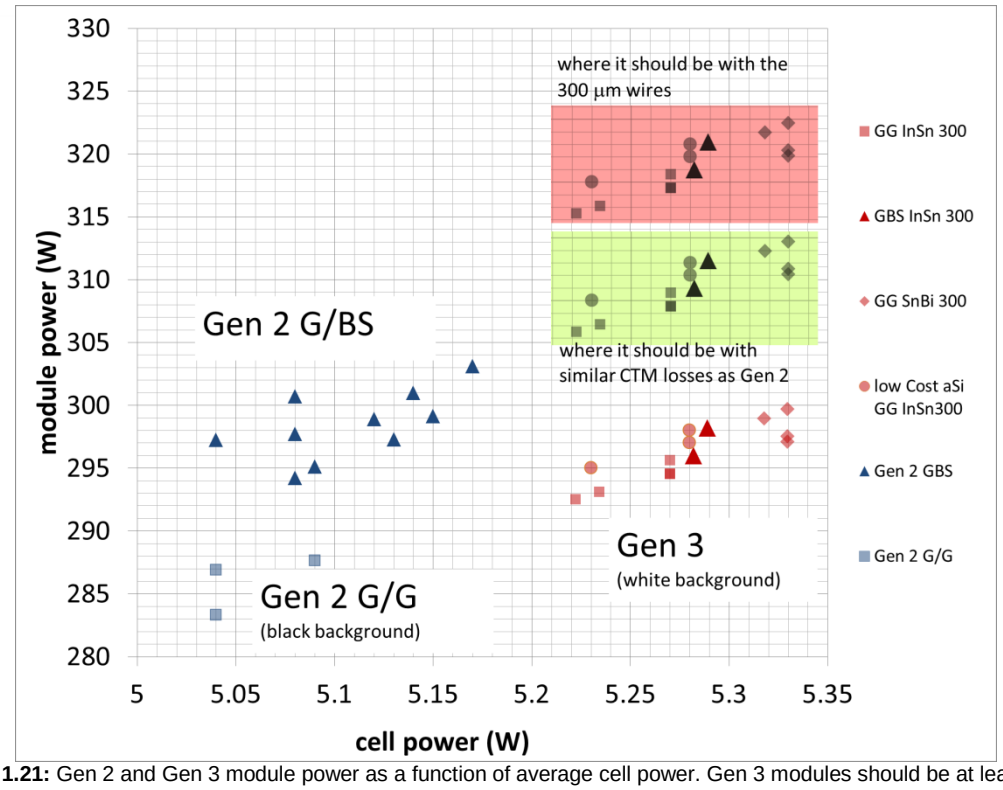


Figure 1.21: Gen 2 and Gen 3 module power as a function of average cell power. Gen 3 modules should be at least 10 W higher in power.

Nevertheless, when comparing the different module groups when can draw some positive conclusions:

1. Indium tin coating on wires can be replaced by tin bismuth without extra CTM losses. This can be seen in Figure 1.21 where all modules are standing on the line independently to the coating used on the wire. Moreover, the best module out of this Gen 3 production is a module with bismuth tin coating.
2. The low cost a-Si processes do not impact the module power as well. It could even improve by ~1W the module power as shown in Figure 1.20, but more statistics is needed to have a more reliable statement.

Figure 1.22 summarizes all modules and cell output power from Gen 1 to Gen 3 modules that have been developed and manufactured within the Swiss Inno-HJT project. Starting from the Gen 1 monofacial cells and modules, it can be seen that a huge progress has been realized. First, managing the transition from monofacial to bifacial cells generating a gain in monofacial module output power of more than 15 W. Second, the introduction of new technologies and processes at the cell level resulted in an important gain in power output at the cell level. Bifacial cells with more than 5.3 W were manufactured with a narrow distribution. However, for still unknown reasons, we were not able to convert this improvement in cell power output into module power improvement. Preliminary tests were successful and investigations are still ongoing to understand and solve this issue

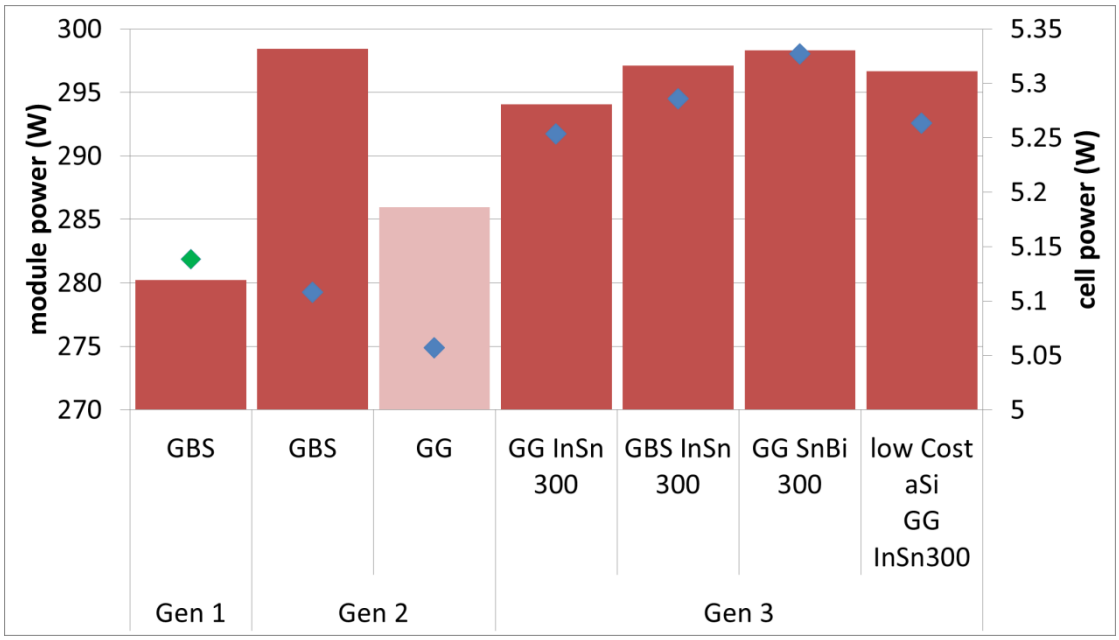


Figure 1.22: average power output of cells and modules produced within the *Swiss Inno-HJT* project. The Gen 2 GG modules (light red bar) are the only one measured whithout white reflecting background and therefore direct comparison with the other modules is difficult. The gen 1 cells (green diamond) are the only monofacial cells presented here.

A total of 39 good modules have been produced within the Swiss Inno-HJT project, cumulating a peak power output of 11'353 Wp. Thirty of these modules together with 10 reference modules have been installed for outdoor monitoring in Hauterive, Neuchâtel (see Figure 2.12). Data are discussed in a separate section in this report and will be consolidated by end of 2017 after 1 full year of outdoor acquisition for all Generations of modules.

Figure 1.23: outdoor installation of 40 module, 10 reference and 30 modules produced within the *Swiss Inno-HJT* project

1.3 Manufacturing cost analysis

Manufacturing costs for the different cells and module configuration presented above have been evaluated. Since material costs have dramatically dropped mid 2016 because of production over capacity, the figures presented in this section cannot be fairly compared to the Gen 1 module manufacturing costs that have been presented in the 2015 report. As a reminder, the Gen 1 manufacturing costs were 0.64 CHF/W_p, hitting the 0.65 CHF/W_p Swiss Inno-HJT cost target.

The cost analysis presented here take into account the latest material costs that are viable for the producer at least on mid-term. As an example, monocrystalline wafer can be found at prices as low as 0.9 $ (~CHF) per piece for standard 180 μm thickness. End of 2015 this price was at 1.1 $ per piece. We decided not to be too optimistic and we have selected a price that is reliable on a more long term target, i.e. 1 $ per piece for a standard thickness.

Cost calculations were done with the following assumptions:

- Production capacity of about 200 MW, corresponding to 2 production lines.
- Production site in Asia (China, Malaysia,…)
- Depreciation duration of equipment of 7 years (building 30 years).
- Interest rate of 0% (generally agreed to compare different technologies)
- Wafer cost based on latest announcement of wafer manufacturer with target price of 0.7 $ per piece for as cut thickness of 130 μm in 2020.

Table 1.10 presents the manufacturing costs for different configurations with costs separated for wafer, cell and module parts. As for the module power comparison in the previous section, only modules measured with a white reflecting background are presented in this table. The last column presents what could be a target for HJT modules in 2020.
First of all, we can note that all steps, wafers, cells and modules have their importance in reducing the costs. The wafers, as discussed in the previous paragraph have a major impact. For Gen 2 modules, the used thickness was 150 μm, 30 μm thinner than for Gen 1 and Gen 3 modules accounting for a ~10% module cost reduction. In the future, 130 μm as cut thickness will be available from wafer manufacture thanks to diamond wire cutting technology and they will be key to further reduce the module costs.

About the cell cost, there has been an important decline in production costs with the introduction of Si-HJT 2.0 cell structure, -20% cell manufacturing costs, and low cost a-Si processes, -12%. A total of 30% cell manufacturing cost reduction has been achieved, accounting for 10 CHF (-8%) module cost. Further, improvements in terms of cell manufacturing are foreseen mostly in terms of equipment cost reduction by the introduction of new manufacturing technologies. These should be ready at the horizon 2020 and offer about 25% cost reduction in cell manufacturing.

Despite the difficulties encountered to transfer the increased power output of the Si-HJT2.0 cells into the module, a major milestone has been achieved with the successful introduction of the tin bismuth coating on the wire. It has been shown that no power difference between the original InSn coating and the new SnBi was observed, but more importantly, this material substitution reduces considerably the wire costs. Indeed, 300 μm core wire diameter can be used with the SnBi coating instead of the 200 μm InSn wire together with a cost reduction of about 2 CHF per module. Overall, it is now possible to shift the module structure from monofacial glass/backsheet to bifacial glass/glass while reducing the module manufacturing costs from 40.6 CHF to 39 CHF per module. Further progresses on both the equipment and the BOM will reasonably lead to a module manufacturing cost reduction of about 10%.

Table 1.10: cost analysis of Gen 2 and Gen 3 modules. Gen x represents an achievable cost target.

	Gen 2	Gen 3				Gen x
Cell type	Si-HJT bifacial	Si-HJT 2.0	Si-HJT 2.0	Si-HJT 2.0	Si-HJT 2.0 Low cost a-Si	Si-HJT 2.0 Low cost a-Si
Module type	G/BS 200 µm InSn @ 298 W	G/G 300 µm InSn @ 294 W	G/BS 300 µm InSn @ 297 W	G/G 300 µm SnBi @ 298 W	G/G 300 µm InSn @ 297 W	G/G 300 µm SnBi @ 315 W
N type mono c-Si wafer per wafer	0.82 CHF (150 µm)	1 CHF (180 µm)	1 CHF (180 µm)	1 CHF (180 µm)	1 CHF (180 µm)	0.7 CHF (130 µm)
Cell manufacturing per cell	0.51 CHF	0.4 CHF	0.4 CHF	0.4 CHF	0.35 CHF	0.26 CHF
Module manufacturing per module	40.6 CHF	47 CHF	44 CHF	39 CHF	47 CHF	35 CHF
Total module cost per module	121 CHF	131 CHF	128 CHF	123 CHF	128 CHF	93 CHF
CHF/Wp	**0.41 CHF/Wp**	**0.45 CHF/W_p**	**0.44 CHF/W_p**	**0.41 CHF/W_p**	**0.43 CHF/W_p**	**0.30 CHF/W_p**

Overall, similar total manufacturing costs per module have been reached for both monofacial (121 CHF) and bifacial (123 CHF) modules. The resulting cost per watt is by far below the target and reaches 0.41 CHF/W_p. Of course, the technologies and processes developed within the Swiss Inno-HJT project helped greatly to achieve this target but this drastic decrease over 2016 from 0.64 down to 0.41 CHF/W_p was made possible as well because of the material cost decrease. Taking the best of each module, we can state that it should be possible today to demonstrate a 310 W with manufacturing cost of about 110 CHF by using 150 µm thick wafers, Si-HJT 2.0 cells with low cost a-Si processes and 300 µm SnBi interconnecting wires, thus achieving <0.36 CHF/W_p. Looking at the 2020 horizon, access to 130 µm thick as cut wafers, further investment reduction both at the cell and module manufacturing level and further cost down thanks to material utilization together combined with a reasonable 315 W module power would make possible to achieve module production cost below 0.3 CHF/W_p.

2. Development activities

In parallel to the preparation and production of the Gen 2 and Gen 3 cells and modules, R&D efforts have been made to improve cost and performance along the full value chain. In this section, some highlights are presented.

2.1 Thin wafers

Using thinner wafers than standard thickness poses challenges for cell processing due to changed mechanical properties that cause increased flexibility but at the same time increased wafer breakage and for cell performance. If both challenges are mastered sufficiently thickness reduction should translate into device cost reduction.

During the project the impact of wafer thickness on mechanical yield was studied for manual and automated wafer handling. Since manual handling yield strongly depends on experience we have observed an expected yield loss going to thinner wafers. While breakage rates are not considerably higher for wafers with an as cut thickness of down to 130µm, which translates into cell thickness of around 110µm, the breakage rate increases notably when cell thicknesses drops below 100µm.

Within the project devices as thin as 50µm have been processed, where the mechanical yield was typically only around 50%.
Monitoring the mechanical yield an automated production line revealed also that processing of wafers with as cut thicknesses of 130µm, i.e. 110µm precursor thickness after wet chemical precursor preparation did not lower mechanical yield. Even processes with high mechanical load on the wafers especially the screen printing did not turn out to be critical in terms of mechanical and electrical yield. The process most critical for as cut wafers thinner than 130µm is the wet chemistry, where increased wafer flexibility caused issues with wafers sticking due to adhesion forces when the wafers are removed from the process liquid.
Yield issues were observed with individual automation stations that sort wafers in and out of carriers, however, those issues were observed not to depend on wafer thickness down to 130µm. For wafer thinner than 130µm an adaptation of the wafer handling in the wet chemistry process would be required to allow high yield processing, the loads on the cell precursors during screen printing needs to be carefully adjusted for precursor thicknesses below 100µm even if successful printing on precursors as thin as 50µm has been demonstrated.
In conclusion cell processing with as cut wafers as thin as 130µm was investigated and found to operate at high yield without thickness related issues.

Cell performance will ideally change little or even not at all when thinner wafers are used for processing. It has been shown that traditional diffusion type silicon cells and even modern rear side passivated (PERC) cells show decline in cell performance when thinner wafers are used. The challenge here is to compensate the reduced silicon absorber volume of the cell by high quality surfaces that minimize losses at the same, which is a key signature for heterojunction technology.
HJT cells with different thickness have been processed and characterized.

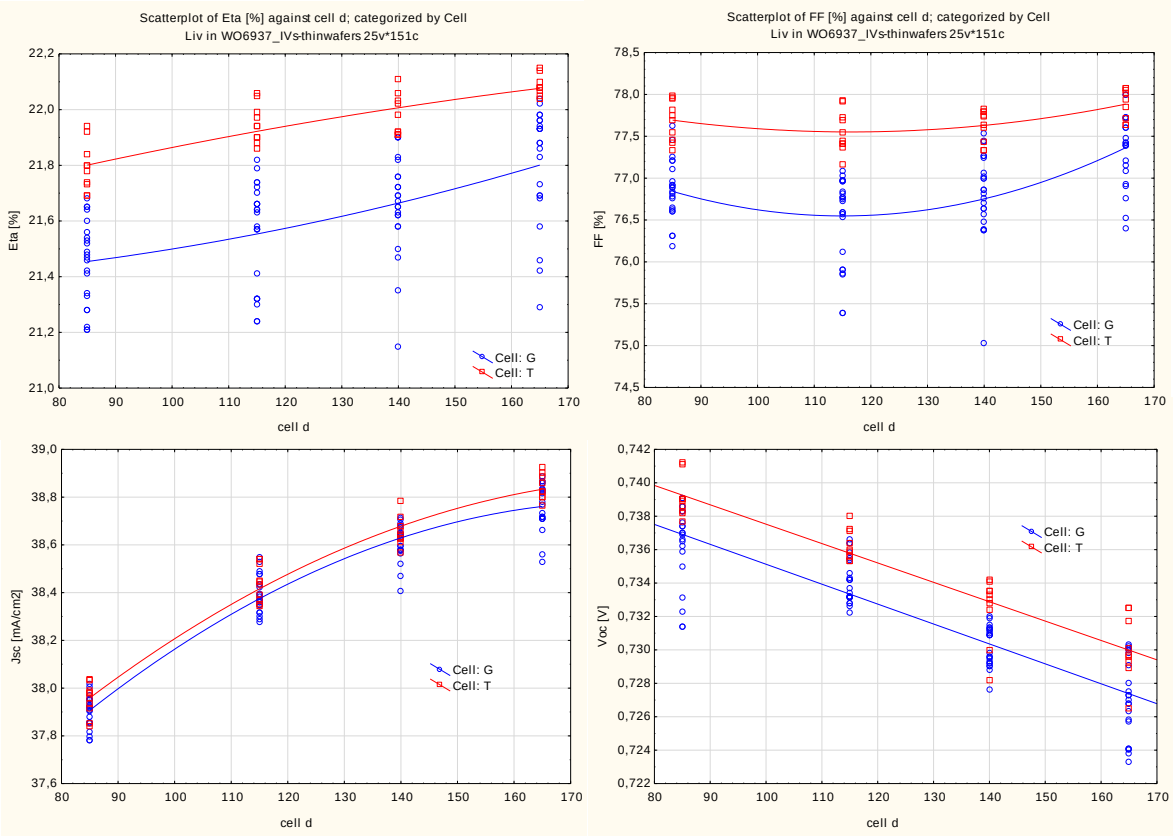


Figure 2.1: HJT cell parameters for cells made from different wafer thicknesses as a function of cell thickness.

As shown in Figure 2.1, as expected Voc increases with decreasing cell thickness due to a very effective surface passivation while Jsc decreases due to the reduced absorber volume and implied optical losses. The FF is nearly independent of thickness and as a result cell efficiency changes only little with the latter.

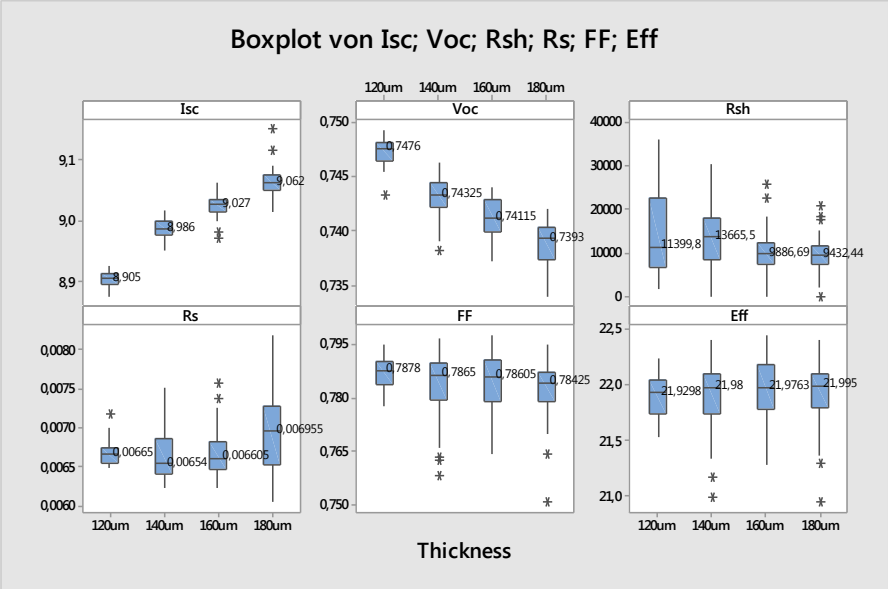


Figure 2.2: Cell parameters from ell processed on MB's HJT production line displayed vs. the as cut wafer thickness. Final cell thickness is around 20µm less.

Similar results were obtained from test lots run on automated production tools that exhibited a practically thickness independent performance for cell thicknesses down to 100µm.

One of the most effective ways towards cost saving is reduction of wafer thickness that allows for a lower wafer costs and thus impacting directly all subsequent cost structures. Wafering for mono crystalline silicon by diamond wire has found wide spread industrial application since 2013. While at the beginning of the project the standard diameter for the diamond wire was 100µm, today the saws with their respective wire management system facilitate handling of wires as thin as 60µm as applied and developed in MB's R&D. Combined with a controlled cut of thin wafers this reduces the so called kerf and thus allows to yield more wafers from the same silicon ingot crystal. The standard wafer thickness at the beginning of the project was 180µm while current cell production at Meyer Burger uses wafers with a thickness of 135µm. Owing tool development for the saws not only the capability of handling thinner core-wire was developed but also the throughput, i.e. the productivity of the tool was considerably increased to more than twice. The cost reduction stemming from these advancements in wafering translate to approximately 30% for a conservative calculation to approximately 40% for a more realistic estimate with the above given numbers.
This trend is reflected in current market spot prices; however the standard market wafer thickness with now around 170µm is still considerably much thicker than above mentioned 135µm as cut wafers.

With processing yield, cell efficiency and wafer cost issues address as above it can be concluded that thin wafers can now be used in MB's HJT production with practically no performance loss and a large cost advantage. The cost advantage translates 1 to 1 to cell and module costs.

2.2 Ozone process

At the beginning of the Swiss Inno-HJT project the wet chemistry wafer texturing and cleaning process was based on hydrogen peroxide and nitric acid. Both are used because of their oxidising power and the later in high concentration while the first is volatile and needs a constant feeding to the process.
Therefore, these chemicals are the cost drivers in the wet processing and they require increased safety measures for stock keeping and application.
An alternative chemical with high oxidising power know from semiconductor industry which is finding more and more application also in the PV industry is ozone (O_3). The ozone is generated, mixed into the process liquid and destroyed on-side. It has the advantage of being virtually contamination free being generated from much less costly oxygen in gas form (O_2), which is much less demanding and dangerous in storage. While hydrogen peroxide and nitric acid need to be applied in high concentrations in the %-range, ozone is dissolved and very effective in much lower concentrations of the ppma-range.
With the much favourable cost structure, the ozone-based chemistry needs to perform on the same level. This was developed, optimised in many single aspects and ultimately achieved for an entirely ozone-based wet chemical process replacing hydrogen peroxide and nitric acid entirely.

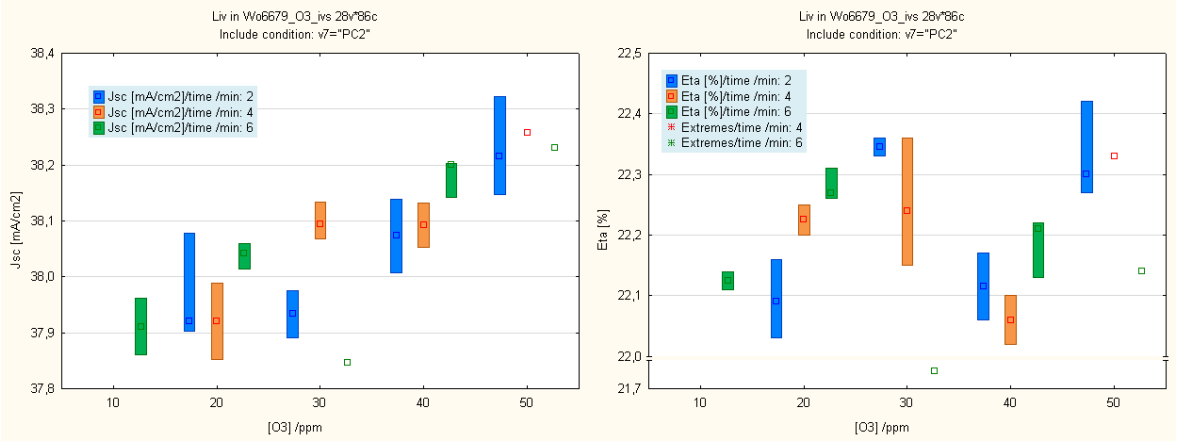


Figure 2.3: Short circuit current and efficiency of HJT cells as a function of ozone concentration [O_3]

In the wet chemical processing two major oxidising process steps are applied; an oxidation for the incoming wafers, cleaning the wafer surfaces from coarse contamination by destroying surface attached organics and a final oxidation for ultimate surface cleaning.
Above pictured influence of 1st oxidation as a function of the ozone process step shows that the texturing quality can be improved by ozone and thus the cells yield higher current and efficiency η that also surpasses level of the previously hydrogen peroxide based process step.
The final surface clean is a key process step that determines how well the surface can be passivated. The development of this process step has obtained most attention. By developing ozone based chemistry we were able to further improve the previously nitric acid based surface cleaning.
Furthermore, due to the more effective cleaning it is now possible to omit process steps that needed to be applied previously, making not only the process much more cost effective by reducing the running costs, but also allowing to reduce size and cost of the wet bench thus lowering the financial market entry barrier.
Calculation for the reduction of the cost of ownership when switching to ozone chemistry is in the range of 30-40%. Cost savings on the wet bench tool and new processing with reduced process steps should translate to a further cost saving of around 20% for the wet processing.

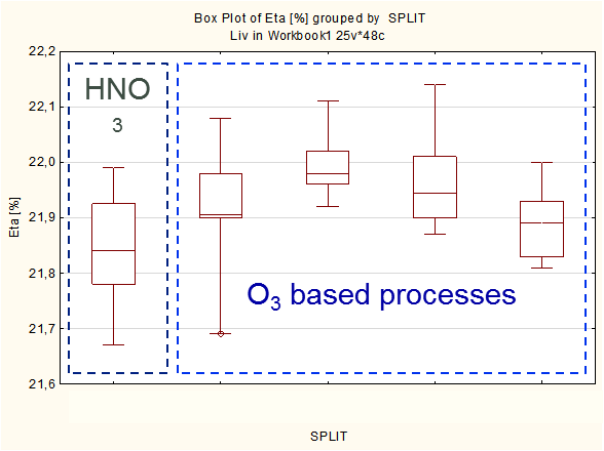


Figure 2.4: Efficiencies of HJT cells for various surface conditions, i.e. final clean processes

2.3 Advanced metallization

An intrinsic process limitation of HJT solar cells is the requirement for a low temperature processing consecutively to the a-Si:H layers depositions, to not degrade its passivation properties. This imposes the use of Ag pastes with curing temperatures typically below 250 ^{0}C. The printing of state-of-the-art low-temperature cured Ag pastes yields Ag lines with bulk resistivity with 6 to 10 $\times 10^{-6}$ Ohm·cm, about a factor 2 to 3 higher than state-of-the-art metallization based on firing-through of high-temperature Ag pastes. The higher Ag line bulk resistance for HJT solar cells when compared to homojunction solar cells therefore imposes economical and performance limitations for standard H-pattern metallization with 2 to 5 busbars: more Ag is required to achieve similar line resistance and lines with higher resistivity or larger dimension have to be employed. Using state-of-the-art low-temperature cured Ag pastes for H-pattern cells with 3 to 5 busbars, improved performance can for instance be achieved using multiple printing, and typical laydown mass of Ag of 180 mg per side can be considered, representing, for an assumed Ag price of 500 $/kg, a metallization cost of 9 $cts/cell, and for a cell > 22.5 % typically ~ 1.68 $cts/Wp per side, or 3.36 $cts/Wp for a bifacial cell (as assumption and simplification, Ag paste cost is considered equivalent to Ag price, taken at 500 $/kg in this report). To overcome this cost and performance limitation due to the metallization, two main routes were addressed in the frame of the *Swiss Inno HJT* project, with strong focus on:

- Relaxing the constraints on the metal grid conductance by using multi-wire interconnection: this enables for development and integration of fine-line printing of low temperature cured Ag (providing performance gain and cost reduction), and of alternative material and deposition techniques;
- Enhancing the metal grid conductance by switching to copper plated fingers: this approach was studied for varied modules configurations, from standard busbar/ribbon to shingling direct cell interconnections, and multi-wires.

Overall, a very complete metallization and interconnection platform was set-up at CSEM for the *Swiss Inno-HJT* project, providing CSEM with key expertise and know-how, with flexible fabrication equipment and high performance processes, and with detailed characterization and simulation tools, for the metallization and the interconnection of cells and modules using advanced industrial technologies.

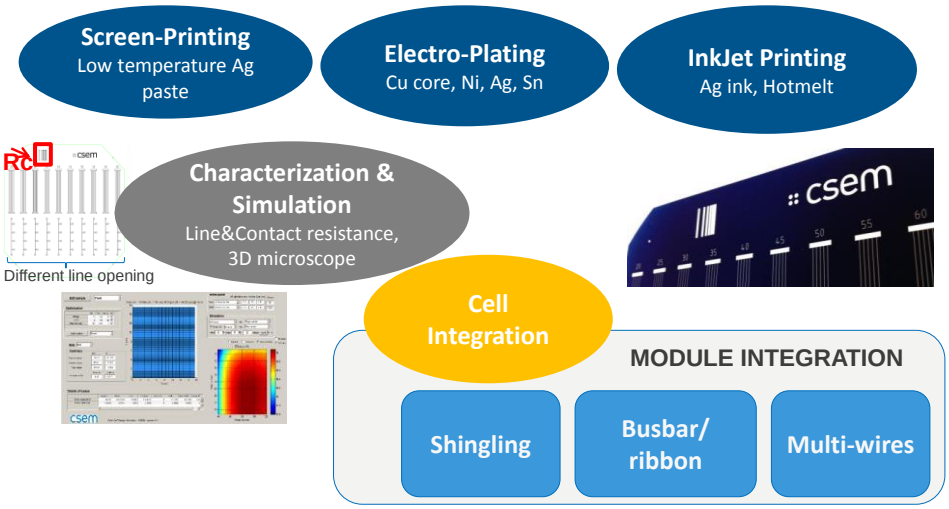


Figure 2.5: CSEM platforms for metallization and interconnection developed in Swiss Inno HJT project.

Printing developments

In the case of busbar/ribbon interconnection design, the cell metal fingers should demonstrate a line resistance < 0.5 Ω/cm to not yield resistive losses. Screen-printing parameters and pastes were first optimized to achieve the line resistance target with a minimum of Ag usage and with minimum line width. All these developments, taking into account recent progress of Ag pastes, lead to:

- 5 busbars cell, printed fingers properties: line spreading of 70 to 80 µm, line resistance of Ag < 0.5 Ω/cm, deposited weight of 220 mg for bifacial cells, corresponding to ~ 11 $cts/wafer (see Figure 2.6 top-left).

With the use of SmartWire technology, the constraint on the conduction of the cell metal fingers is strongly relaxed, and typical line resistance of up to 5-8 Ω/cm does not yield resistive losses. A strong focus was therefore set in the project on the development of fine-line printing of low-temperature cured Ag pastes. By working on the evaluation of different pastes, different screens, openings, and different printing parameters, fine-line printing and ultra-fine line printing could be achieved:

- SmartWire interconnection, fine-line: line spreading of 30 to 40 µm, line resistance of Ag < 6 Ω/cm, deposited weight of 60 mg for bifacial cells, ~ 3 $cts/wafer (see Figure 2.6 top-middle).
- SmartWire interconnection, ultra-fine-line: line spreading down to 16 µm, achieved with advanced mesh orientation/design, screen costs then overcomes Ag savings, not competitive (see Figure 2.6 top right).

In addition, developments were conducted on alternative printed materials and printing technologies. The screen-printing of Copper based paste cured at low temperature was evaluated (see Figure 2.6 bottom left), and the inkjet printing of Ag inks cured at low temperature was developed (see Figure 2.6 bottom right). The different properties of the achieved figures of the lines printed are summarized in Figure 2.6, as listed here above. At present stage, the copper based paste does not provide sufficient costs reduction with respect to Ag paste, while the Ag inks used in inkjet printing have high costs, so that the two alternative materials and technologies evaluated are not yet at competitive level with respect to fine-line printing of Ag lines.

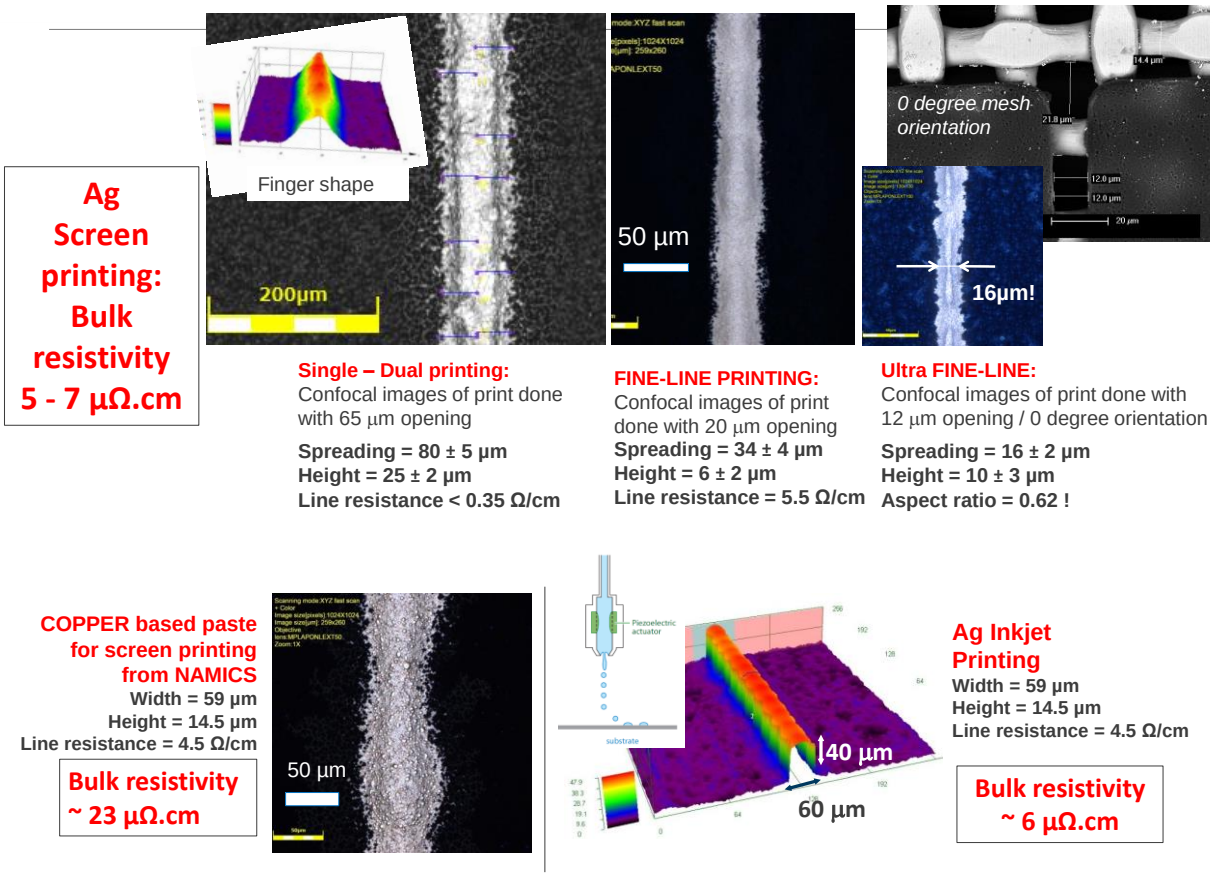


Figure 2.6: Summary of properties of lines printed at CSEM following developments on screen-printing and inkjet-printing. Top: left: printing optimized for low line resistance (< 0.35 Ω/cm, but with 80 µm spreading and high Ag consumption > 100 mg per side), middle: printing optimized for fine line (sufficient line conductance for integration in SmartWire without performance loss, only 34 µm spreading reducing shadowing losses, only 30 mg Ag per side), right: printing strategy developed for ultra fine line (some of finest fingers ever printed on HJT cells, only 16 µm large, but using more expensive screens). Bottom: left: printing optimized for Copper based pastes (high bulk resistivity), right: inkjet printing of Ag inks (compatible for SmartWire, however high costs of Ag inks).

Plating developments

A strong focus was set in the project on the full development of materials, processes, technologies and fabrication equipment for the definition of a plating technology for bifacial silicon heterojunction solar cells, compatible with line dimensions < 50 µm. Over the course of the project, the needed technologies have been developed, optimized and matured.

In the metallization of HJT cells by electroplating, patterning is needed to define the front and back metallic grid geometries. This step creates an insulating layer on the seed-layer with small cavities where the subsequent growth of the metallic finger will occur. In the *Swiss Inno HJT* project, an industrially compatible process based on inkjet printing of an insulating hotmelt ink was chosen. In this process, the hotmelt is heated until becoming liquid inside the printing head and then solidifies when reaching the substrate surface. A crucial point in the development of printing recipes is the determination of the resolution. Indeed, a high printing resolution although allowing the realization of small geometries leads to an important ink consumption and to long printing time. Here, this tradeoff between the printing speed, the ink consumption and the minimal feature size achievable is managed by using a two steps approach for the front-side patterning: First, a low-resolution print defines the rough shape of the finger by creating openings in the 200 µm range [see Fig. 2.7 a)]. Then, a second

print is carried out by using this time a high resolution print which accurately defines the finger edges [Fig. 2.7 b)]. Therefore, by using this two steps approach, extremely narrow geometries as small as ~30 µm can be obtained while maintaining a low hotmelt consumption. At the rear-side, due to the "mesh" geometry featuring lines at 45° and as the optical constraints are relaxed compared to the front-side, a single print approach is used achieving geometries in the 60 um range as shown in Fig. 2.7 c), printing at lower-resolution (i.e. requiring less printing time) is investigated. In the framework of the *Swiss Inno HJT* project, this process was applied at the back-side of the cell therefore reducing the processing time and the hotmelt ink consumption [Fig. 2.8]. This process can be as well applied at the front side and demonstrates the feasibility of opening of ~30 µm thus suppressing the need of a second print. However, the sidewalls achieved with this process will not be as vertical as in the standard two-step approach resulting in wider fingers if a thick Cu layer is grown.

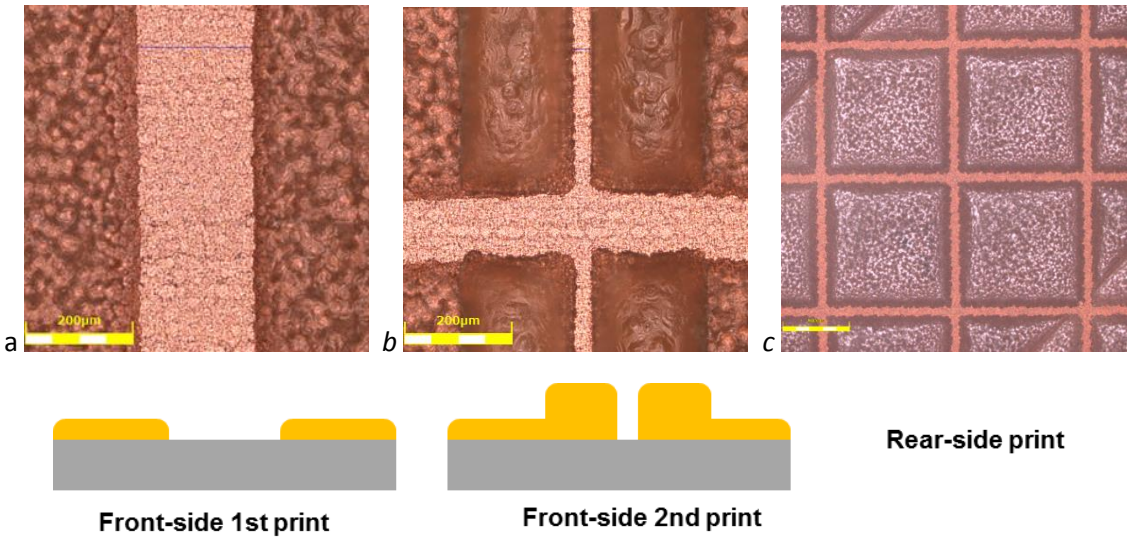


Figure 2.7: Finger opening in the hotmelt layer: a) after the 1st low-resolution print, b) after the high-resolution print. c) Hotmelt layer at the rear side with the "mesh" geometry.

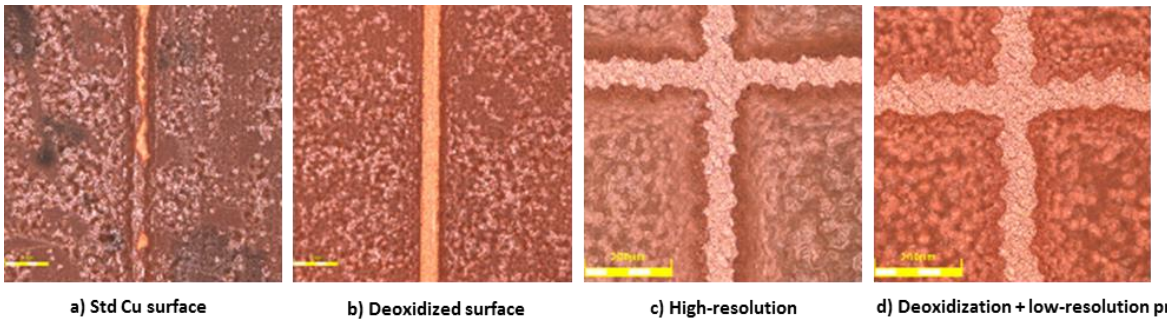


Figure 2.8: *Low-resolution print on : a) a standard surface, b) a deoxidized Cu surface. c) Standard high-resolution print at the rear-side. d) Low-resolution replacement print for the rear-side.*

After the patterning definition, the following processes are carried out: wafer preparation, bifacial plating in 1-go, finish layers, hotmelt removal, and seed-layer etch-back. All these different processes are done in the plating R&D pilot line developed in the frame of the project together with the Swiss company Alfatech Galvano SA. The pilot line was installed in CSEM new metallization and module facility in Innoparc, Hauterive, next to Meyer Burger Research pilot line infrastructure. The line is shown in Figure 2.9. The developed process flow, conducted in the developed and ramped-up pilot line, was qualified with the processing of > 130 Gen3 cells, with tight distribution in achieved cell

performance, and with the high performance attained (22.3 % average efficiency for a maximum efficiency at 22.8 %).

Figure 2.9: Picture of the CSEM R&D pilot line for plated metallization.

The processes and designs were then optimized for different module integration strategies, with geometries optimized for bifacial busbarless cells interconnected using SmartWire technology, for bifacial 3 busbars cells interconnected using ribbons or light capturing ribbons, and for bifacial cells segments designed for shingling direct interconnection using conductive adhesives applied for instance by dispensing. Pictures of developed 6'' wafer cells for these different module integration strategies are presented in Figure 2.10.

Figure 2.10: Pictures of full wafer 6'' silicon heterojunction cells with the different plated metallization grid patterns defined, respectively for busbarless bifacial cells, 3 busbars bifacial cells and bifacial cells with specific design for cell segmentation followed by direct interconnection ("shingling")..

Technology Comparison

The performance achieved with the different metallization materials and processes can be summarized in graphics presenting the line resistance (key for low electrical losses) versus the optical width (key for optical performance, defining shadowing losses). This can be analyzed at the cell level, but also, and more importantly, at the module level. Going from cell to module, the finger shape is taken into account, as depending on this shape and on the metallization reflectance, light can be recollected by internal light trapping in the module, reducing the optical width to an "effective" optical width. In Figure 2.11 all the developed metallization materials and technologies are represented. This clearly demonstrates that:

- < 0.5 Ω/cm can be achieved with ~ 30 µm effective optical width in the case of plating and with ~ 50 µm effective optical width in the case of printing. A performance gain of about 1.1 % relative can be accounted for by switching to plated metallization. In such configuration, the Ag costs amounts for typically about 11 $cts/wafer.
- < 6 Ω/cm can be achieved with ~ 20 µm effective optical width in the case of the developed plating (could be achieved with finer fingers but not adapted to the patterning methods developed so-far) and with ~ 25 µm effective optical width in the case of the developed fine-line printing. A performance gain of about 0.3 % relative can be accounted for by switching to plated metallization. In such configuration, the Ag costs amounts for typically about 3 $cts/wafer.

Regarding material costs, the Ag costs varies strongly between the two modules integration routes, with typically about 11 $cts/wafer for the busbar/ribbon case, and down to only 3 $cts/wafer for the SmartWire case. In the case of plating, the chemistry and anodes costs are limited, and can be estimated to typically 0.5 $ct/wafer. For plating, the material costs are dominated by the patterning material costs, which will be only slightly different between the 2 modules configurations: a total amount of 1 g of hotmelt per cell has to be considered, representing about 4.3 $cts/wafer (low resolution back). Switching to a low-resolution 1-step processing both for front and back, the consumption could even be more limited, ending to about 0.76 g per cell, therefore to about 3.3

$cts/wafer. The plating materials costs therefore amounts to about 4.8 $cts/wafer, with a potential for reduction to ~ 3.8 $cts/wafer.

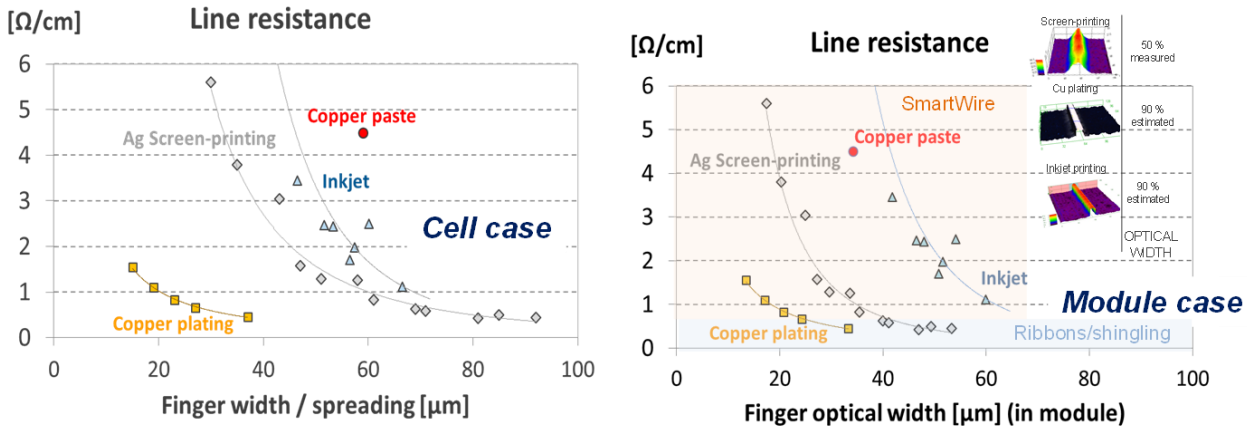


Figure 2.11: Line resistance vs. finger width (optical width in the cell performance case) and finger optical width (optical width to be considered in the module case) of the different metallization lines fabricated at CSEM during the project.

	Potential performance gain w plating	Ag costs	Plating materials costs (patterning + chemistry + anodes)	Cost/Wp based on a printed cell w. 5.3 W.
5 busbars	+ 1.1% relative	11 $cts/wafer	4.8 $cts/wafer	1.9 $cts/Wp for Ag 0.9 $cts/Wp for Cu
SmartWire	+ 0.3 % relative	3 $cts/wafer	4.8 $cts/wafer	0.56 $cts/Wp for Ag 0.9 $cts/Wp for Cu

The costs given in the table above are based on a Ag cost of 500 $/kg. In the case of a Ag cost increase > 850 $/kg, the present plating solution would become the most competitive technological approach.

Achievements for Gen2 and Gen3 modules

The two developed routes, i.e. copper plating for metallization combined with any module interconnection technology, and fine-line Ag printing for metallization combined with SmartWire module, enable to cancel the initial limitation of the metallization costs. The project developments are therefore successful, providing two pathways for cost competitive metallization of silicon heterojunction solar cells, both routes validated and qualified on pilot lines equipment and on the different cells produced in the project.

At present stage, for a Ag cost of 500 $/kg, and for the present patterning costs for plating, the fine-line printing of Ag combined with SmartWire demonstrates to be the most competitive solution. The Gen2 bifacial cells were therefore metallized using fine-line printing, benchmarked to a “robust” printing using large fingers and more Ag. Overall, 800 Gen2 bifacial cells were printed using a maximum Ag total weight of 60 mg, with stable performance and tight efficiency distribution. Thanks to the finer fingers, the fine line printed cells demonstrate a gain in current generation of ~ 0.3 mA/cm2 with respect to the robust print. In the module case, this current gain is compensated by a FF loss, typically of about 1 % absolute, and the powers of Gen2 modules then lie all in the 300 W range. This demonstrates that low Ag content is compatible with high performance modules fabrication.

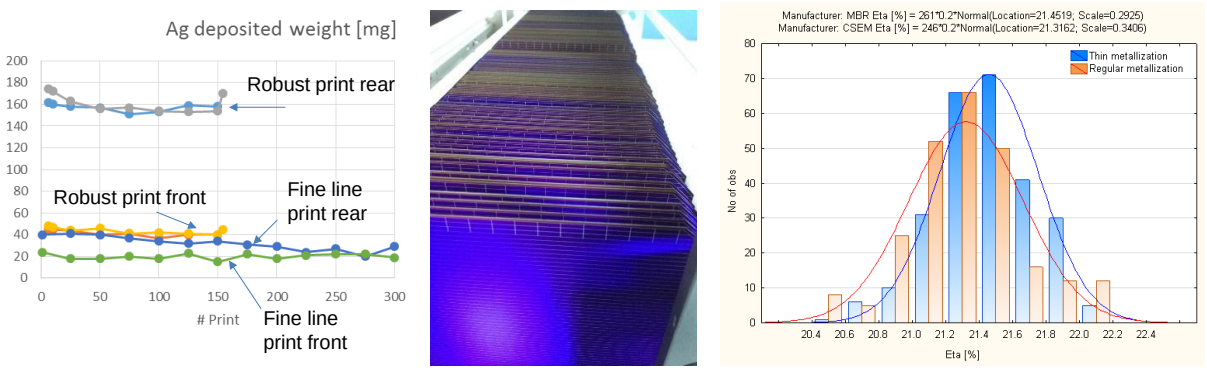


Figure 2.12: Distribution of printed Ag weight on the 1'000 Gen2 cells, demonstrating low Ag content (< 60 mg for fine line printed bifacial cells).

Similar light print /fine-line printing was then used for Gen3 cells, for a total of 920 cells. The distribution of the Ag weight laydown on the cell is detailed in Figure 2.13 for both front and rear side of the fabricated cells, demonstrating the reliability of the developed processes. The printed Gen3 cells therefore demonstrate very low Ag content, with typically < 60 mg total amount of Ag for bifacial cells, and only ~ 20 mg of Ag for the front side metallization.

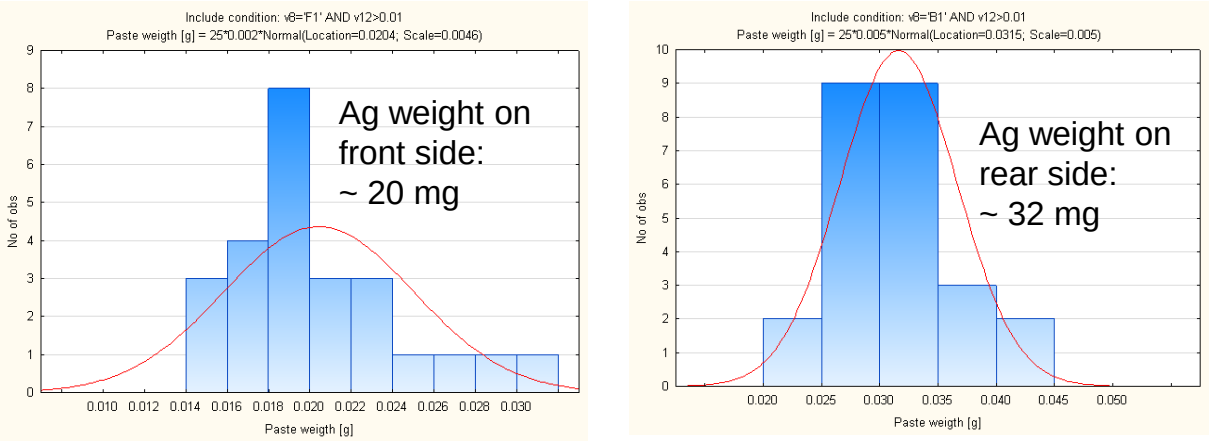


Figure 2.13: Distributions of Ag laydown weight on front side and rear side of Gen3 printed bifacial cells (distribution over the 800 cells fabricated).

Finally, a batch of more than 130 cells was used for evaluation of the plating metallization developed in the project, for busbarless bifacial heterojunction solar cells. The achieved plated grid metallization was very uniform over the cells batch, with high FF maintained over the 130 cells, enabling to achieve a tight efficiency distribution, with an average efficiency at 22.3 %, for a maximum efficiency of 22.8 %.

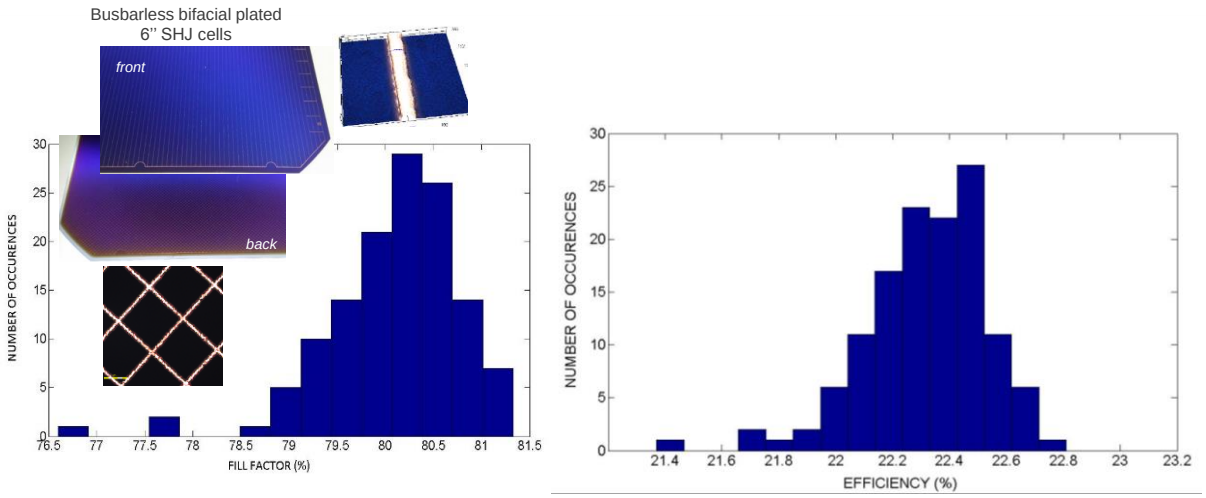


Figure 2.14: Performance achieved on the > 130 cells plated using patterning and plating processes, materials and designs developed in the project, demonstrating high efficiency and tight efficiency distribution.

The cells and modules developed in the project confirm and qualify the developments conducted on the metallization and interconnection of full wafer 6'' heterojunction cells. The fine-line printing and SmartWire combination is validated with > 1'500 cells pilot processing, while the plating processes were validated on > 130 cells pilot processing. These cells and modules demonstrate that the initial costs limitation due to the usage of low temperature cured Ag is suppressed by switching to SmartWire interconnection combined with fine line printing, or to plated metallization.

Record module

Sunpower is the only industrial Si cells & modules maker producing in large scale 21% modules since 2013. Technologies involved on these modules are very costly and our goal was to demonstrate that this module efficiency could be reached by combining the heterojunction cells and SWCT module technologies.

HJT-SWCT modules installed on the Swiss Inno HJT outdoor stand present efficiency between 18-19% and have been built to be cost competitive compare to mainstream module market. To achieve a 21% module, we have listed the power losses roots causes at cell and module and determine potential gain of different improvements.

Changing the shape of the cell was one of the most effective ways to improve module efficiency. Indeed, PV module is based on rectangular shape glass filled with 60 pseudo square shape heterojunction cells. Placed next to the others pseudo square cells leave empty diamond shape spaces in module as show in Figure 2.15. Our solution is to replace these pseudo-square cells by rectangular shape cells.

Figure 2.15: on left, picture of a regular SWCT module based on PSQ cells, the white diamond shape between cells produces no power. On right, rectangular shape cells leave minimal area between the cells, high cell density in module.

Rectangular shape cells are produced as regular pseudo-square HJT cells despite an extra laser engraving too form 156x121mm cells.
Table 2.1 shows module performances of two modules based on similar cells either with pseudo-square shape or realized with rectangular 156x121mm cells. A power gain of 5.6% was obtained with the module based on rectangular shape cells. This result confirms interest to use rectangular shape cells. Moreover these rectangular shape cells produce individually less current and ohmic losses on SWCT interconnections are thereby reduced (higher module FF) and more efficient is the module.

Table 2.1: Modules performances based on HJT cells of two different shapes: Pseudo-square (PSQ) and rectangular shape (121x156mm). A power gain of 5.6% is obtained thanks to rectangular shape cells.

Module based on	Power [W]	Voc [V]	Isc [A]	FF [%]	Module area [m2]	Wp/m2
PSQ cells	76.7	11.6	8.7	74.7	0.406	189
Rectangular cells	78.1	14.6	6.9	77.3	0.397	197

Based on these cell & module concepts many studies were conducted to improve steps by steps module efficiency: optimization of cell antireflection coatings, choice of best suitable wafer, improvement of the laser engraving step, optimization of the SWCT wire number & dimension, selection of most transparent module encapsulants…..
The Table 2.2 below resumes the more efficient modules obtained so far in the Swiss Inno HJT project. 21% module was obtained in small area (0.4m^2) and 20.8% module was achieved with 78 rectangular shape cells on large area 1.5 m2.

Table 2.2 : Resume of higher efficiency modules produced in the SwissInno project. The 21.5% module is based on heterojunction cells from Meyer Burger Germany.

Module Efficiency [%]	Module area [m^2]	Power [W]	Voc [V]	Isc [A]	FF [%]	Cells number & size
21.0	0.406	**80.3**	14.7	7	77.7	20x rectangular HJT (121*156mm)
20.8	1.49	**310**	57	7.2	75.8	78x rectangular HJT (121x156mm)
21.5	1.53	**330**	44.5	9.5	78.5	60x M2 HJT (156.5x156.5mm almost rectangular)

The work achieved on the rectangular shaped wafers and on module integration optimization made possible the manufacturing of a 21.5% module based on Heterojunction solar cells and SWCT. Cells used on this record module were based the most efficient cells produced by Meyer burger Germany production lines. As for the 21% small area module, wafers used to build this module were almost rectangular in shape and module presents only very little diamond shape areas without cells.

3. Demonstration systems and performance monitoring

The first two phases of the demonstration systems were installed at the end of 2015 and have been fully operational since February 2016. Performance data for standard, non-standard innovative, and Swiss Inno HJT Gen 1 modules have been collected from these systems over the reporting period. In parallel, single-module monitoring continued on the Microcity building.

Over this reporting period, we improved the data analysis software to increase the robustness of the results. To improve the quality of temperature coefficients, we also introduced a new design for holding temperature sensors on to modules. As a result, temperature measurements have been stable over the reporting period. These changes made it possible in particular to calculate temperature coefficients over irradiance bands of only 25 W/m². The most stable values of the whole range of irradiance are the temperature coefficient of voltage:

- PERC modules: typically -0.30 %/°C
- HJT modules: typically -0.25 %/°C

The temperature coefficients of power are in line with expectations (between -0.25%/K and -0.30%/K for HJT modules, between -0.40%/K and -0.50%/K for PERC modules).

We also introduced new metrics in order better to characterize the performance of monitored modules at low irradiance:

- Values of short-circuit current, open-circuit voltage, and efficiency at 300 W/m² normalized, after temperature correction, to values in standard test conditions
- Maximum power conversion efficiency and the irradiance level at which it is obtained.

The main lesson that can be drawn from this year is that the main driver for annual performance ratio in Switzerland is the efficiency at 300 W/m² relative to the efficiency at STC. The correlation coefficient between performance ratio is indeed 0.83. On the other hand, the effect of the thermal coefficient of power on the performance ratio is negligible (correlation coefficient: 0.11). The HJT modules under monitoring on the Microcity building, in particular those manufactured by Meyer Burger in December 2014, rate highly on both metrics and therefore exhibit high performance ratios (Figure 3.1).

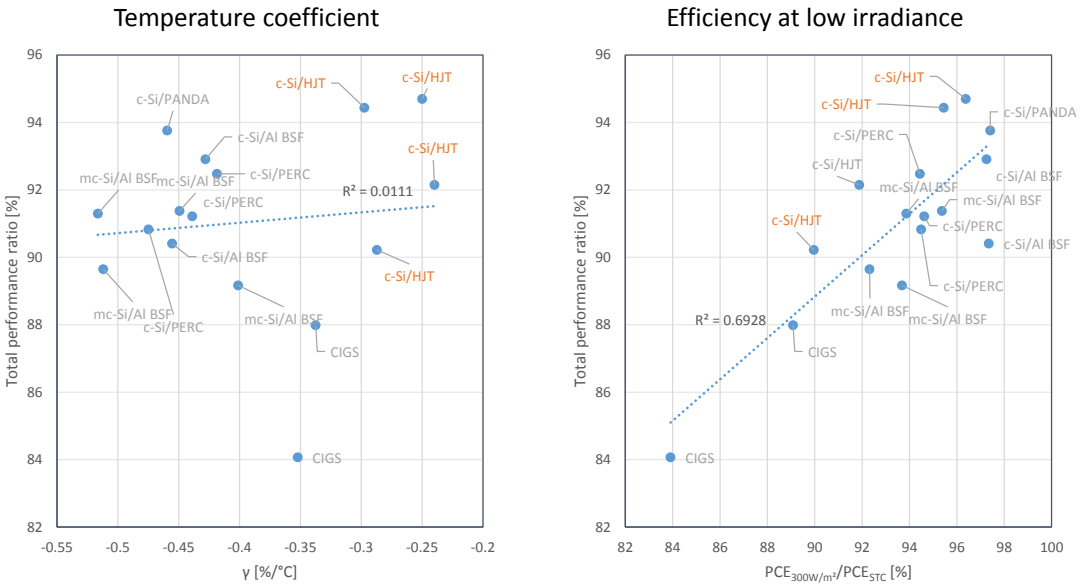


Figure 3.1: Performance ratio (PR) of the individual modules under monitoring on the Microcity building over the entire period as a function of the temperature coefficient of power (left) and the efficiency at 300 W/m² (average outdoor measurement) relative to the efficiency at STC (indoor measurement). Highlighted points are heterojunction modules from Meyer Burger. The temperature coefficient is a poor predictor of PR whereas the relationship between relative efficiency at 300 W/m² and PR is strong and can be approximated as linear with a fitting coefficient R^2=0.69.

Figure 3.2: Four 3 kWp demonstration systems installed on the Innoparc building in Hauterive (NE). In the foreground are frameless Gen 2 and Gen 3 modules connected in November 2016.

The architecture of the demonstration 3 kW_p systems is based on module-level DC/DC conversion combined with string inverters. We selected SolarEdge P405 module-level power optimizers since their voltage and power range is compatible with all the module technologies. They also provide

recordings of the generated power, energy, operating voltage, irradiance in the plane of array, and ambient temperature with a time resolution of one hour. These monitoring data are visible on the SolarEdge monitoring portal but require weekly downloading for detailed processing. In this reporting period, we developed software tools to streamline the treatment of data and the computation of key performance metrics.

The results observed on the first two of these 3 kW_p systems ("standard" technologies and Swiss Inno HJT Gen 1) were at first sight at odds with those observed on the Microcity building. Instead, the best performers on the demonstration systems were the worst in single-module monitoring (Solar Frontier CIGS modules), and the Swiss Inno HJT Gen 1 system showed lower than expected performance ratio. Over the available monitoring period (February to November 2016), the overall performance ratio of the Swiss Inno HJT Gen 1 system is 85%, instead of the expected 91%. The seasonal variations are also much lower than in single-module monitoring (monthly performance ratio varying between 0.84 and 0.94 for Gen 1 system, and between 63% and 98% in single-module monitoring of HJT modules). Since this stabilization of performance ratio is observed for all module technologies, we attribute it to the module-level power converters.

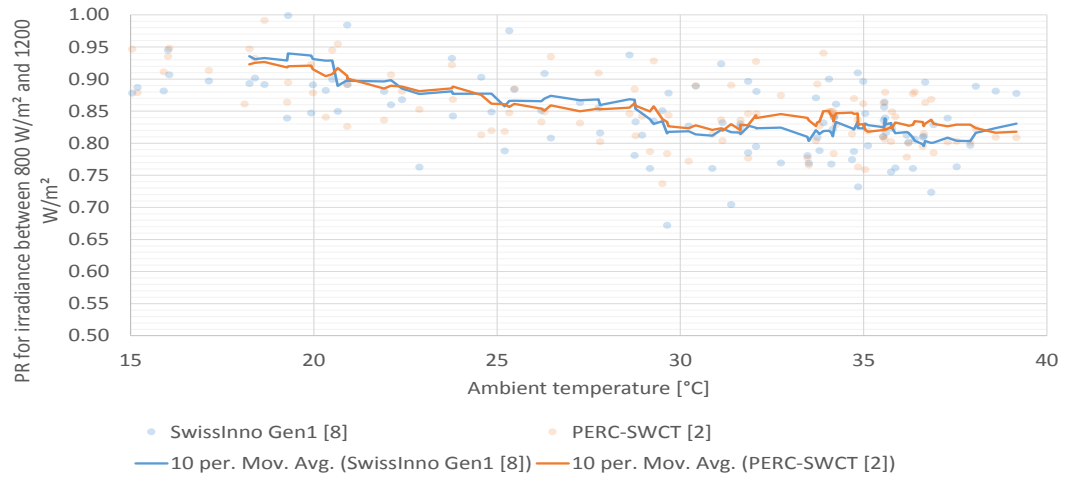


Figure 3.3: temperature dependence of performance ratio on the 3 kWp demonstration systems.

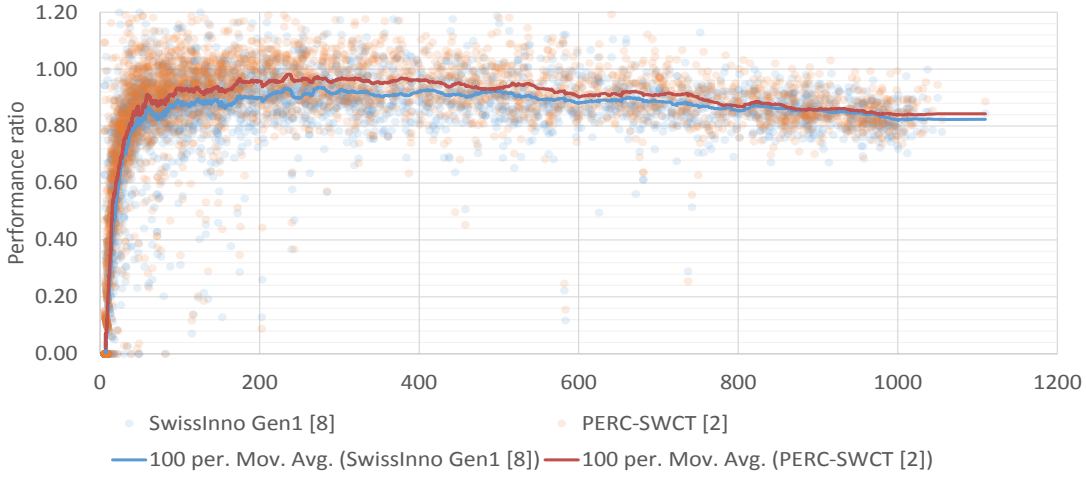


Figure 3.4: Irradiance dependence of the performance ratio on the demonstration 3 kWp systems.

Detailed analysis of how the performance of the demonstration systems depends on environmental conditions (Figures 3 and 4) however show consistent results with the observations done in single-module monitoring: the performance of HJT modules relative to other c-Si technologies improves with temperature, and the lower performance at low irradiance translates into lower performance ratio over the year. However, unlike the HJT modules tested on the Microcity building, the Gen 1 modules installed in the demonstration systems have a lower efficiency at low irradiance (normalized to their efficiency at STC) than standard or innovative c-Si technologies. The recommendation that can be drawn from this monitoring is therefore:

1. To enhance the performance ratio of modules to be installed in Switzerland or similar climates, future developments should therefore focus on improving the efficiency at low irradiance
2. Since the temperature dependence of the Gen 1 modules is as expected, they should be compared with standard technologies in hotter, sunnier climates where they may outperform

Finally, the remaining two 3 kW_p systems have been connected, with Gen 2 and Gen 3 modules respectively, on 31st November 2016 (Figure 3.2). The data collection is functional (Figure 3.5) but due to the limited amount of data it is too early to draw any conclusions. As planned, data collection and analysis on these systems will continue for another year after this commissioning.

Figure 3.5: Hourly energy production of the 20 modules forming the Gen 2 and Gen 3 demonstrating the operation of the data acquisition tool. Each curve represents one module. Data for quantitative analysis as shown on Figure 3.3 and Figure 3.4 are extracted from this tool.

4. Impact on MB product portfolio

The equipment installed in the R&D pilot lines at Meyer Burger, Meyer Burger Research and CSEM have been a key parameter in the development and introduction of new technologies in the Meyer burger portfolio. Indeed, not only production technology understandings and knowledge have been acquired during this project, but the impact of the project has been extremely important for the introduction of new technologies to increase the competitiveness of Meyer Burger products. As examples we can cite, the introduction of the thin wafers which are today standard in all Meyer Burger tool specifications (sawing, cell and module making), the introduction of new Si-HJT 2.0 solar cell concept that is currently being introduced to Meyer Burger customers or the low cost a-Si processes that are already being tested at the manufacturing scale.

National cooperation

The *Swiss Inno-HJT* project is based on a large consortium of competence centers. The Meyer Burger group is participating actively in R&D as well as production activities within the project. Meyer Burger AG (Thun) is working in the field of high speed crystal cutting using diamond wire technology as well as in module assembly by using the newly developed SmartWire Contacting Technology. Si-HJT solar cells are developed and produced by Meyer Burger Research AG (Hauterive, NE) and the efficiency measurement methods for cells and modules are achieved by PASAN SA (Neuchâtel). CSEM (Neuchâtel) is also active in the solar cell process by developing advanced metallization processes and materials, and by implementing at R&D pilot scale the electro plating of copper to replace the screen printed silver. CSEM is also in charge of the outdoor installation and monitoring of the produced modules within the project.

International cooperation

During the duration of the project, we have seen a great impact of the *Swiss Inno HJT* project on the HJT community at the international level. Indeed, thanks to the *Swiss Inno HJT* project, Switzerland is now considered as a main pole in HJT development with CSEM and Meyer Burger as technological leaders. The communication in international conferences about the creation of a pilot research line in Switzerland has generated a lot of request from the PV community. Thanks to the increased capacity in cell production while keeping the flexibility of R&D environment, CSEM and Meyer Burger are now able to support research labs all across the world by providing samples and are invited to participate to many European research projects (2 already running and >5 under submission or evaluation). We can already say that the *Swiss Inno HJT* is a great success in terms of R&D acceleration and place Meyer Burger and CSEM in a central position in Europe for international collaboration in the field of silicon heterojunction technology.

Evaluation 2016 and outlook for 2017

2016 has been extremely intense with the introduction of several major breakthroughs in terms of cell and module technologies in parallel to the production of more than 2’500 cells for the Gen 2 and Gen 3 Swiss Inno HJT modules. The Gen 2 production has been a great achievement with the introduction of bifacial cells and modules with a demonstrated module power of more than 300 W. However, the third generation of modules has not been as successful as the second. Indeed, despite all the success

in pushing the cell efficiency up to 22.8 % by the introduction of new cell structure, innovative PECVD process and copper plated metallization, we were not able to demonstrate higher module power than for Gen 2. Investigations are ongoing to understand the origin of this issue and solve it, while 2 modules implementing cells with copper metallization are under fabrication. Nevertheless, despite these limitations, extremely low production costs have been demonstrated, with down to 0.4 CHF/Wp module manufacturing costs reached, while perspectives for up to 310-320 Wp were shown, with close investigation on-going for corrective actions for future modules manufacturing to qualify this demonstrated potential.

Even if all milestones and deliverables of the project have been achieved, work will continue to first reduce the cell to module losses of the Gen 3 module and reach a module power of at least 315 W. Moreover, as planned originally, the outdoor monitored modules will be survey over 2017 to demonstrate that energy performance ratio higher than 91% can be achieved at least with the current Generation 2 but as well with corrected Generation 3.
This project made us able to show the potential of Si-HJT technology but also pointed out what are the key parameters to be improved to further increase its competitiveness.

Annex I Dissemination of results

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