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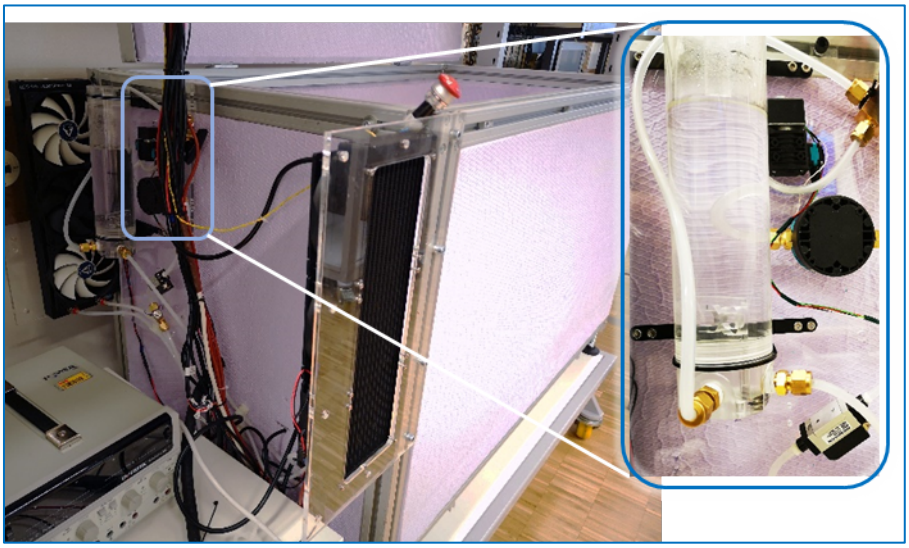
Measurement of intrinsic wide band gap device properties for power conversion

(MEPCO)



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Zusammenfassung

Dieses Projekt zielt darauf ab, neuartige Techniken und Verfahren zur Messung intrinsischer Bauelementeigenschaften zu entwickeln und die verschiedenen in der Leistungselektronik verwendeten Halbleitertechnologien wie GaN, SiC und Si zu vergleichen, um zu verstehen, wie diese Technologien für eine effiziente Leistungsumwandlung besser angewendet werden können. Die Informationen über die Verlustmechanismen kommerziell erhältlicher Bauelemente werden auch Möglichkeiten eröffnen, die Halbleiterdesigns zu verbessern.

Insbesondere haben wir zunächst die Ausgangskapazität von GaN-Geräten als kritische Verlustquelle im Hochfrequenzbetrieb identifiziert und fortschrittliche Messmethoden untersucht, um das Verlustniveau genau zu bestimmen. Es werden neue energieorientierte Methoden und Messmethoden auf Waferebene vorgeschlagen, um die Verluste im Zusammenhang mit der Ausgangskapazität zu charakterisieren. Die Messung, Analyse und Modellierung von Ausgangskapazitätsverlusten liefert Einblicke in das Geräteverhalten und das Verständnis der Ursprünge dieser Verluste.

Um den Vergleich verschiedener Wide-Band-Gap-Leistungshalbleitertechnologien zu erleichtern, haben wir eine umfassende Verlustanalyse für den Soft-Switching-Betrieb von Wide-Band-Gap-Transistoren demonstriert. Dazu gehören Verluste im Zusammenhang mit der Leitung und der dynamischen Widerstandsverschlechterung im EIN-Zustand sowie das Laden/Entladen der Eingangskapazität und der Ausgangskapazität. Die Studie erleichtert die Bewertung von Systemverlusten und die Auswahl effizienter Leistungsgeräte auf der Grundlage der Kompromisse zwischen verschiedenen Verlustquellen bei hohen Frequenzen. Diese Analyse ist auch für Geräteingenieure aufschlussreich, um Hochleistungs-Leistungstransistoren für Hochfrequenzanwendungen zu entwerfen.

Schließlich haben wir ein neues kalorimetrisches Echtzeit-Messsystem entwickelt, um die Schaltverluste in Hochfrequenzwandlern genau zu bestimmen, wo elektrische Messungen eine Herausforderung darstellen.

Résumé

Ce projet vise à développer de nouvelles techniques et procédures pour mesurer les propriétés intrinsèques des dispositifs et comparer les différentes technologies de semi-conducteurs utilisées en électronique de puissance, telles que GaN, SiC et Si, afin de comprendre comment mieux appliquer ces technologies pour la conversion de puissance efficace. Les informations sur les mécanismes de perte des semi-conducteurs disponibles dans le commerce ouvriront également des opportunités pour améliorer les conceptions de semi-conducteurs.

En particulier, nous avons d'abord identifié la capacité de sortie des dispositifs GaN comme une source critique de pertes en fonctionnement à haute fréquence et étudié des méthodes de mesure avancées pour déterminer avec précision le niveau de pertes. Une nouvelle méthode orientée énergie et une méthode de mesure au niveau de la tranche sont proposées pour caractériser les pertes liées à la capacité de sortie. La mesure, l'analyse et la modélisation des pertes de capacité de sortie fournissent des informations sur le comportement du dispositif et sur la compréhension des origines de ces pertes.

Pour faciliter la comparaison de différentes technologies de semi-conducteurs de puissance à large bande interdite, nous avons présenté une analyse complète de la répartition des pertes pour le fonctionnement en commutation douce des transistors à large bande interdite. Cela inclut les pertes

liées à la conduction et à la dégradation dynamique de la résistance à l'état passant, ainsi que la charge/décharge de la capacité d'entrée et de la capacité de sortie. L'étude facilite l'évaluation des pertes du système et la sélection de dispositifs de puissance efficaces basés sur les compromis entre diverses sources de pertes à hautes fréquences. Cette analyse est également utile aux ingénieurs de dispositifs pour concevoir des transistors de puissance hautes performances pour les applications haute fréquence.

Enfin, nous avons développé un nouveau système de mesure calorimétrique en temps réel pour déterminer avec précision les pertes de commutation dans les convertisseurs haute fréquence, où les mesures électriques sont difficiles.

Summary

This project aims to develop novel techniques and procedures to measure intrinsic device properties and compare the different semiconductor technologies used in power electronics, such as GaN, SiC and Si, aiming to understand how to better apply these technologies for efficient power conversion. The information on the loss mechanisms of commercially available devices will also open opportunities to enhance the semiconductor designs.

In particular, we first identified the output capacitance of GaN devices as a critical source of losses at high frequency operation and investigated advanced measurement methods to accurately determined the losses level. New energy-oriented method and wafer-level measurement method are proposed to characterize the output capacitance related losses. The measurement, analysis and modelling of output capacitance losses provide insights on the device behaviour and on the understanding of the origins of these losses.

To facilitate the comparison of different wide-band-gap power semiconductor technologies, we demonstrated a comprehensive loss-breakdown analysis for soft-switching operation of wide-band-gap transistors. This includes losses related to conduction and dynamic ON-state resistance degradation, also charging/discharging of input capacitance and output capacitance. The study facilitates the evaluation of system losses and selection of efficient power devices based on the trade-offs between various sources of losses at high frequencies. This analysis is also insightful for device engineers to design high-performance power transistors for high-frequency applications.

Finally, we developed a new real-time calorimetric measurement system to precisely determine the switching losses in high frequency converters, where electrical measurements are challenging.

Main findings

- Output capacitance is a critical device feature affecting power device losses under high frequency soft switching operation.
- Epitaxial level investigation enables identifying the origin of output capacitance losses.
- At high frequencies, loss behaviour varies significantly between different WBG technologies. Precise measurements methods, such as calorimetric method, for various power electronics components are important.

Contents

1 Introduction

1.1 Background information and current situation

The purpose of this project is to develop techniques to measure the intrinsic device properties of wide-band gap devices. Throughout the project, we have advanced in our understanding of the properties and sources of potential energy losses in GaN devices. The techniques and results have been submitted to the most important journals in the field.

1.2 Purpose of the project

The outstanding electronic properties of wide band-gap materials, and in particular Gallium Nitride (GaN) semiconductors, such as large breakdown voltage, high critical electric field, high electron mobility and saturation velocity, high frequency switching, high temperature operation, make them an ideal material for power switches and converters. These properties are already enabling several applications for energy efficiency, such as drivers for LED light bulbs, inverters for photovoltaic panels, embedded power converters for computers and data centers, drivers for electric and hybrid automobiles, trains, ships, etc.

However, the current performance of these devices is not completely understood, and the predicted efficiency by simulations don't match the observed experimental results. The measurements of their properties is not trivial due to the high switching frequency allowed by these devices. This hinders the full use of this technology in energy-efficiency applications. The focus of our laboratory, the POWERlab, is to develop new technologies for GaN-based power electronic devices (such as transistors and diodes) that outperform the state-of-the-art leading to much more efficient power systems. Our laboratory has demonstrated in several occasions new approaches based on a nanoscale design of power devices that resulted in high voltage devices, operating at high frequencies and high temperature, with several orders of magnitude lower leakage current (hence, dissipation losses) as well as much lower switching losses. The purpose of this project is to develop techniques to measure the intrinsic device properties of wide-band gap devices. This will allow the correct design of converters at high frequencies due to a precise knowledge of the intrinsic properties, such as output capacitances (Coss). In addition, this project will compare the effect of several device properties, such as the effect of voltage rise times on a circuit level, to understand their consequence under realistic operation conditions. Finally, we will demonstrate a new real-time calorimetric measurement system to precisely determine the switching losses in high frequency converters. These topics will result in a much deeper understanding of these new technologies for power electronics, as well as how to best utilize their superior properties.

1.3 Objectives

This project aims to address all these challenges by developing new measurement methods that will allow to accurately determine these intrinsic properties and compare them to other semiconductor technologies. In particular, this project has three main goals:

A. Analysis, measurement and evaluation of losses in GaN power devices.

B. Semiconductor technology comparison for soft-switching losses.

C. Novel real-time calorimetric method for precise circuit-level evaluation of efficiency.

2 Results and discussion

2.1 Analysis, measurement and evaluation of losses in GaN power devices.

With our research efforts we have found that the device *Output Capacitance* (C_o) is one of the key device characteristics that is entangled with the switching losses in power. It affects both hard-switching (at relatively lower switching frequencies, such as 100 kHz) and soft-switching (at higher switching frequencies, usually above 5-10 MHz) topologies. We have demonstrated the use of the Sawyer-Tower measurement technique as a powerful method to analyse the behaviour of C_o, especially for soft-switching circuits [A1]. Based on this method, we carried out a full investigation of C_o losses of Field-Effect Transistors, which is explained next [A2]. In addition, we propose a pure energy-oriented measurement technique that directly captures the energy dissipated in the output capacitance, without any pre-assumption about the device circuit model. Applying this method to two type of GaN power devices (enhancement-mode and cascode) provides new insights on the frequency-dependence of such losses and their correlation to the dynamic ON resistance degradation. Finally we propose a wafer-level measurement technique to evaluation of C_{OSS}-related losses in power epitaxies, prior to the device fabrication. Our work sets the stage to optimize power epitaxies before scaling up and packaging and paves the way towards next generation of ultra-efficient power devices.

2.1.1 Investigation of Output Capacitance Hysteresis Losses of Field-Effect Transistors

Resonant-type power converters are an attractive solution to achieving large power densities at high frequencies due to their soft-switching behaviour [A3], [A4]. Their applications include, among others, computer power supplies [A5], radio-frequency (RF) power amplifiers in communication systems [A6], [A7], and wireless power transfer systems [A8]. During a single switching cycle in these converters, the output capacitance, C_o, of the switching device is charged and discharged in a resonant manner dictated by the specificities of the topology, as means of achieving soft-switching conditions [1]. Since the device is in OFF state during the charging–discharging process of C_o, this ideally yields zero losses [A1], [A4].

However, it has been reported in recent research that, transition losses still exist due to dynamic charging and discharging of the power device's output capacitance under soft-switching conditions [A4], [A9]. The corresponding energy loss is attributed to a hysteresis loss [A1], which is observed in large-signal charge versus voltage (QV) curves. Numerous works have reported such losses pertaining to different device structures: in Si Super- Junction (Si-SJ) transistors [A10]; and wide-band- gap (WBG) SiC transistors [A11], and GaN high-electron- mobility transistors (HEMTs) [A1], [A4], [A11]. The hysteresis energy loss in C_o is a function of the maximum (or peak) voltage, V_m, across the device's drain– source terminals, and is expressed as,

$$E_{\text{diss}} = \int_0^{Q_1} v_{\text{ds}} dQ - \int_{Q_1}^0 v_{\text{ds}} dQ$$

This energy loss adds an extra constraint on deciding the maximum voltage across a switching device for a given high- or very-high-frequency (HF or VHF) application. This is especially important in resonant converters where the device voltage stress could be quite high [A7]. Prior knowledge on the dependence of hysteresis energy losses with V_m, for the available devices, would allow to select the most suitable operational voltage range for the circuit.

In this research work, four prominent field-effect transistor (FET) technologies were examined to observe their *QV* patterns. The study concerned soft-switching losses in the frequency range of 10 kHz to 1 MHz. The test circuit (see Figure A1) operates such that the excitation voltage across the device drain–source terminals is of sinusoidal nature, while the gate–source terminals are shorted, i.e., v_{GS} = 0 V. High-voltage Si, Si-SJ, SiC and GaN devices are tested up to a V_m of 400 V. To make a comparative study, twelve FETs are selected such that they have a current rating around 30 A. The part numbers, device technologies and other important details from the datasheets of the selected FETs are tabulated in Table A1.

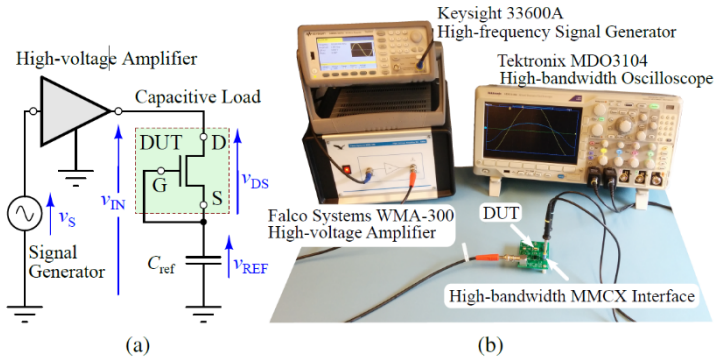

Fig. A2 (a) Schematic and (b) the experimental test setup of the Sawyer-Tower measurement technique used to analyse large-signal output capacitance.

DEVICES EVALUATED IN THE STUDY

Index	Technology	Voltage (V)	Part Number	Manufacturer	Current Rating (A) @ T_C = 25 °C	$R_{DS(on)}$ (mΩ) typical	Package
Si-1	Si (planar)	500	SiHG32N50D	Vishay Siliconix	30	125	TO-247
Si-2	Si-SJ	650	NTHL110N65S3F	ON Semiconductor	30	98	TO-247
Si-3	Si-SJ	650	IPW65R110CFD	Infineon	31	99	TO-247
Si-4	Si-SJ	650	STW38N65M5	STMicroelectronics	30	73	TO-247
SiC-1	SiC	700	MSC090SMA070S	Microsemi	25	90	D3PAK
SiC-2	SiC	650	SCT3080AL	ROHM Semiconductor	30	80	TO-247
SiC-3	SiC	900	C3M0065090D	Cree	36	65	TO-247
SiC-4	SiC (cascode)	650	UF3C065080K3S	UnitedSiC	31	80	TO-247
GaN-1	GaN	650	GS66508T	GaN Systems	30	50	GaN*PX*
GaN-2	GaN	600	IGOT60R070D1	Infineon	31	55	PG-DSO-20-87
GaN-3	GaN	600	PGA26E07BA	Panasonic	31	56	DFN 8X8
GaN-4	GaN (cascode)	650	TPH3212PS	Transphorm	27	72	TO-220

Table. A1 Evaluated Devices

Figure A2 shows that the DUTs exhibit diverse *QV* patterns, even within the same semiconductor types. In the Si family, the planar-Si structure shows negligible hysteresis while the SJ counterparts exhibit significant hysteresis with E_{diss} values greater than 1 μJ. The SJ devices show a distinct knee-type behaviour in their discharging paths (indicated by a green circle), around where the region corresponding to E_{diss} is much larger, while the respective charging paths show much smoother transitions. The hysteretic area ceases around 200 V, beyond which the two paths coincide. SJ devices show much larger Q_o values (250 nC), while other devices—with comparable or lower values of on-state resistance, $R_{DS(on)}$— show much lower Q_o values (100 nC) at 400 V.

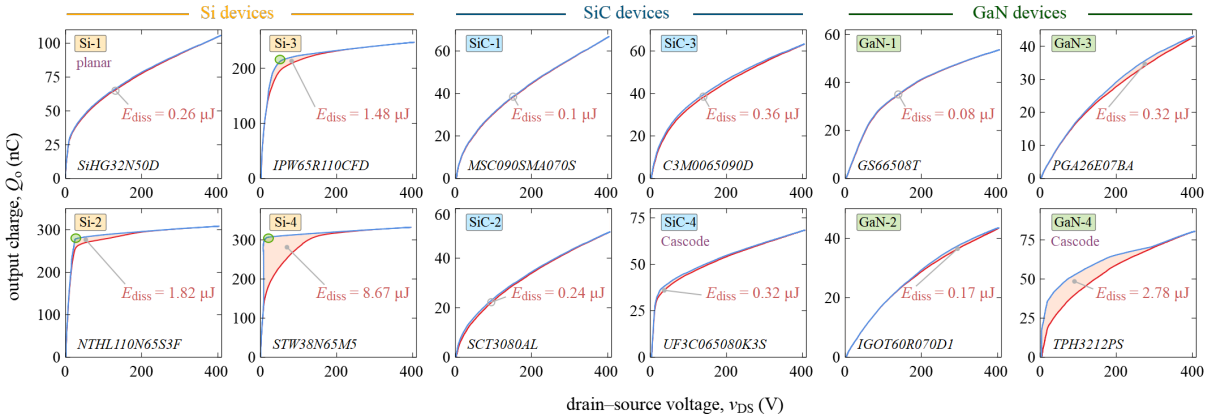

Fig. A2 Experimental QV (Q_o versus v_{DS}) curves of twelve different high-voltage transistors (current rating around 30 A): planar-Si device Si-1, Si-SJ devices Si-2 to Si-4, SiC devices SiC-1 to SiC-4 and GaN devices GaN-1 to GaN-4. The details of the devices are listed in Table A1. The solid red and blue lines correspond to charging and discharging paths, respectively; the hysteresis energy loss E_{diss} is indicated by the area between the two curves (shaded in orange).

The WBG devices SiC-1 and GaN-1 hardly show any hysteresis. The barely visible area between the charge–discharge curves of these two devices and the devices Si-1 and SiC-3, is symmetrically distributed within the whole v_{DS} range (i.e., the widening in the hysteretic area is symmetrical about $V_m/2$). An interesting observation is that the patterns of the cascode structures of the WBG devices (SiC-4 and GaN-4) deviate from their non-cascode counterparts, showing the knee-type behaviour characteristic of SJ structures. Furthermore, the cascode GaN device shows significant hysteresis compared to other GaN devices.

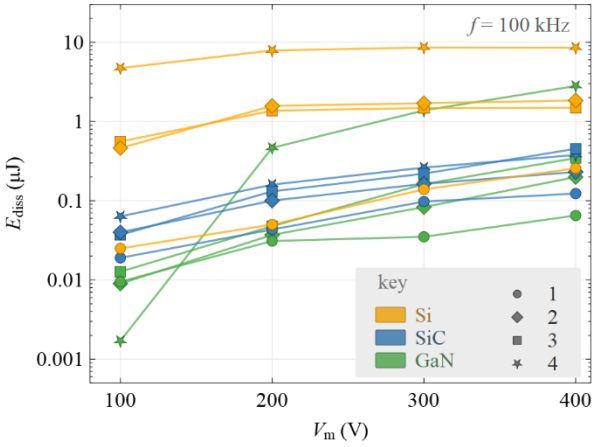

Fig. A3 Variation of E_{diss} with different V_m values for the twelve tested devices. V_m is varied between 100 and 400 V at 100 V steps.

Figure A3 compares the variation E_{diss} with V_m for all the devices, while the excitation frequency is kept fixed at 100 kHz. A clear observation is that the Si-SJ devices show a saturation of their E_{diss} values as V_m passes 200 V. The devices Si-1, SiC-1 and GaN-1, as expected from their 400-V results (in Figure A2), exhibit no appreciable hysteresis even at low voltages. Figure A3 also indicates that these devices show, although lower in value, an increasing E_{diss} with V_m.

The investigations presented so far concerned the soft-switching loss behaviour in the low-frequency range (below 1 MHz). In the next section, we present a method to qualitatively predict the soft-switching losses in the high-frequency range, based on a small-signal measurement approach.

2.1.2 Prediction of High-Frequency Soft-Switching Losses by Defining an Output-Capacitance Loss Tangent

The dissipated energy (E_{diss}) related to the resonant charging/discharging of a transistor output capacitance, becomes a dominant loss factor for power converters operating in the MHz range. A recent work has introduced a small-signal measurement method to quantify E_{diss} with a frequency-dependent small-signal resistance, R_s, and an effective *small-signal* output capacitance, C_{oss}^{eff} [A13]. Our new investigations provide further insights on the effect of R_s and C_{oss} upon the device losses in a broader sense (see Figure A4).

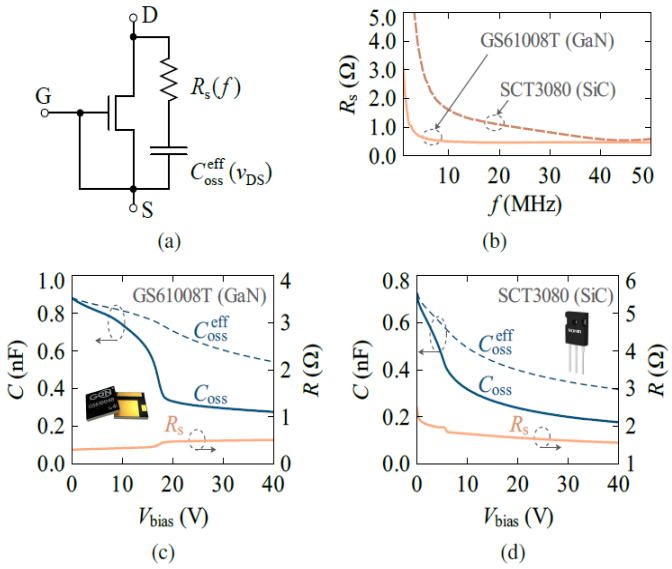

Fig. A4 (a) The small-signal model for output capacitance. (b) The frequency dependence of R_s for a 100-V GaN device and a 650-V SiC device, where (c) and (d) show the variation of C_{oss}, C_{oss}^{eff} and R_s with bias voltage for the same devices. A Keysight E4990A impedance analyzer with a 16047E test fixture (50 MHz) was used with an excitation signal of f = 10 MHz at a peak of 100 mV. The gate and source terminals of the transistors were shorted, i.e. v_{GS} = 0 V ($C_{oss} = C_{GD} + C_{DS}$).

To encompass the C_{oss} and the R_s information of a device, the concept of C_{oss} loss tangent, tan (δ), is introduced as a unified selection and benchmarking criterion; where R_s and the capacitive reactance, $X_c = 1/(j\omega C_{oss}^{eff})$, respectively, represent the real and imaginary parts of a complex impedance with an angle δ. The frequency of operation is $\omega=2\pi f$. The loss tangent normalizes E_{diss} with respect to E_{oss} (stored energy in C_{oss} for a given drain-source voltage), enabling comparison of device families solely based on their loss tangent values, regardless of on-state resistance ($R_{DS(on)}$) variations in devices within a family.

Benchmarking of devices based on the proposed concept provides important information for the circuit designer to choose the best device that minimizes the overall losses. Moreover, the presented results can be insightful for the device designer to improve the high-frequency behaviour of their devices. The details of our method and the experimental results are summarised as follows.

In our analysis, first the behaviour of R_s within commercial devices for five high-voltage device families A to E (tabulated in Table A2) is analysed. Figure A5 plots R_s versus $R_{DS(on)}$ for the considered device families. All families generally show a linear relation between R_s and $R_{DS(on)}$. These results suggest that R_s is fundamentally related to the sizing of a device in a linear manner.

EVALUATED DEVICE FAMILIES

Family	Voltage	Technology	Manufacturer
A	500	Si (planar)	Vishay
B	650	GaN	GaN Systems
C	700	SiC	Microsemi
D	650	SiC	Rohm
E	650	SiC (Cascode)	United SiC

Table A2 Device families evaluated in the study.

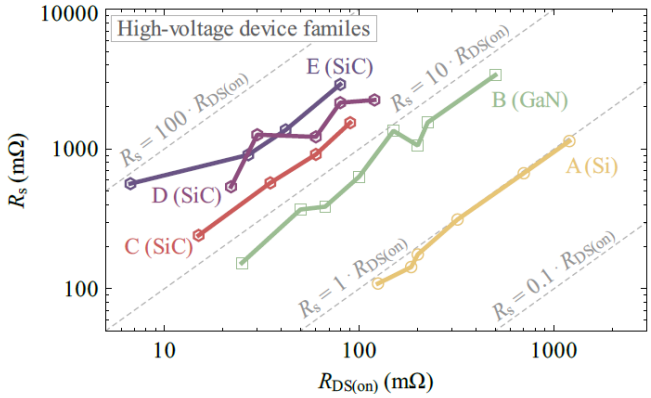

Fig. A5 Variation of R_s (at v_{DS} = 40 V and v_{GS} = 0 V) with $R_{DS(on)}$ for 500-700 V normally-off device families. The excitation signal has f = 10MHz and a peak of 100 mV.

Then, R_s can be incorporated to a loss tangent, defined by the following equation.

$$\tan(\delta) = \frac{R_s}{X_c} = \frac{R_s}{\omega C_{oss}^{eff}}$$

The dissipated energy E_{diss} can be expressed as follows, where k is a constant based on the excitation signal type:

$$E_{diss} = k f V_p^2 {C_{oss}^{eff}}^2 R_s$$

Therefore, a normalized E_{diss} can be expressed as,

$$\overline{E_{diss}} = \frac{E_{diss}}{\frac{1}{2} C_{oss}^{eff} V_p^2} = \frac{k}{\pi} \tan(\delta)$$

We arrive at the following important conclusions:

- tan(δ) normalizes E_{diss} and encompasses C_{oss}^{eff}, R_s and f in a single parameter for loss evaluation. In other words, tan(δ) is a measure of E_{diss} for a unit stored energy.
- tan (δ) is constant for a given family and is independent of current rating.
- Sizing up of a device increases (as C_{oss}^{eff} increases) the absolute E_{diss} within a device family.
- For different device families, the family with the lowest tan(δ) offers the lowest E_{diss} for a given stored energy (or equivalently for a given current capability).

The loss tangents and the related percentage losses (with respect to an effective stored energy ($\frac{1}{2}C_{\mathrm{oss}}^{\mathrm{eff}}V_{\mathrm{p}}^{2}$) with the excitation frequency (up to 50 MHz) are plotted in Figure A6(a) for different device structures: Si, SiC, and GaN power devices with similar current ratings on the high-voltage range (500-900 V) are considered. Note that, since R_s is a frequency-dependent parameter, as illustrated in the example-cases shown in Figure A4, the value of tan(δ) changes non-linearly with f. For frequencies below 15 MHz, the Si device (planar MOSFET) and two GaN devices show tan(δ) values well below 0.01, with less than 1 % of losses. However, above 15 MHz, GaN devices show the lowest tan(δ) values, keeping around 3 % of losses. The lower rate of increase of tan(δ) towards the large frequencies of the GaN devices is attributed to the general decrease of R_s with frequency. The significant increase of tan(δ) in the Si device up to 25 MHz, which leads up to 8 % of losses, is due to the large increase of its R_s in this frequency region. The SiC devices show negligible variation in their tan(δ) values between 5 to 30 MHz. This agrees well with the observations in [A14], where the measured E_{diss} for the tested SiC devices show little change within the considered frequency range. All the SiC devices generally show higher losses for the whole frequency range.

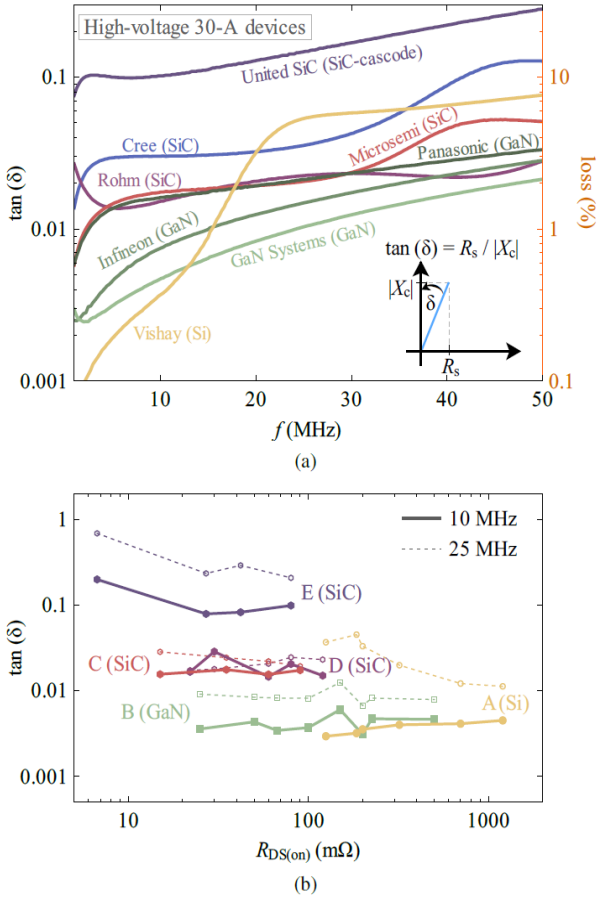

Fig. A6 (a) The variation of tan (δ) versus f for 30-A high-voltage (500-900 V) devices from different manufacturers. The percentage losses are also given with respect to their effective stored energies, where the factor k=π from is not considered. A sinusoidal excitation signal with a peak of 100 mV was employed. (b) The variation of tan(δ) with $R_{\mathrm{DS(on)}}$ for the device families A-E (tabulated in Table A2), measured at f = 10 MHz (solid lines) and f = 25 MHz (dotted lines), with $C_{\mathrm{oss}}^{\mathrm{eff}}$ values estimated at v_{DS} = 400 V.

Figure A6(b) plots tan(δ) value with $R_{DS(on)}$ for different devices within a family at 10 MHz (solid lines) and at 25 MHz (dotted lines): five different families from A to E were considered (see Table A2). For all the device families it is clearly observed that tan(δ) stays fairly constant for 10 MHz, irrespective of the value of $R_{DS(on)}$, hence with the device current rating. This is in agreement with our analysis, and is expected based on the linear behaviour observed between R_s and $R_{DS(on)}$ at 10 MHz in Figure A5. A similar trend can be seen at 25 MHz, except for the Si family that shows a deviated behaviour with much higher *tan*(δ) values at lower $R_{DS(on)}$ values. The families A (Si) and B (GaN) offer best performance at 10 MHz, with tan(δ) = 0.005; however, the GaN family B offers much lower $R_{DS(on)}$, allowing same level of soft-switching performance at much higher current ratings. The GaN device family outperforms all the families at 25 MHz with the lowest tan(δ).

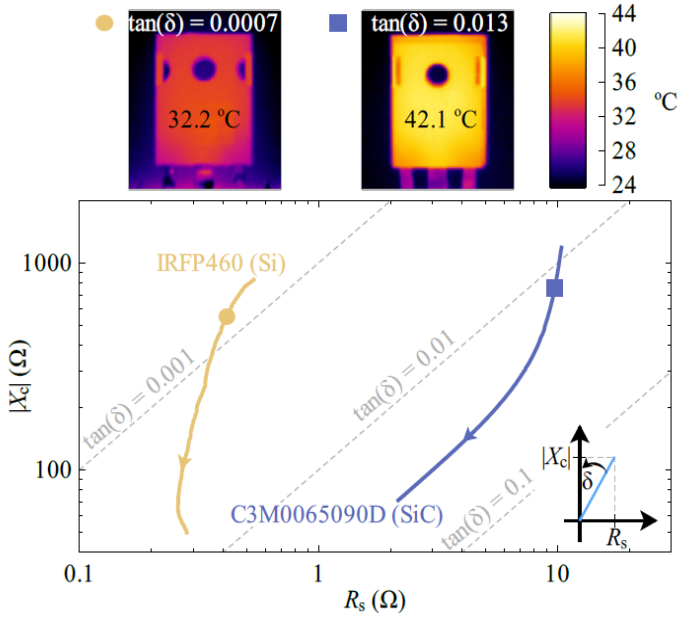

Fig. A7 Temperature rise of two devices that have approximately equal E_{oss} values at 400 V, but different tan(δ) values. The devices were excited using the Sawyer-Tower circuit with a v_{DS} swing of 400 V and f = 900 kHz. Note: the arrows in X_c curves show the direction of increasing frequency.

Since it can be assumed that $E_{oss} \propto C_{oss}^{eff}$, the device family with lowest tan(δ) should be selected as the preferred choice to minimize E_{diss} for a given E_{oss}. To corroborate this experimentally, two high-voltage Si and SiC devices were excited with the Sawyer-Tower circuit at a peak voltage of 400 V and a frequency of 900 kHz. The devices have similar E_{oss} values (around 10 µJ) and the same hardware-package (TO-247); also, similar environmental conditions were maintained during the test. Figure A7 shows the impedance-plane measurements of the two devices whose $|X_c|$ values lie in the same range, indicating that E_{oss} values are in close range. The steady-state thermal images of the two devices are also shown in Figure A7. The SiC device exhibits much higher power dissipation compared to the Si device. This is due to its much larger tan(δ) value (about 0.013) which is more than an order of magnitude larger compared to the Si device.

It should be noted that, the loss-tangent method is valid for frequency-dependent energy losses related to C_o, which can be characterized by the small-signal R_s. This is the case observed in most WBG devices

[A13]. For such devices, the large-signal C_o loss is solely determined by tan(δ). On the other hand, the frequency-independent energy losses [A13], which can be observed mostly in Si-SJ devices, should be estimated using large-signal measurement methods, like the Sawyer-Tower method [A1]. Since these losses are observed at much lower frequencies, such as 10-50 kHz [A1], at which the value of tan(δ) is negligible, the extracted frequency-independent loss is a good measure of the C_o losses. If such a device has a frequency-dependent energy loss component, then one can simply add the frequency-independent component to the losses predicted by tan(δ), to calculate the total loss. However, the frequency-dependent component becomes dominant, and surpasses the frequency-independent portion at larger frequencies.

In conclusion, by evaluating commercial device families, we demonstrated that tan (δ) is constant for a given family, independent of the device on-state resistance, $R_{DS(on)}$. It is shown that a minimum E_{diss} is achieved by having the lowest tan (δ) for a given stored energy (E_{oss}) in C_{oss}. With accompanying guidelines, this work identifies tan (δ) as a powerful figure of merit to classify field-effect transistors for soft-switching applications, regardless of $R_{DS(on)}$ variations in devices within a family. The proposed concept provides a comprehensive method to characterize and benchmark power transistors for high-frequency applications.

2.2 Pure energy-oriented method to capture C_{OSS} losses in nanosecond time scales: New insights to soft-switching losses in Cascode GaN transistors and the correlation to the $R_{DS(ON)}$ degradation

Due to the importance of characterizing the output capacitance losses in power transistors, historically in Si superjunction (SJ) MOSFETs and now in high switching frequency GaN FETs, different measurement methods have been proposed to capture C_{OSS}-related losses. On one side, electrical measurement and evaluation methods such as Sawyer Tower (ST) [A1], Nonlinear Resonance (developed in POWERlab [A15]), and Small-signal modelling (developed in POWERlab [A13], [A16]), indirectly extract the C_{OSS} loss. On the other side, calorimetric approaches more directly monitor the power losses in the devices, however, they require enormous number of measurements to fully characterize a device in different operation points.

We proposed, for the first-time, an electrical measurement method which directly captures the energy loss in C_{OSS} based on energy balance and without any post data processing. We extract the energies corresponding to charging and discharging of C_{OSS} as well as E_{DISS}, based on the current of a high quality factor inductor. This is a unique feature of this method and makes it an 'energy-oriented' technique. Even by looking at C_{OSS} as a black-box with an unknown circuit model, the method gives a valid value of dissipated energy. This is of extreme importance especially for devices with complex charging and discharging processes.

2.2.1 Methodology and the experimental scheme: Verification for a SJ transistor

The method works based on a resonance between C_{OSS} and a pre-calibrated inductor, where the initially stored energy of inductor L (Fig. A8a) is fully transfers to the C_{OSS} and comes back again to the inductor.

As shown in Fig. A8b both charging and discharging processes occurs in this resonance ($t_0 < t < t_1$), so the initial energy of inductor ($E_0 = 1/2\ LI_0^2$) equals the charging energy of C_{OSS} when it charges up to V_{max}, and the final energy of inductor ($E_1 = 1/2\ LI_1^2$) equals the discharging energy of C_{OSS}. Fig. A8c shows inductor energy over time for devices with and without C_{OSS}-losses. Although losses due to the high-Q inductor L is very small during the single-cycle resonance, this loss can be easily de-embedded, resulting in a very high-precision measurement. In this regard, $2\pi/Q$, where Q is the inductor quality factor, is the portion of energy dissipated in L, so the C_{OSS}-loss can be calculated as

$$E_{\mathrm{DISS}} = \left(1 - \frac{2\pi}{Q}\right) E_0 - E_1$$

The C_{OSS} charging and discharging can also be extracted from

$$E_{\mathrm{DISS}}^{\mathrm{ch}} = \left(1 - \frac{\pi}{Q}\right) E_0$$

and

$$E_{\mathrm{DISS}}^{\mathrm{disch}} = E_1 + \frac{\pi}{Q} E_0$$

respectively. A typical Q-factor larger than 100 leads to 2% or less change in E_{OSS}. A realization of the proposed circuit has been illustrated in Fig. A8d. A high precision series resistor is used to measure i_{L}.

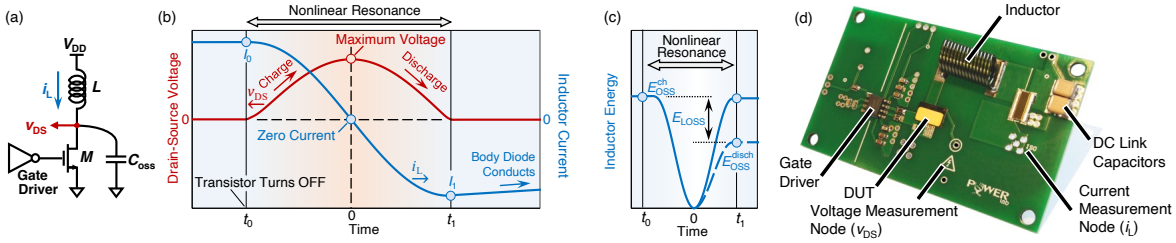

Figure A8. (a) Schematics of the proposed circuit. (b) Illustrations of v_{DS} and i_{L} waveforms showing a resonance between L and C_{OSS}. (c) Inductor energy for devices with (solid line) and without (dashed line) C_{OSS}-loss. (d) Realization of the proposed circuit.

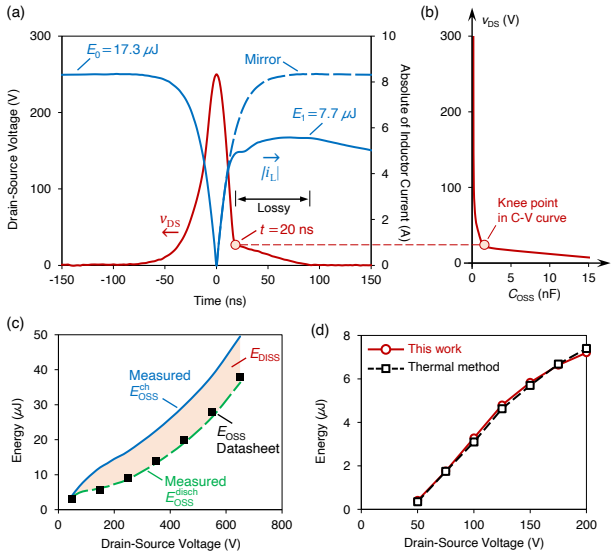

Figure A9. (a) Measurement results for a 650-V 60-A Si SJ MOSFET using L = 500 nH at maximum voltages 250 V. Lossy behavior of this device starts when it is getting out from full depletion regime. (b) C_{OSS}-V_{DS} curve reported in datasheet verifies the jump in COSS happens exactly at the voltage that the lossy behavior is started. (c) Extracted C_{OSS} charging/discharging energies and data reported in datasheet as well as the extracted COSS loss (E_{DISS}). (d) The estimated C_{OSS} loss from thermal measurement (dashed line) verifies the extracted E_{DISS} by the proposed method (sloid line).

We conducted experiments on transistors with different technologies to show the applicability of the proposed method. The measurements were carried out with a 1-GHz 5-GS/s digital oscilloscope. Voltage measurement with a 1-GHz differential-probe across a 200 mΩ series resistor was used to extract current of the inductor. The small energy loss in this small resistor is included into the inductor quality factor. The high bandwidth provided in these measurement enables capturing C_{OSS}-losses at very high frequencies.

To examine the accuracy of the method we first examined a super junction transistor with considerably large C_{OSS} losses and compared the extracted energy losses with those obtained by a thermal method. Measured results for a 650-V 60-A Si SJ MOSFET at V_{max} = 250 V are shown in Fig. A9. From the initial inductor energy of 17.3 µJ, only 7.7 µJ has been recovered, showing a lossy charging/discharging process. This method, not only extracts the C_{OSS}-losses, but also gives insights to device behavior and shows indications about origin of these losses. The mirror of current with respect to t = 0, shows a symmetry until t = 20 ns, where the inductor current is almost equal to that at t = −20 ns.

At t = 20 ns the slope of v_{DS} significantly changes, which corresponds to the jump in C_{OSS} (knee point in Fig. A9b), typical for SJ devices, showing that the depletion process is fully completed around this voltage. The lossy behavior starts immediately after t = 20 ns, when the device is getting out from depletion regime, showing that the energy corresponds to stranded charges has not been fully recovered. Fig. A9c shows extracted E_{OSS}^{ch} and E_{OSS}^{disch}, as well as the E_{OSS} reported in datasheet (corresponding to small-signal measurement). It appears that the smaller energy corresponds to the discharge of C_{OSS} has been reported in datasheet. The extracted C_{OSS} energy loss from this method were verified with a thermal measurement, where sinusoidal signals with different amplitudes from 25 V to 200 V was applied to the device in a ST circuit. The temperature rise was captured with a thermal camera. The measurements were calibrated with a DC test. Fig. A9d shows a good agreement between extracted energy loss with this method and the estimated energy loss with thermal measurement.

2.2.2 Evaluation on an enhancement-mode and a cascode GaN FET: A Correlation to $R_{DS(ON)}$ degradation

Figs. A10a and A10b, respectively show measured v_{DS} and i_L waveforms for a 650-V 30-A GaN HEMT. The extracted C_{OSS} energy dissipation, as well as R_{ON} degradation are shown in Fig. A10c. Dynamic $R_{DS(ON)}$ in GaN devices is susceptible to degradation right after a turn-ON transition. To measure this dependency, we used the pulsed-IV system (AMCAD), where the DUT was subjected to V_{GS} (using gate-probe iTest AM213) and VDS (using 1 kV/30 A drain-probe PIV AM241) excitations, with a 5-µs ON time and 15-µs OFF time. To capture the actual $R_{DS(ON)}$ and minimize the effect of noise, we averaged the resistance values over a 1-µs interval, after the settling time of the measurement tool was reached (2.5 µs after the device was turned ON). For the considered enhancement-mode GaN HEMT the R_{ON} degradation rises until 300-V and then it becomes smaller. Such effect has been previously observed [B25]. Interestingly, the percentage of C_{OSS}-losses also decreases at almost the same voltage, suggesting a possible relationship between these two effects. This indicates that buffer trapping is

possibly the physical mechanism behind frequency-independent C_{OSS} losses in enhancement-mode GaN HEMTs [A12].

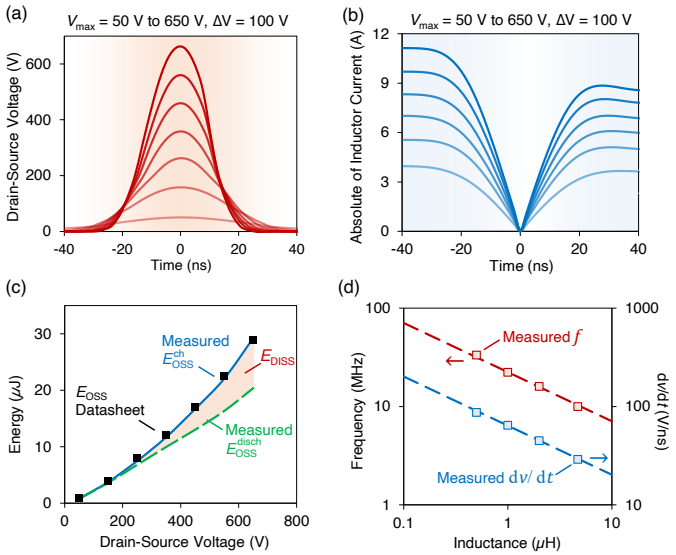

Figure A10. (a) Measured v_{DS} at three different voltage levels for an enhancement-mode GaN HEMT together with (b) current waveforms. (c) Extracted E_{DISS} and measured ON resistance degradation.

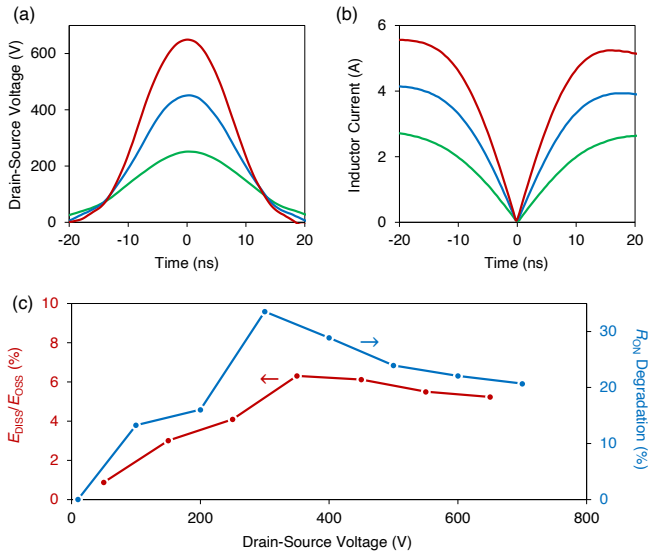

Figure A11. (a) Measured v_{DS} at different voltage levels V_{max} = 50 V, 150 V, 250 V, 350 V, 450 V, 550 V, and 650 V for a cascode GaN transistor together with (b) current waveforms. (c) Extracted C_{OSS} charging/discharging energies and data reported in datasheet as well as the extracted C_{OSS} loss (E_{DISS}). (d) Measured (discrete points) and modeled (dashed lines) frequency and dv/dt versus inductance L.

Then, using the new energy-oriented C_{OSS} loss measurement method we evaluated another technology of GaN FETs: the cascode devices. Figs. A11a and A11b, respectively show the measured v_{DS} and i_L of a Si/GaN cascode transistor. As shown in Fig. A11c, the device exhibits relatively low C_{OSS}-losses at low voltages (V_{DS} < 200 V), however, E_{DISS} becomes considerable at higher drain-source voltages. This indicates a different type of C_{OSS} losses in cascode GaN devices. The magnitude of losses is much larger than that of an e-mode device. Furthermore, C_{OSS} losses in cascode devices are strongly nonlinear with respect to the drain-source voltage. In addition to that, such losses show only a small

dependence on frequency. All these features indicate a different mechanism for C_{OSS} losses in cascode transistor, which requires further device-level studies.

Fig. A11d shows that by changing L, it is possible to cover a wide variety of different frequencies and dv/dt values. For instance, an inductance of 500-nH results in a very high frequency and dv/dt of 33 MHz and 87 V/ns, respectively. To obtain the same frequency with the ST method, a power amplifier with a high power delivery of ~4 kW at the same frequency is needed, while the proposed method just relies on an ordinary dc power supply. This is another important advantage of the energy-oriented measurement technique over the classic ST method.

2.3 Characterization of C_{OSS}-related soft-switching losses in epitaxial level: New insights on the buffer-related losses in GaN power devices

Precise evaluation and understanding mechanisms behind soft-switching losses in power devices is of great importance and has initiated extensive researches to propose and utilize measurement methods to examine packaged devices. Such evaluations after the whole process of device development, while being valuable, has two major issues:

1. Packaging by itself induces parasitics which makes it challenging to directly evaluate the active part of the device.

2. Optimization based on this approach is very costly as it relies on a long development process until the very final stage, in which the device can be examined in a circuits such as ST, nonlinear resonance, etc.

We present a precise on-wafer measurement technique (prior to the device fabrication, scaling-up, packaging, etc.) to evaluate C_{OSS} losses due to the epitaxial structure. This method uses a small-signal modeling approach to evaluate large-signal C_{OSS} losses [A13], [A16], which quantifies frequency-dependent energy dissipation in the C_{OSS} [A2]. The extremely low parasitics provided by this method enables the measurement of C_{OSS}-related losses at very high frequencies >100 MHz. This provides a general characterization method of epitaxial structures, enabling their optimization prior to the transistor fabrication. This new technique revealed unexpected resonant lossy-peaks in GaN-on-Si epitaxies, which were identified to be mainly due to the Silicon substrate.

2.3.1 Methodology: Radiofrequency techniques for power devices

The output capacitance of a power HEMT mainly consists of three parts: gate-drain capacitance (C_{GD}), drain-substrate capacitance through the vertical epitaxial structure (C_{epi}), and drain-source capacitance through the two-dimensional electron gas (2DEG) (C_{lat}). In power (MOS)HEMTs, C_{GD} is significantly smaller than the two other terms, so that one can consider $C_{OSS} = C_{epi} + C_{lat}$ (Fig. A12a). By applying drain-source voltage in the OFF-state, the 2DEG under the gate is depleted, resulting in a considerable reduction in C_{lat} and C_{OSS}. At high enough drain-source voltages, C_{OSS} becomes constant, approximately equal to C_{epi} (Fig. A12b) [A17], [A18]. C_{epi} has been presented as the significant part of C_{OSS} and also the main source of C_{OSS} losses in power HEMTs [A18]. This is a vertical capacitance sandwiched between drain pad and silicon substrate, so the capacitance mainly depends on the area of the drain pad, independent from the device layout. Although the characterization of high-frequency losses of RF

epitaxies has been proposed in the literature [A19], there is little knowledge on high-frequency losses of power epitaxies.

Here we present a wafer-level measurement method based on a simple proposed test structure (Fig. A13a) including a signal and ground pads to extract losses due to the epitaxial structure, which is the main source of C_{OSS} losses. The signal pad dimensions should be considerably larger than thickness of the insulating epitaxy so that the effect of fringing fields can be neglected. The RF signal pad is surrounded by a considerably larger ground pad. The ground pad forms a giant capacitance (C_∞) with the substrate, which grounds the doped silicon

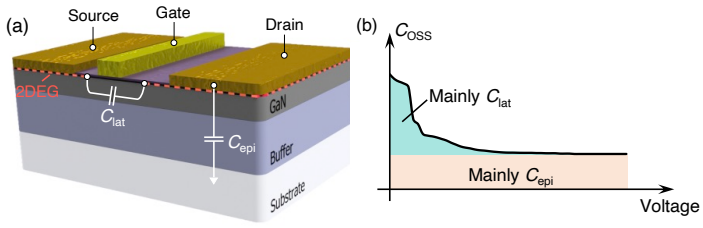

Figure A12. (a) Simplified structure of an AlGaN/GaN HEMT showing its output capacitance $C_{OSS} = C_{GD} + C_{epi} + C_{lat}$. In practice the effect of $C_{GD} \ll C_{OSS}$ is negligible. (b) C_{OSS} versus V_{DS} curve for a commercial device showing that C_{epi} dominates at high drain-source voltages.

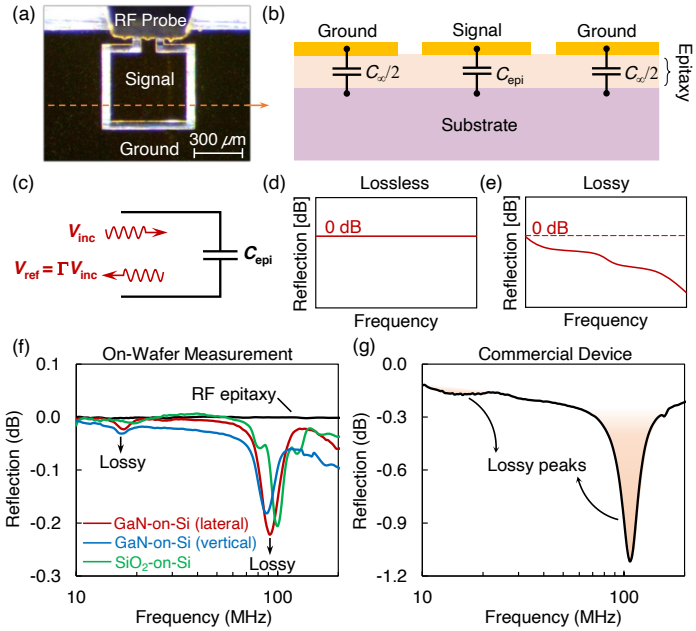

Figure A13. (a) Optical image of the test structure measured with an RF probe. (b) Cross-section illustration of the proposed test structure. (c) Measurement method to extract losses from output capacitance to characterize epitaxial structures. Illustration of reflection coefficient for (d) lossless, and (e) lossy epitaxies. (f) Measurement results for an RF epitaxy (GaN-on-SiC), together with two GaN-on-Si power epitaxies (corresponding to a lateral HEMT and a vertical MOSFET), as well as a SiO2-on-Si test structure. (g) Measurement results for a 600-V-rated commercial device showing similar lossy peaks.

substrate at radio frequencies (Fig. A12b). The test structure shown is examined with an incident wave with amplitude V_{inc}, and the reflection coefficient $\Gamma = V_{ref}/V_{inc}$, in which V_{ref} is the reflected wave

amplitude, is measured by a network analyzer (Fig. A13c). A frequency sweep of V_{inc} gives full information on the behavior of the device under test (DUT), including its circuit model and losses. A lossless C_{epi} results in the total reflection of the incident wave, thus Γ is equal to 0 dB (Fig. A13d). Whereas a lossy C_{epi} results in a partial reflection of the incident wave, thus in negative values of Γ (Fig. A13e).

One can extract the impedance of the DUT using

$$Z = Z_0(1+\Gamma)/(1-\Gamma)$$

where Z0 = 50 Ω is the measurement port characteristic impedance. The quality factor Q of the capacitor is obtained as

$$Q = \mathrm{Im}(Z)/\mathrm{Re}(Z)$$

where Im(Z) and Re(Z) represent the imaginary and real parts of Z, respectively. For a capacitive element, the amount of charging/discharging losses (between 0 to V) is inversely proportional to its Q, as

$$E_{diss} = \frac{\pi}{2Q}E_{tot}$$

where $E_{tot} = ½CV^2$ is the total energy stored in the capacitor when charged to the voltage V. Thus $\pi/(2Q)$ represents the percentage of energy losses.

Fig. A13a shows the fabricated experimental structure. The size of the signal and ground pads are 0.24 mm2 and 3.7 mm2, respectively, and the thickness of the pads is 300-nm (270-nm gold with 30-nm titanium adhesion layer). A ground-signal-ground (GSG) RF probe connected to a network analyzer (Keysight N5225A) was used to measure the reflection coefficient at different frequencies, with the lowest possible parasitics and an extremely high bandwidth of 50 GHz. Fig. A13f shows the measured reflection coefficient from test structures fabricated on four different epitaxies: GaN-on-SiC RF epitaxy, GaN-on-Si power epitaxies for lateral HEMTs and vertical MOSFETs, and a test SiO2-on-Si wafer. In all cases, we fabricated devices on 2 cm × 1.8 cm chips diced from 6-inch wafers. All samples on Si substrates (p-type with a resistivity of ~ 0.02 Ω·cm) exhibited considerably higher losses with respect to the reference RF epitaxy, with two pronounced peaks at ~17 MHz and ~90 MHz. The presence of lossy peaks (especially the larger one at higher frequency) for the SiO2-on-Si sample (with no GaN layer) suggests that the Si substrate is a potential origin of C_{OSS} losses in GaN-on-Si HEMTs. We also observed very similar lossy peaks in some commercial GaN-on-Si power HEMTs (Fig. A13g). In this case – in an off-chip measurement – we measured the reflection coefficient from drain-source of the commercial transistor, while the gate was shorted to the source. The vertical GaN-on-Si epitaxy also presented similar lossy peaks. In this case, the drift layer is lightly doped which results in a leakage current between the signal and the ground pads. This causes a lossy behavior over all frequencies and so a lower Q factor. This effect can be seen in Fig. A13f, where the vertical epitaxy (blue) shows higher background losses. Therefore, the proposed method reveals all sorts of power dissipations including resonant and leakage losses.

2.3.2 Experimental evaluation of lateral and vertical epitaxies

We used the proposed method to quantify the amount of output capacitance losses due to these resonances for epitaxies with different buffer thicknesses. Using (1) and (3), we extracted the capacitance as well as the losses related to C_{epi}, for two GaN-on-Si power epitaxies 4-µm (Fig. A14a) and 5-µm (Fig. A14b) buffer thicknesses (similar to the lateral GaN-on-Si epitaxy shown in Fig. A13f). There are two distinct peaks corresponding to losses for both epitaxies. Exactly at these peaks, abrupt changes in capacitance are observed, which shows a resonance happening in the epitaxial structure. Although the second epitaxy is 25% thicker than the first one, the resonance frequencies are very close,

showing a material dependency of such resonances. As expected, the thicker buffer has a lower capacitance and so a lower stored energy while the dominant part of losses due to the substrate is about the same. This results in a higher relative losses for the thicker epitaxy.

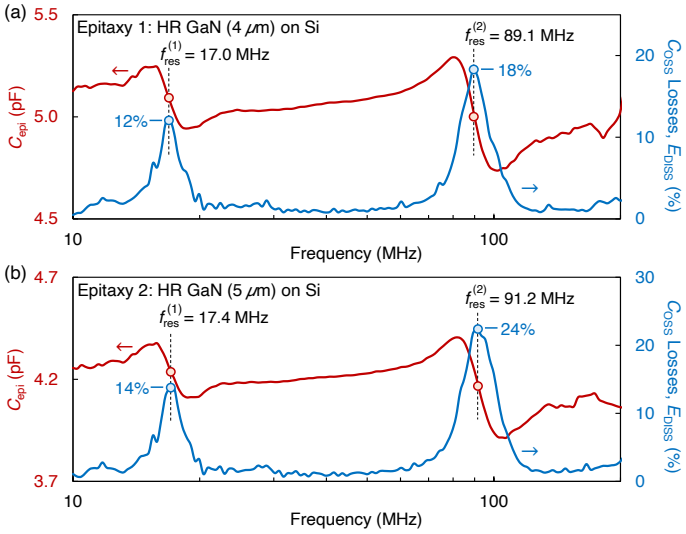

Figure A14. Extracted capacitance and losses of the test capacitor on (a) 4-µm-thick, and (b) 5-µm-thick carbon-doped high-resistive (HR) GaN buffers. In both cases, there are lossy resonances at ~17 MHz, and ~90 MHz.

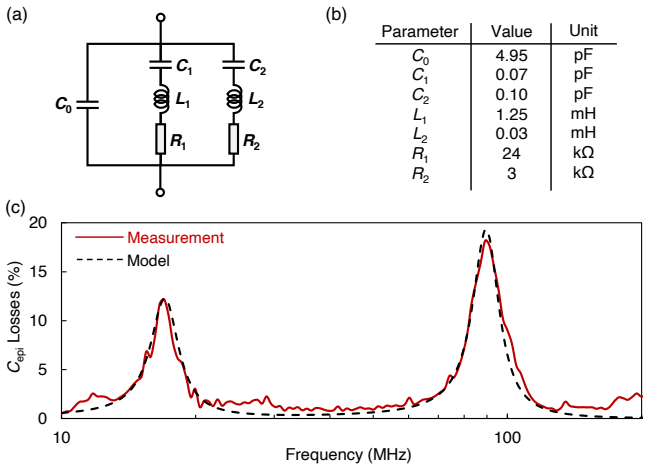

Fig. A15. (a) Proposed circuit model for output capacitance losses, together with (b) circuit parameters of the 4-µm-thick buffer sample. (c) Measured (solid line) and modeled (dashed line) C_{epi} losses.

Fig. A14 shows the importance of characterizing C_{OSS} losses at high frequencies, since a low frequency test, for instance up to 10 MHz, would not show such significant frequency-dependent losses happening at high frequencies. This could be a potential reason of higher measured losses with pulse excitation (containing higher harmonics) in comparison to sine-wave in ST method [A4], [A18]. For instance, at 10-MHz, the employed pulse waveform in [A4] had a 5-ns rise-time, and the C_{OSS} losses corresponding to this waveform was not limited to the fundamental frequency of 10-MHz, but it included all the frequency content of the pulse, exceeding 100-MHz. This also shows that single-tone ST measurements,

previously performed up to 35 MHz [A4], should be performed at much higher frequencies to cover the typical switching harmonics of wide-band-gap transistors [A20], [A21]. In addition, Fig. A14 shows a 1-2% loss over a wide frequency range, which indicates the ability of the proposed method in capturing background C_{epi} losses, caused by other phenomena such as the resistivity of substrate.

A circuit model of the C_{epi} can be extracted from the results shown in Fig. A15. The model includes a lossless capacitor C_0 in parallel with two lossy RLC resonant branches (Fig. A15a). Fig. A15b shows the extracted circuit parameters for the 4-µm-thick buffer. Fig. A15c presents the measured and modelled C_{epi} power dissipation, showing a good agreement between them. We employed the model presented in Fig. A14a in a circuit-level simulation with LTspice to extract the amount of C_{OSS} losses due to these resonances for different switching times. Fig. A15a shows the power dissipated in R_1 and R_2 (Fig. A14a) representing the low-frequency and high-frequency resonances. The switching time and voltage are 2-ns and 400-V, respectively. The results for 5-ns switching at the same switching voltage level are shown in Fig. A15b. As expected, the high-frequency resonance leads to much higher losses for the faster switching transient. The low-frequency resonance, however, is considerably slower than the typical switching transient of a GaN transistor, so both switching times of 2-ns and 5-ns lead to an almost equal power loss. It should be noted that the power loss continues happening after the switching transient is finished. For example for low-frequency resonance, there is a considerable power loss even 100-ns after the switching transient. This cannot be observed in the previous simplified models of output capacitance losses [A22], since they do not show any resonances. Fig. A15c shows the C_{OSS}-related energy

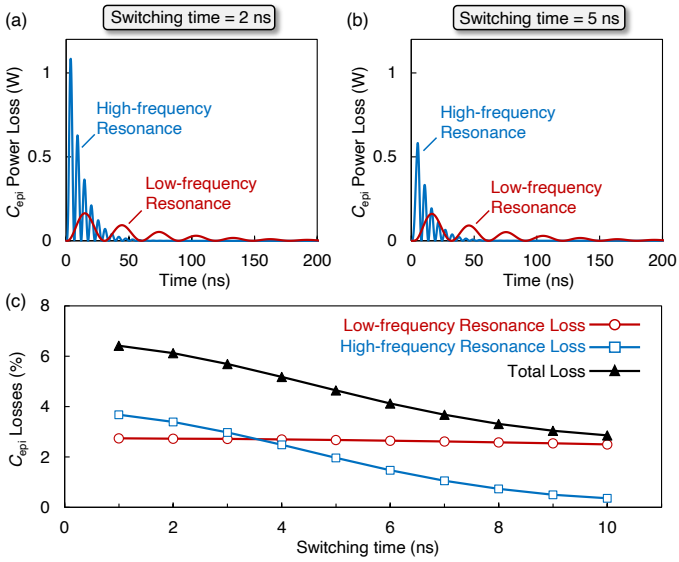

Figure A16. Simulated C_{OSS} power losses of the 4-µm-thick buffer sample for 400-V (a) 2-ns, and (b) 5-ns switching transients. The plots show separately the power loss representative for the low- and high-frequencies resonates. (c) Extracted C_{OSS} energy dissipation corresponding to the low- and high-frequencies resonates, as well as the total loss.

dissipation versus switching time for 400-V switching, from 1 to 10 ns, as well as the share of each resonance in the total loss. For fast switching transients, about 6% of the stored energy is dissipated during charging and discharging. This number is higher for the 5-µm-thick buffer and can reach to about 8% of the stored energy, showing that C_{OSS} losses can be potentially more severe for devices with a higher blocking voltage capability.

2.4 WBG Semiconductor Technology Comparison for Soft-Switching Losses

The reduced input capacitance (C_{ISS}) and ON Resistance ($R_{DS(ON)}$) in wide-band-gap (WBG) transistors enable their efficient operation at high frequencies [B1], [B2], for instance, high-power-density dc-dc conversion [B3]–[B6], wireless power transfer and radio-frequency amplification [B7], [B8]. At such frequencies, soft-switched topologies, especially those designed for zero-voltage switching (ZVS), can potentially achieve high efficiencies [B5], [B9]–[B11]. To that end, low levels of electromagnetic interference (EMI) and proper design of passive components, especially the magnetics, become crucial [B5], [B12], [B13]. Furthermore, conduction losses (P_{CON}), Output-capacitance (C_{OSS}) losses (P_O) and gate losses (P_G) reduce the system efficiency and expose the devices to thermal runaway [B1], [B14]–[B17]. Hence, it is important to adhere to accurate methods to extract these losses in different device technologies such as Gallium Nitride (GaN) and Silicon Carbide (SiC).

In this report, we demonstrate straightforward measurement methods to compare and break down soft-switching losses in various WBG technologies [B18], as illustrated in Fig. B1.

Commercial devices with similar current and voltage ratings (see TABLE B-I) are compared and their various losses are evaluated up to 40 MHz. In the following subsections, each source of losses is analysed in full details for the selected WBG technologies.

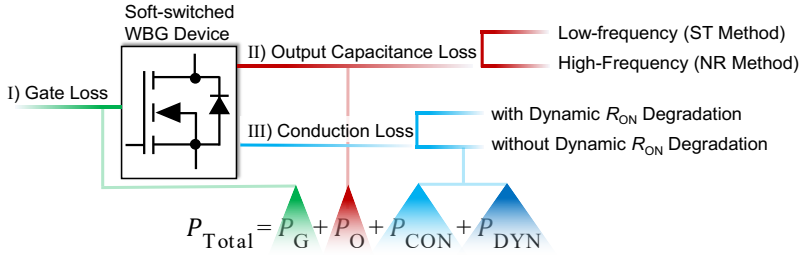

Figure B1 - Major sources of loss in a soft-switched WBG device. Various WBG technologies exhibit significantly different loss behaviors, that are comprehensively analyzed in [B18].

TABLE B-I

CHARACTERISTICS OF THE EVALUATED TRANSISTORS

ID	Part Number (Technology)	V_{BR} (V)	I_D (A)	Q_G (nC)	$R_{DS(ON)}$* (mΩ)	C_{OSS}** (pF)
T_1	GS66508T (p-GaN-gated)	650	30	5.8	50	65
T_2	PGA26E07BA (GaN GIT)	600	31	5	56	71
T_3	TP65H050WS (GaN Cascode)	650	36	16	50	130
T_4	SCT3060AL (SiC)	650	39	58	60	85
T_5	MSC060SMA070S (SiC)	700	37	56	60	138
T_6	UF3C065080K3S (SiC Cascode)	650	31	51	80	62

* Typical value at 25°C ** Reported at 400 V

2.4.1 Gate Loss

By modelling the gate as C_{ISS} in series with a gate resistance and a gate driver resistance, for push-pull gate drivers (i.e. hard gating), P_G is equal to the total energy used to charge C_{ISS} from V_{OFF} to V_{ON}, multiplied by f_{SW} as

$$P_G=Q_G(V_{ON}-V_{OFF})f_{SW} \qquad \text{(B1)}$$

where Q_G for soft-switched transistors can be formulated as

$$Q_G=\int_{V_{OFF}}^{V_{ON}} C_{ISS}(V)dV \qquad \text{(B2)}$$

C_{ISS} in (B2) is the small-signal capacitance measured versus voltage using an impedance analyzer, when the drain is shorted to the source, to emulate ZVS condition.

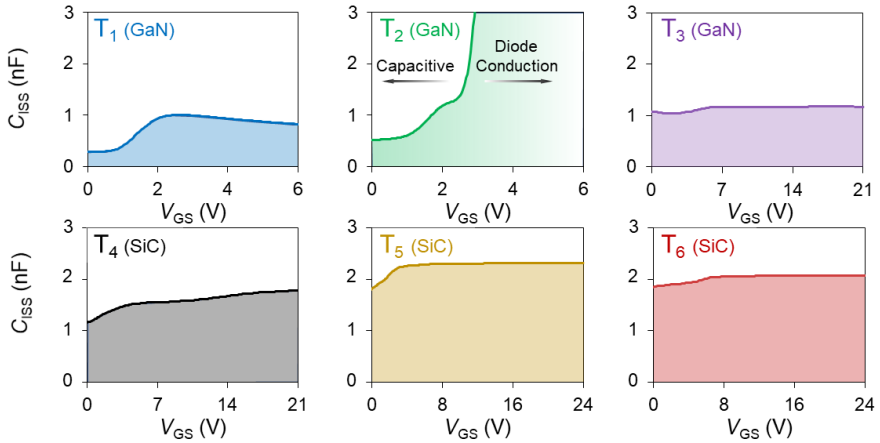

Figure B2 - Small-signal C_{ISS} versus V_{GS} for T_1 to T_6 measured at 1 MHz. The gate in most of the transistors can be regarded as an RC circuit. Device T_2 exhibits a capacitive behavior for low drive voltages and as the voltage increases, it performs similarly to a diode with an ON-state current, as indicated by the gradient shading under its C_{ISS}-versus-V_{GS} curve.

The results of C_{ISS} measurements using an E4990A impedance analyzer and a 16047E test fixture are shown in Fig. B2. Next step was to verify the evaluated losses based on small-signal measurements by real-circuit power measurements. As presented in Fig. B2a, time-domain V_{GS} was measured for all the transistors at 5 MHz, at their nominal drive conditions. An important difference between GaN and SiC devices is their performance at their input (i.e. gate) node. GaN devices can turn ON faster, and thus, enable much higher switching frequencies. Fig. B2b shows the measured power losses due to the gate drive operation over a wide range of frequencies. These experimental results verified the results of small-signal measurement, with an outstandingly-low mismatch error of less than 10%.

Standard methods used in datasheets to report gate-charge (Q_G) are based on hard-switching tests, and using those values for soft-switched transistors may result in large errors in high frequencies [B17]-[B20]. The proposed small-signal measurement reported in this work is highly recommended to be considered by WBG device manufacturers, enabling the precise design of power converters at high and very-high frequencies (HF and VHF).

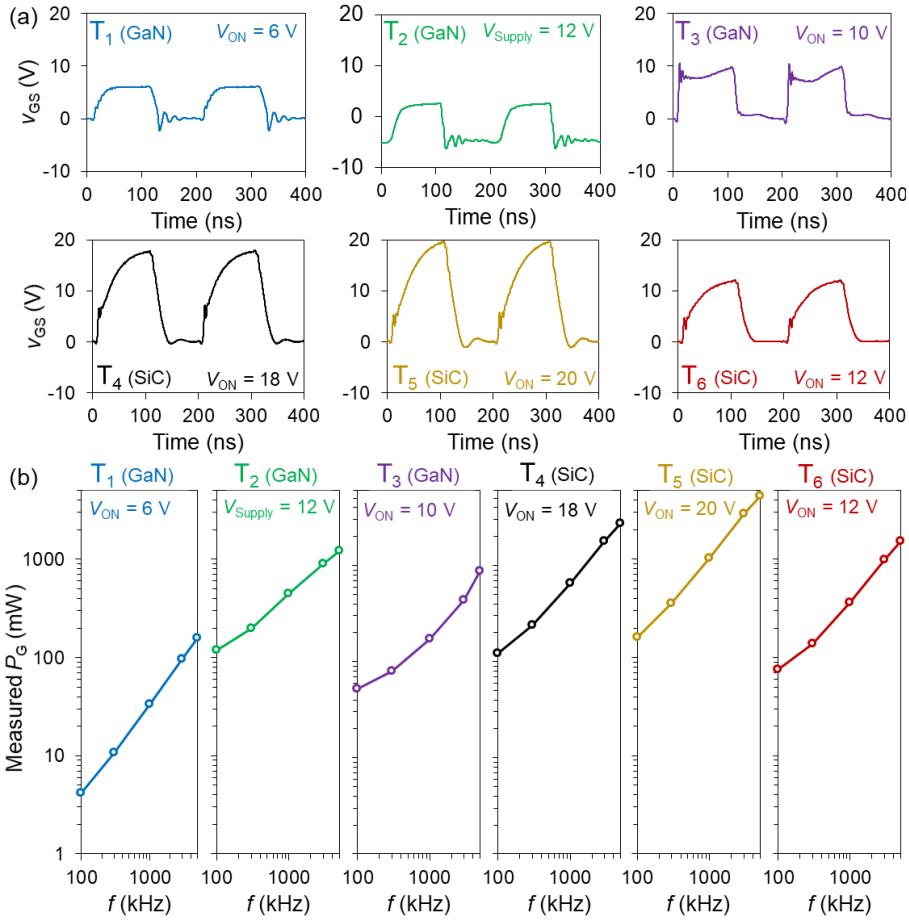

Figure B3 - (a) Time-domain gate-to-source voltages for T_1 to T_6, driven at 5 MHz with nominal gate conditions. (b) Measurement of real P_G versus f from 100 kHz to 5 MHz at nominal gate-driver conditions.

2.4.2 Output-Capacitance Loss

Charging and discharging of C_{OSS} could lead to excessive energy loss in WBG transistors [B14], [B21], [B22]. The overall large-signal C_{OSS} loss can be formulated as

$$P_O = fE_{DISS} \quad \text{(B3)}$$

where f is the switching frequency and E_{DISS} represents the energy dissipated in each charging/discharging cycle of the C_{OSS}. To measure E_{DISS} over a wide frequency range, we employed a combination of ST and NR methods [B16], [B23].

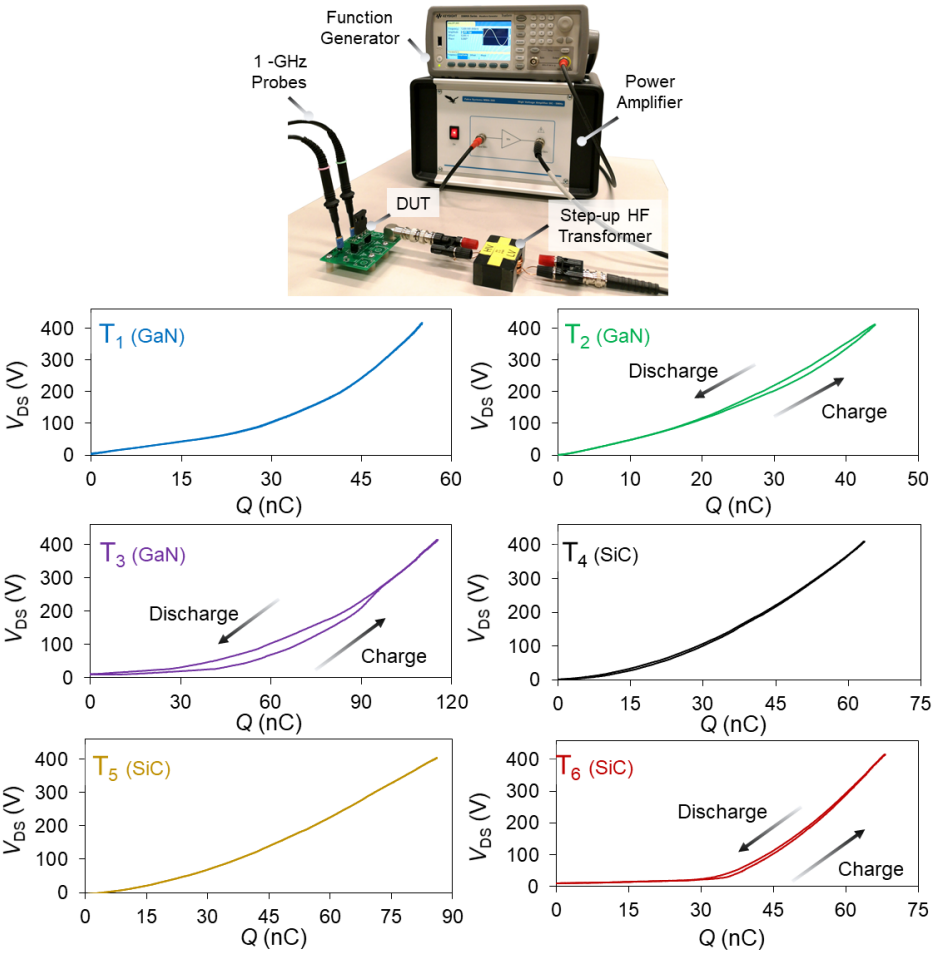

Figure B4 - Evaluation of large-signal C_{OSS} losses using ST method. Test setup for ST experiment comprised of a DUT, a high-frequency step-up transformer, a WMA-300 power amplifier and a 33600A function generator. The measurements show the V_{DS}-versus-Q results based on ST method for T_1 to T_6 at 100 kHz and 400 V.

For ST experiment, we used a Keysight 33600A function generator, a WMA-300 amplifier and a high-frequency step-up transformer to generate a 400-V peak-to-peak voltage over the device under test (DUT) with its gate shorted to the source, as shown in Fig. B4. For higher frequencies, the application of ST method is not feasible due to several limitations, especially those related to the power amplifier. To investigate C_{OSS} losses at higher frequencies, we employed the non-linear resonance (NR) method introduced in [B16]. Using the setup presented in Fig. B5, enabled the measurement of the losses up to 40 MHz.

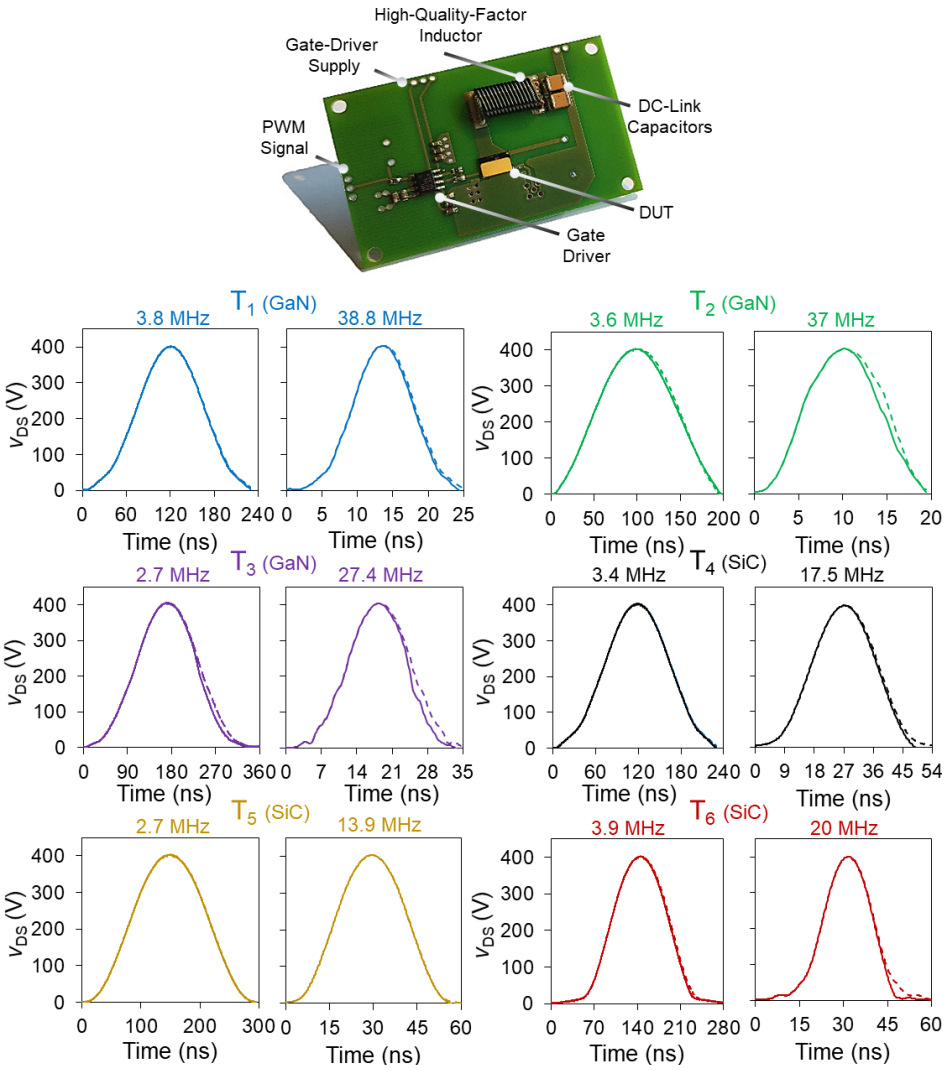

Figure B5 – NR test board together with the time-domain v_{DS} for T_1 to T_6 at two distant frequencies. The dashed curves are the mirrored of the rising half of the generated pulse. A higher deviation from the solid curve indicates higher E_{DISS}.

2.4.3 Conduction Loss

Dynamic $R_{DS(ON)}$ in GaN devices is susceptible to degradation right after a turn-ON transition [B15], [B24], [B25]. It leads to extra power dissipation referred here as dynamic losses (P_{DYN}). The OFF-state voltage has the highest impact on the dynamic $R_{DS(ON)}$ behaviour of soft-switched GaN transistors [B2]. To measure this dependency, we used the pulsed-IV system (AMCAD), where the DUT was subjected to V_{GS} (using gate-probe iTest AM213) and V_{DS} (using 1kV/30A drain-probe PIV AM241) excitations as shown in Fig. B6a, with a 5-µs ON time and 15-µs OFF time. Time-domain $R_{DS(ON)}$ measurements for the device T1 are presented in Fig. B6b for V_{DS} = 0 V, 100 V and 400 V.

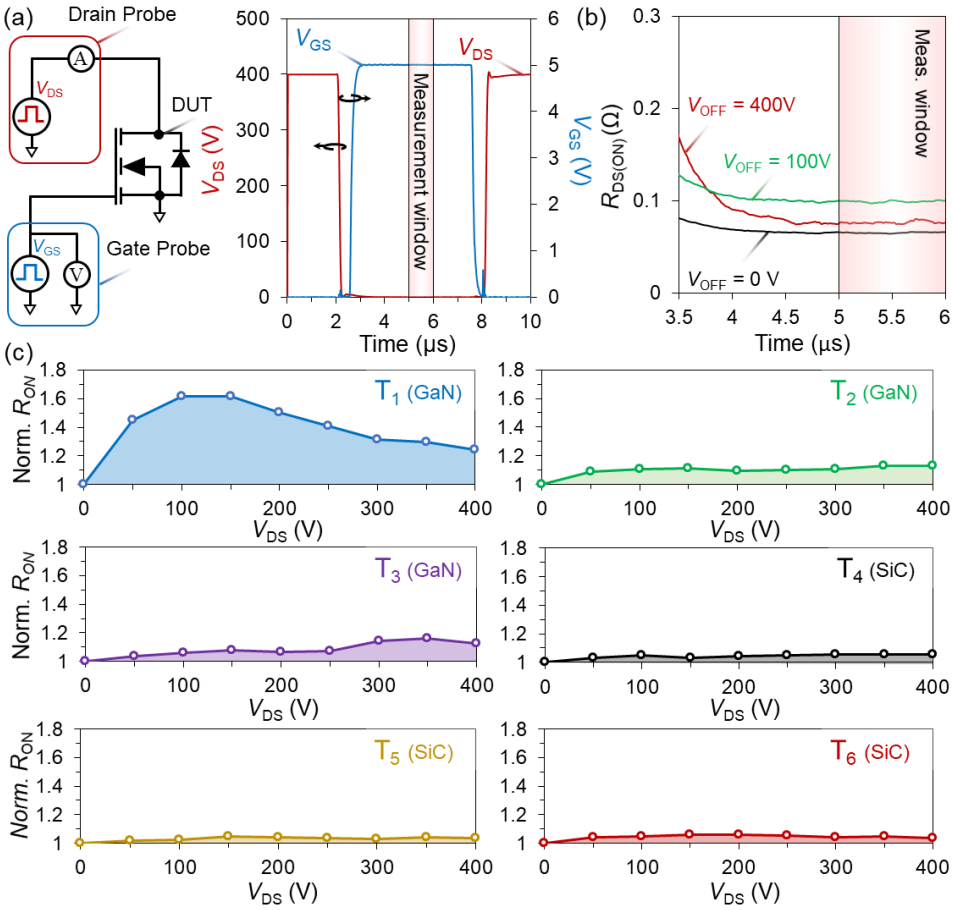

Figure B6 – Dynamic $R_{DS(ON)}$ measurement using pulsed-IV method. (a) The DUT is subjected to V_{GS} and V_{DS} pulses and the resistance was measured after the settling time of the setup was reached. (b) $R_{DS(ON)}$ variation for T1 at OFF-state V_{DS} of 0 V (no voltage stress), 100 V and 400 V. (c) Normalized dynamic $R_{DS(ON)}$ at different V_{DS} values for transistors T1 to T6. $R_{DS(ON)}$-versus-V_{DS} pattern varies between GaN devices.

To capture the actual $R_{DS(ON)}$ and minimize the effect of noise, we averaged the resistance values over a 1-µs interval, after the settling time of the measurement tool had reached (i.e. 2.5 µs after the device was turned ON, as indicated by the measurement windows in Figs. B6a, b). $R_{DS(ON)}$ was measured at 20% of the rated current (i.e. about 6 A). Fig. B6c shows the $R_{DS(ON)}$ normalized by its measured value at V_{DS} = 0. In T1, we observed a degradation of 25% at 400 V, and even larger at lower voltages, whereas T2 and T3 exhibited lower degradations. $R_{DS(ON)}$ degradation was almost absent in SiC transistors T4 to T6.

2.4.4 Overall Comparison of Soft-Switching Losses

The soft-switching losses of devices T1 to T6 up to 5 MHz are summarized in Fig. B7. The devices were driven at their respective nominal gate voltages with 50% duty cycle and 20% of their rated currents at V_{DS} = 400 V. The loss due to conduction is divided into P_{CON} and P_{DYN}. P_{DYN} represents only the contribution of the dynamic $R_{DS(ON)}$ degradation, whereas P_{CON} considers the measured value of $R_{DS(ON)}$ at V_{DS}= 0.

Fig. B7 illustrates that GaN device T_1 has the lowest overall losses. Despite exhibiting the most severe $R_{DS(ON)}$ degradation at 400 V (also see Fig. B6c), due to its low gate and output capacitance losses, T_1 is advantageous for VHF applications, especially those with low duty cycles or small currents. Relatively higher gate losses and special gate-drive circuitry impose limitations on high-frequency application of

GaN transistors such as T_2, whose gate behaves similarly to a diode at large V_{GS} values. A cascode arrangement enables higher threshold voltage in T_3 (compared to GaN devices T_1 and T_2) and lower gate loss in T_6 (compared to SiC devices T_4 and T_5); however, higher output-capacitance losses are observed for these cascode devices, even at low frequencies. Besides, the observed gate resonance in T_3, together with its negative resistance behavior [B26], could result in large-signal instabilities [B27].

By combining the estimation methods and measurements presented in the previous sections, one could extend the loss evaluation to higher frequencies (even up to 40 MHz).

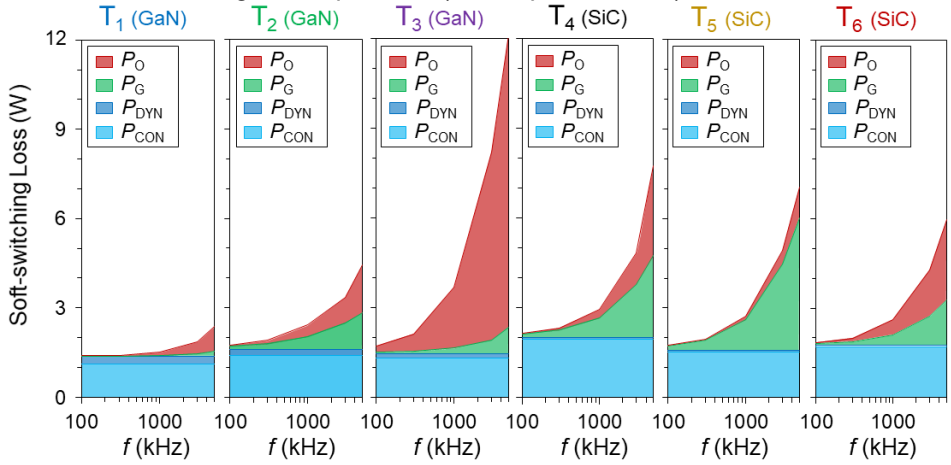

Figure B7 – Soft-switching loss components versus frequency for transistors T1 to T6 at nominal V_{GS} when transistors are subjected to a V_{DS} of 400 V and 20% of their nominal current. The comparison is of great significance for selection of WBG devices, efficiency optimization and proper design of cooling systems.

2.5 Novel real-time calorimetric method for precise circuit-level evaluation of efficiency.

Accurate measurement of converter loss is important for evaluating efficiency, optimizing performance and designing proper cooling systems. We proposed a novel real-time calorimetric method with details about the design of the entire operational system.

The proposed calorimeter enables geometry-independent loss measurements by transferring the heat to the water through heat-exchangers (convection) and cold plates (conduction). Two identical heat-insulated chambers are placed inside an outer chamber that isolates the calorimeter from the ambient (See Fig. C1). The water at ambient temperature flows through the DUT chamber and after absorbing the heat generated by the DUT, gets cooled down to the ambient temperature using an external heat-exchanger. The liquid then flows through the calibration (CAL) chamber and heats up with its dissipated power (P_{CAL}). After the calibration chamber, another external heat-exchanger cools down the liquid to the ambient temperature. The entire heat-transfer cycle is repeated until the temperatures reach steady state. Such a closed loop for the coolant ensures a constant flow in both chambers and eliminates the need for precise flow measurements. Temperature gradients T4-T3 and T2-T1 are measured and compared constantly, and a proportional-integral (PI) regulator adjusts PCAL, such that both chambers have equal steady-state temperature gradients. Thus, the DUT losses, P_{DUT}, can be derived at steady state as

$$T_2\text{-}T_1=T_4\text{-}T_3 \leftrightarrow P_{DUT}=P_{CAL} \qquad \text{(C1)}.$$

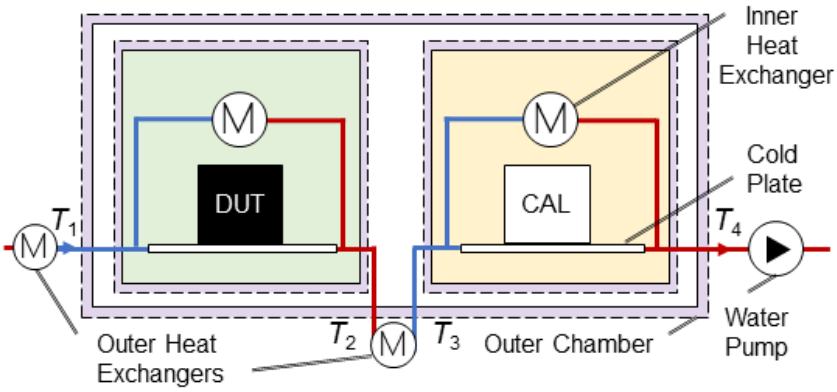

Figure C1 – Schematic of the proposed calorimeter. Water flows in identical chambers containing DUT and CAL. Heat is transferred to the water through heat-exchangers (convection) and cold plates (conduction). The water temperature rise is measured across both chambers and compared for loss evaluation. The blue lines indicate cold water and red lines represent hot water after absorbing the energy dissipated in the chambers. The arrows show flow direction.

2.5.1 System Design

Fig. C2a shows the outer chamber with dimensions 120×66×70 cm^3, made of polystyrene insulator. The water circuit (inset of Fig. C2a) includes a water reservoir connected to a μ-diaphragm pump with a pulsation-damper, to stabilize the low flow of the liquid. Low flow rates enable higher water-temperature rise and thus a higher sensitivity. Inner chambers are consisted of polystyrene boxes with dimensions of 48×42×36 cm^3 and are covered with shielding foils to suppress the effect of EMI from the DUT on the measurements by having the sensors outside the chambers (Fig. C2b). They enclose an aluminium container to hold the inner heat exchangers and the cold plates (see Figs. C2c, d). The DUT is mounted on the cold plate, and its hot-spot temperature (T_{HS}) is monitored through the aperture in the container, using thermal imagers to avoid a thermal runaway. To verify the real-time calibration and its dependence on the DUT geometry, two very different fixtures, *A* and *B*, were employed as shown in Fig. C2e. The fixture *A* is an array of thick-film resistors mounted on a printed circuit board (PCB). The fixture *B* is a power resistor connected to the cold plate using only one nylon stand-off (with poor thermal conductivity to the cold plate).

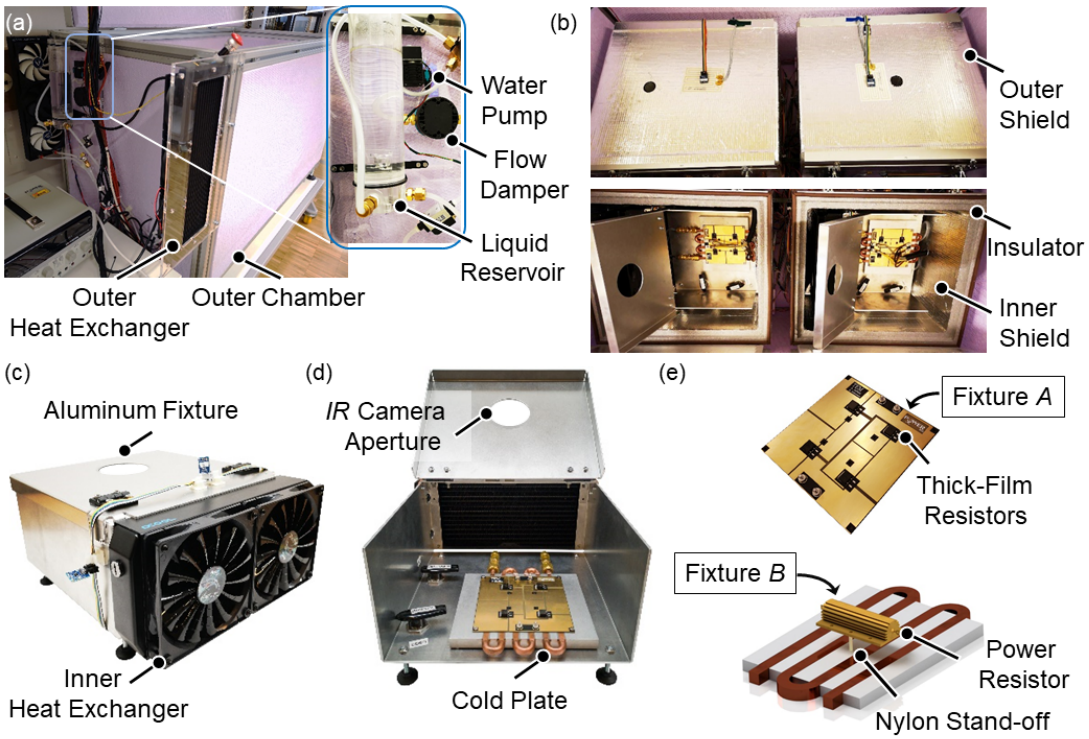

Figure C2 – Calorimeter design. (a) The outer chamber and heat exchangers, together with the water circuit. (b) The inner chambers with the aluminium fixtures inside and shielding foils all over the inner and outer walls to suppress the effect of radiated EMI on the measurements. (c) The container holding inner heat exchangers and cold plates. (d) The back view of the container with resistors mounted on the cold plate. (e) An array of thick-film resistors (Fixture *A*) and a power resistor mounted on the cold plate using only a nylon stand-off (Fixture *B*) are used to verify the absence of any dependence of the calorimeter on the DUT geometry.

2.5.2 DC Calibration

DC calibrations were performed to verify that both chambers are identical and to ensure that the measurement method has no dependency on the geometry of the DUT. In dc calibrations, equal levels of power were dissipated in both chambers, and the water temperature gradients were measured and compared. The flow rate was adjusted using the power of the μ-diaphragm pump. As illustrated in Fig. C3a, using a low flow (minimum pump pressure) enabled a good sensitivity to losses as low as 100 mW with a mismatch of less than 10% up to 10 W, which is attributed to the temperature measurement errors (see Fig. C3b).

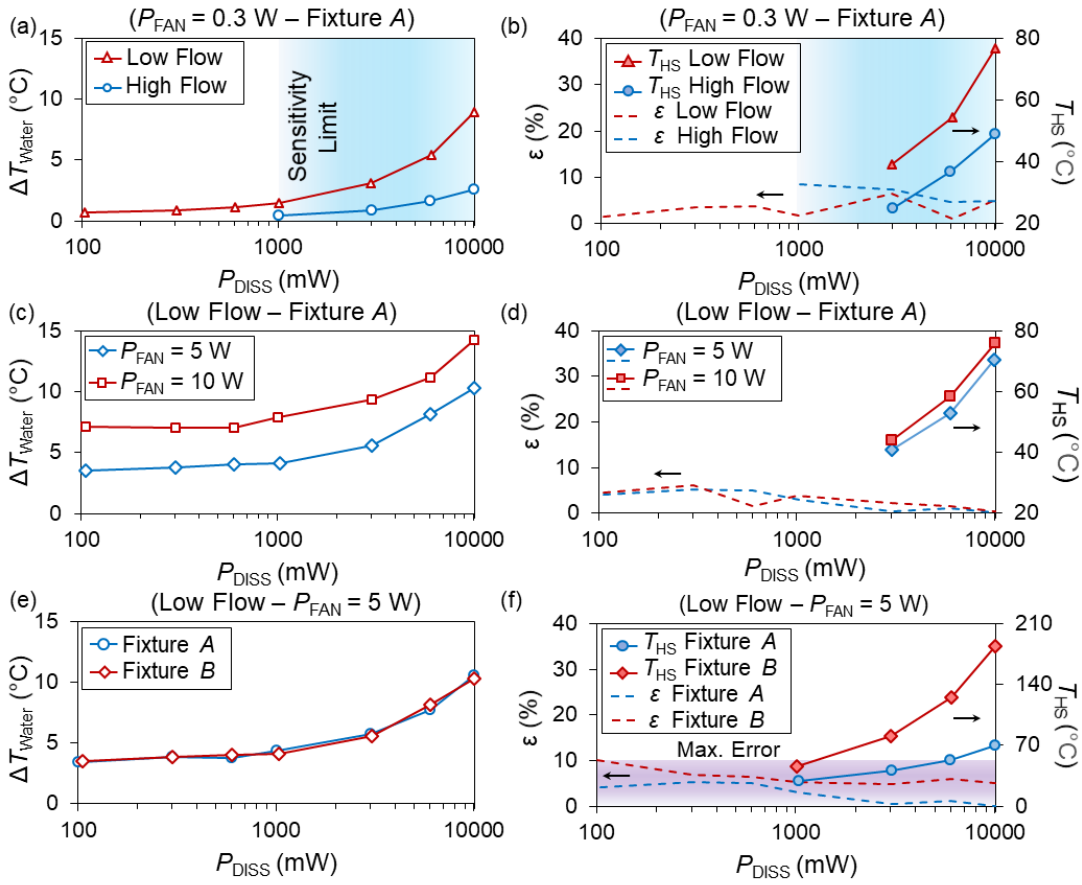

Figure C3 – Steady-state dc calibration. (a) The effect of different water flow rates. Low flow increases the sensitivity. High flow enables better cooling of the DUT. (b) The effect of P_{FAN} at 5 W and 10 W. Increasing fan power leads to higher steady-state T_{HS}. This parameter is instrumental to converters and components that use a heatsink for cooling. (c) The effect of DUT geometry. Due to the low thermal conductivity of the fixture *B* to the cold plate, it has a much higher T_{HS}. However, ΔT_{Water} remains similar in both cases, exhibiting no dependence on DUT geometry. The mismatch errors of less than 10% for losses as low as 100 mW indicate similar designs of the two chambers and repeatability of the results.

A minimum P_{FAN} of 0.3 W was used for homogenous air circulation. We repeated the dc calibrations for a high flow rate, corresponding to the maximum pump pressure, and an error less than 10% was maintained for losses down to 1 W, where the water temperature gradient (ΔT_{Water}) reached the accurate detection threshold of the sensors. As Fig. C3b shows, high flow rates result in lower T_{HS} for the DUT,

which can be tuned to avoid its thermal runaway, depending on the DUT loss level and the overall thermal resistance. P_{FAN} is a secondary tunable parameter, whereby increasing the air flow, a better convective heat transfer through the inner heat-exchangers is achieved. Fig. C3c presents the cases where 5 W and 10 W are consumed by the fans. As the chambers are thermally insulated, higher fan powers result in larger steady-state T_{HS}. However, increasing P_{FAN} results in higher air velocity and thus a better convective heat transfer, which is more advantageous for converters using heatsinks for their cooling. As Fig. C3d shows, for P_{FAN} values of up to 10 W, an error much lower than 10% was obtained. To investigate the dependence of the calorimeter on geometry of the heat source, fixtures *A* and *B* were compared. Even with such extreme changes in the geometry of the heat source and its coupling to the system, ΔT_{Water} remained similar (see Fig. C3e), and a maximum error of 10% was obtained (see Fig. C3f), indicating the independent performance of the calorimeter with respect to the DUT geometry. The higher overall T_{HS} observed using the fixture *B* (shown in Fig. C3f), suggests that the heat transfer is dominated by the cold plate. Hence, DUTs with larger losses should have a better thermal coupling to the cold plate by using a thermal interface material (TIM). Heat sinks could also be utilized to improve the convective heat transfer. The mismatch errors of less than 10% for all the dc calibrations show the repeatability of the measurements as well as the identical thermal resistances of the two chambers to the water circuit. Although the water temperature sensors are highly linear within the measured ranges, their limited accuracy is the main source of the observed mismatches.

2.5.3 Power Tracking and Accuracy

Fig. C4a presents the transient ΔT_{Water} for both chambers, together with the power tracking in CAL, when DUT is dissipating 7.8 W. A PI regulator provided the reference power (P^*_{CAL}) to a dc source to satisfy (C1), as shown in Figs. C4b, c.

The system constantly monitored T_{HS} in the chambers and limited the power to the CAL and DUT to avoid thermal runaway. The proportional (k_P) and integral (k_I) coefficients were set to tune the power tracking transient. The power is measured by multiplying the voltage and current of the calibrator using Fluke 45 multimeter as

$$P_{CAL}=(V_{CAL}\pm\epsilon_V)(I_{CAL}\pm\epsilon_I) \qquad \text{(C2)}$$

in which ε_V = 0.025% and ε_I = 0.2% are the dc voltage and dc current measurement errors, respectively. At steady state, the temperature rise in the water is linearly proportional to the dissipated power (see the left-side curves in Fig. C3, and note that the power is in logarithmic scale). Based on (C1) and (C2), one can extract the tracked power (P_{TRACK}) as

$$P_{TRACK}=P_{LOSS}(1\pm\epsilon_V\pm\epsilon_I)\frac{\Delta T_{DUT}\pm 2\epsilon_T}{\Delta T_{CAL}\mp 2\epsilon_T} \qquad \text{(C3)}$$

in which P_{LOSS} is the *actual* power dissipation and ε_T = 0.1 °C is the error involved in the water temperature measurements. In the first parenthesis of (C3), the values of ε_I and ε_V are much smaller than unit, and thus are negligible. Fig. C5 presents the measurement error (ε) for the proposed calorimeter for various power dissipations, when a low flow rate is applied and P_{FAN}= 0.3 W.

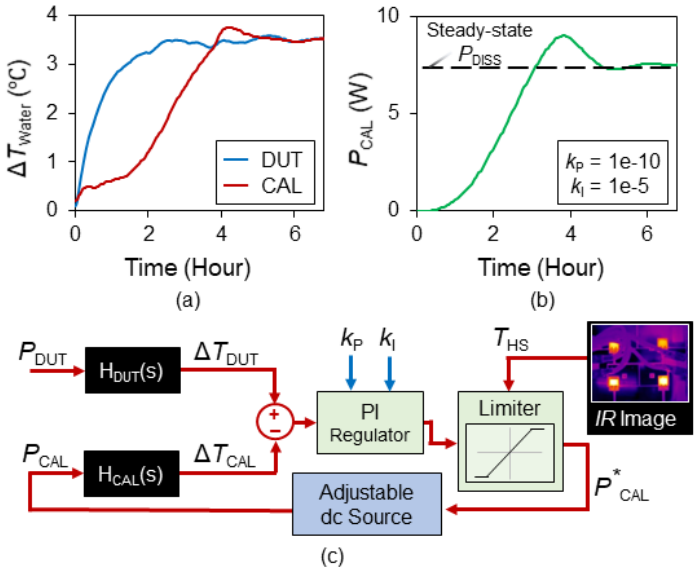

Figure C4 – System transient response and control scheme. (a) Water temperature gradients and (b) the corresponding power tracking for a 7.8-W test. (c) Controller implementation. Temperature gradients are compared, and a PI regulator adjusts P^*_{CAL} to equalize the temperature gradients. MyRio-1900 was employed as controller. An IR camera provides T_{HS} to avoid device thermal runaway.

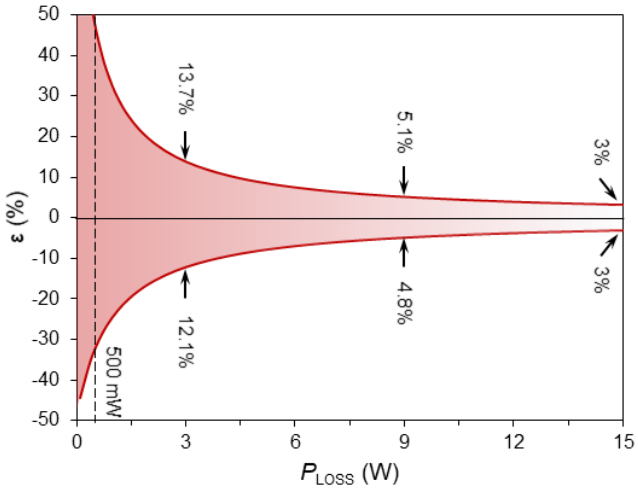

Figure C5 – Power tracking error vs. the actual dissipated power when the low flow is applied. The system can measure P_{LOSS} = 500 mW (indicated by the dashed line) with an error of less than 50%. The error is significantly reduced at higher losses. The accuracy at low losses can be improved by using more accurate water temperature sensors.

TABLE C-I summarized the performance of the demonstrated calorimeter with the previous literature, where the proposed system significantly extends the measurement range down to mW while maintaining a high accuracy.

TABLE C-I
METHODS USED IN CALORIMETRIC SYSTEMS

Reference	System	Type/ Coolant	Minimum Power	Accuracy	Accuracy Limitation
[C1]	Single-chamber	Closed/ Water	74.5 W	±0.5 W	Flowmeter, water temp. sensors
[C2]	Double-chamber	Open/ Air	200 W	±15 W	Uneven air flow, air variations
[C3]	Single-chamber	Closed/ Water	10 W	Max {±0.4 W, 1%}	Flowmeter, water temp. sensors
This work [C4]	Double-chamber	Closed/ Water	500 mW	At 500 mW: +50%/ -30% At 15 W: ± 3%	Water temperature sensors

2.5.4 Component-Level Loss Measurement

Low losses in components with high-frequency ac excitations (e.g. inductors and transformers) and fast voltage and current transitions (e.g. switches and diodes) can be very difficult to be measured electrically. The proposed calorimeter overcomes the difficulties of electrical measurements at high frequencies (tens of MHz) and unlike most electrical methods which extract inductor losses only under sinusoidal excitations, it can measure these losses under real power circuit operation, regardless of waveforms, frequencies and transition speeds (i.e. dv/dt) applied.

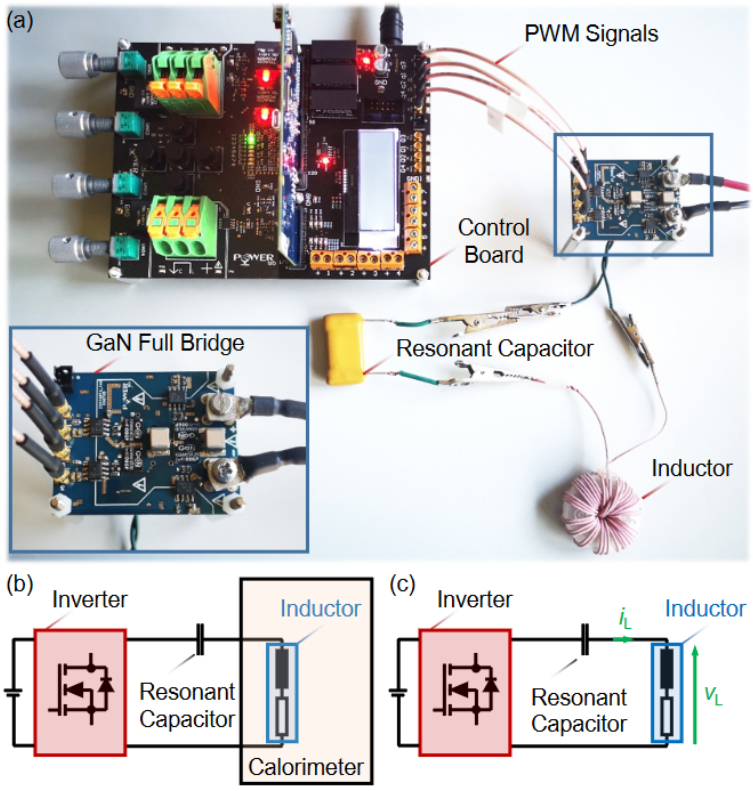

Figure C6 –Large-signal loss measurement setup. (a) a controller using TMS320F28379D DSP generates PWM signals to drive a GaN-based inverter. In order to make a resonance, the inductor was in series with a highQ (mica) capacitor. (b) shows a setup for calorimetric measurement, and (c) shows a setup for electrical measurement using MSO64 oscilloscope with voltage (TPP1000) and current (TCPA300 Amplifier + TCP305) probes.

Two sets of measurements were performed to extract the inductor losses. In Fig. C6 configuration, the calorimeter was used to measure inductor losses. According to the configuration in Fig. C6c, a voltage probe with 1 GHz of bandwidth (BW) and current probe with BW = 50 MHz were employed to extract the overall (core and winding) losses involved in each charging-discharging cycle of the inductors.

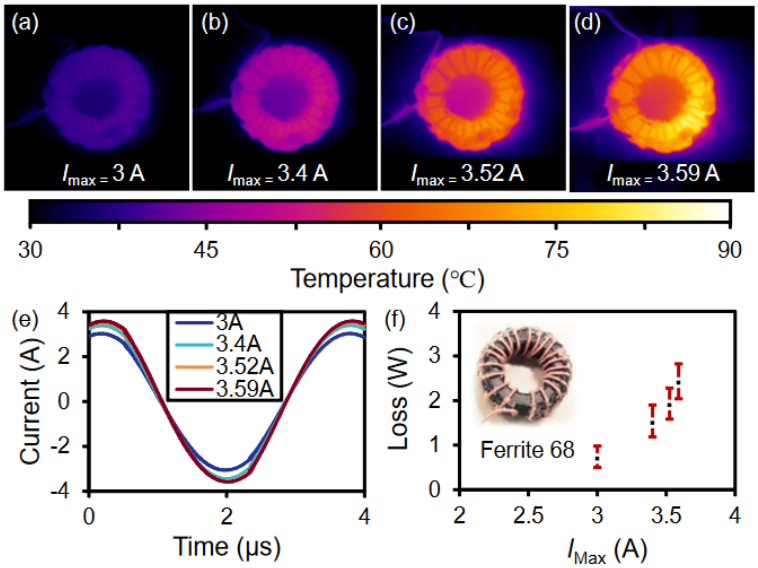

Figure C7 –Thermal measurements for the Ferrite 68 inductor. (a) to (d) present device temperatures under different peak currents ranging from 3 A to 3.59 A. (e) shows current waveforms and (f) provides the losses measured by the proposed calorimeter. The error bars are indicated for each measurement. A low water flow rate and an inner fan power of 300 mW were applied.

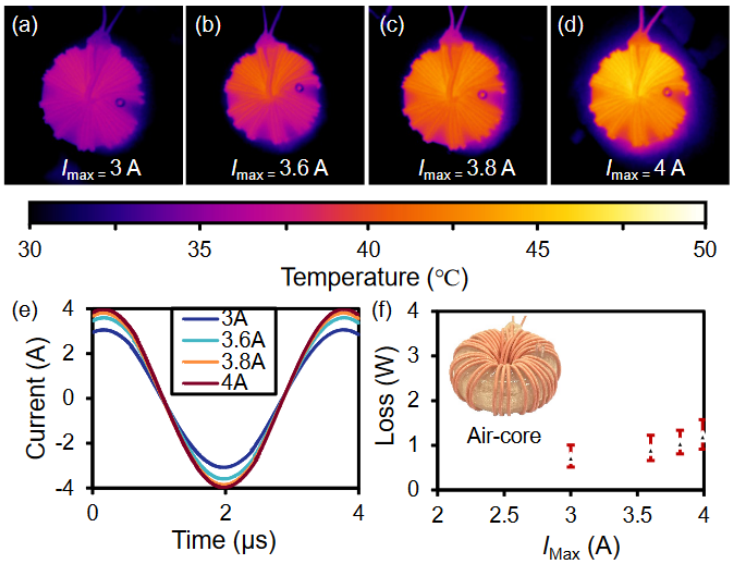

Figure C8 – Thermal measurements for the air-core inductor. (a) to (d) present device temperatures under different maximum currents ranging from 3 A to 4 A. (e) shows the current waveforms and (f) provides the losses measured by the proposed calorimeter. The error bars are indicated for each measurement. A low water flow rate and an inner fan power of 300 mW were applied.

The calorimetric measurements are presented in Fig. C7 and Fig. C8, in which the inductors were subjected to current excitations at a fundamental frequency of 277 kHz, with different amplitudes. Figs. C7a-d present IR thermographs of the ferrite 68 inductor with peak currents ranging from 3 A to 3.59 A, as shown in Fig. C7e. The losses are plotted in Fig. C7d (uncertainty ranges are indicated in red). Figs. C8a-d show the IR thermographs of the air-core design, with peak currents ranging from 3 A to 4 A (see Fig. C8e), and losses plotted in Fig. C8d. Unlike the air-core design, ferrite 68 inductor losses increase significantly with current excitation amplitude (cf. Fig. C7f and Fig. C8f).

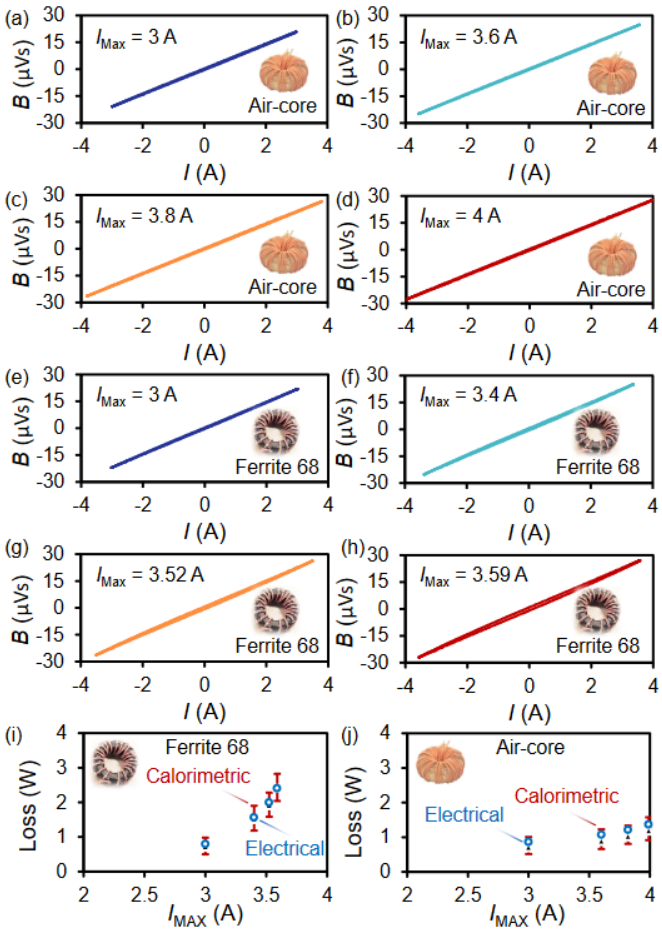

Figure C9 – Measurement results. (a) to (d) present the B-I curves for the ferrite 68 inductor with peak currents from 3 A to 3.59 A. (e) to (h) present the B-I curves for the air-core inductor with peak currents from 3 A to 4 A. (i) and (j) compare the electrical and calorimetric results. The calorimeter accuracy is verified by the electrical measurements. For inductors operating at several tens of MHz, loss measurement based on electrical methods is not feasible, due to the BW limitations of probes, especially current probes.

In parallel with each calorimetric measurement, an electrical measurement was performed to extract magnetic flux density (B) over current (see Figs. C9a-h). The B-I curves were used to calculate electrical loss as

$$P_E = f \int IdB \qquad \text{(C4)}$$

P_E incorporates hysteresis loss (as the major source of power dissipation in ferrite cores) and winding loss. Figs. C9i, j compare extracted losses based on calorimetric and electrical methods, and the calorimeter obtained an outstanding accuracy in loss measurements, verified by electrical measurements at a relatively low fundamental excitation frequency of 277 kHz, at which the BW of probes were sufficient. Nonetheless, for inductors operating at higher frequencies (i.e. several tens of MHz), BW limitations of probes (especially in current probing) hinder their utility. For such applications, the proposed calorimeter provides a simple, accurate and cost-effective solution to capture small losses.

3 Conclusions

In this work, we have proposed novel methods to investigate output capacitance-related losses, and applied to investigate all four prominent power FET categories (planar-Si, Si-SJ, SiC and GaN) for their output capacitance-related QV hysteresis patterns. A categorical overview of hysteresis patterns of different device structures was presented along with their frequency dependence. We have shown that different structures exhibit different dependencies on excitation voltage levels, resulting in diverse hysteresis patterns. For instance, some structures show no hysteresis below 100 V, whereas for another group, hysteresis is a high-voltage (above 150-200 V) phenomenon. These observations are essential in identifying the underlying physical phenomena in output-capacitance-related losses. The modelling of the voltage dependence of QV hysteresis patterns in spice simulations is essential for a more realistic analysis of switching transients and losses.

In addition, we proposed a new C_{OSS} model and measurement technique that enables selection of devices with lowest C_{OSS} losses among different WBG transistors, just by performing one small-signal measurement: R_S-versus-frequency. It is also possible to use the measured R_S together with C_{OSS} (which can be extracted from datasheet) to estimate the amount of C_{OSS} losses. The generality and robustness of this method enables it to quantify C_{OSS} losses of WBG transistors, which is a crucial source of losses in soft-switched power converters, and to select devices with the best performance.

Then, we demonstrated a comprehensive loss-breakdown analysis for soft-switching operation of wide-band-gap transistors. A small-signal input capacitance measurement versus gate-to-source voltage was used to evaluate gate losses under soft-switching conditions, and its accuracy was experimentally verified. By using a combination of ST (for f < 1 MHz) and NR methods (for 1 MHz < f < 40 MHz), we demonstrated the variation of large-signal C_{OSS} losses for different technologies over a wide frequency range. To obtain an overall view of the losses, we further compared the degradation of dynamic $R_{DS(ON)}$ and its dependence on the off-state voltage using a standard pulsed-IV method. Three SiC and three GaN devices were evaluated and compared for their gate losses, output capacitance losses, and conduction losses up to 5 MHz. The most severe $R_{DS(ON)}$ degradation and the lowest gate losses were observed in a p-GaN-gated device (T_1), which is the best choice for VHF applications, especially those with low duty cycles or small currents. The cascode arrangement in SiC and GaN devices offers advantages such as increased threshold voltage and reduced gate loss. However, the output capacitance losses are aggravated at high frequencies, which limit their high-frequency operation. The demonstrated measurement methods are general and can be used to evaluate the soft-switching losses in other WBG transistors. Given the diversity of WBG technologies, this work presents the major trade-offs in selecting a power device to maximize the system efficiency, and to carry out a proper thermal design for high-frequency soft-switching applications. This analysis is also insightful for device engineers to design high-performance power transistors for high-frequency applications.

Finally, we proposed a closed-type dual-chamber calorimeter with high accuracy and large measurement range. The calorimeter can measure low levels of power dissipations, enabling measurement of losses down to 500 mW. The method reduces measurement time and avoids further data processing by applying a real-time calibration. The outstanding accuracy of the calorimeter for measuring low losses in power inductors was demonstrated. Being simple, cost-effective and accurate, the proposed calorimeter concept paves the way for loss measurements in the high and very high frequency domains.

4 Outlook and next steps

As future work, we will continue to investigate the sources of output capacitance losses of different device technologies. Depending on the device structure, circuit level design methods will be explored to remedy the output capacitance losses under soft switching operations.

We will also focus on another important source of high frequency losses, dynamic ON-resistance degradation, exclusively for GaN devices. The device behaviour will be studied under real circuit operation to understand its implication on system level performance and facilitate the comparison of different device technologies.

5 National and international cooperation

Although the execution of this project did not rely on any national or international cooperation, it has opened many door for future collaborations. We have been in discussions with the companies *Sonceboz* (Switzerland) and *Infineon* (Austria) to use the proposed techniques and technologies in some of projects of interest for them.

6 Communication

This project has led to many publications in top journals and conferences in the field, as described below. The results of this project have also been presented during the PECTA workshop.

7 Publications

1 N. Perera, G. Kampitsis; R. Van Erp; J. Ançay; A. Jafari; M. S. Nikoo; E. Matioli, “Analysis of Large-Signal Output Capacitance of Transistors using Sawyer–Tower Circuit,” IEEE J. Emerg. Sel. Topics Power Electron., DOI: . /JESTPE.2020.2992946, 2020 1109, doi: 10.1109/JESTPE.2020.2992946.

2 N. Perera, M. S. Nikoo, A. Jafari, L. Nela, and E. Matioli, “Coss Loss Tangent of Field-Effect Transistors: Generalizing High-Frequency Soft-Switching Losses,” IEEE Trans. Power Electron., vol. 35, no. 12, pp. 12585–12589, Dec. 2020, doi: 10.1109/TPEL.2020.2990370.

3 N. Perera, A. Jafari, L. Nela, G. Kampitsis, M. Samizadeh Nikoo, and E. Matioli, “Output-Capacitance Hysteresis Losses of Field-Effect Transistors,” presented at the Twenty-first IEEE Workshop on Control and Modeling for Power Electronics (COMPEL 2020), Aalborg, Denmark.

4 A. Jafari, M. S. Nikoo, N. Perera, H. K. Yildirim, F. Karakaya, R. S. Z. Ardebili, E. Matioli, "Comparison of Wide-Band-Gap Technologies for Soft-Switching Losses at High Frequencies," in IEEE Transactions on Power Electronics, vol. 35, no. 12, pp. 12595-12600, Dec. 2020, doi: 10.1109/TPEL.2020.2990628.

5 A. Jafari, M. Heijnemans, R. S. Z. Ardebili, R. van Erp, M. S. Nikoo, E. Figini, F. Karakaya, E. Matioli, "High-Accuracy Calibration-Free Calorimeter for the Measurement of Low Power Losses," in IEEE Transactions on Power Electronics, vol. 36, no. 1, pp. 23-28, Jan. 2021, doi: 10.1109/TPEL.2020.3001001.

6 A. Jafari, M. S. Nikoo, F. Karakaya, N. Perera and E. Matioli, "97.4%-Efficient All-GaN Dual-Active-Bridge Converter with High Step-up High-Frequency Matrix Transformer," *PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Germany, 2020, pp. 1-8.

7 Mohammad Samizadeh Nikoo, Armin Jafari, Nirmana Perera, and Elison Matioli, Negative Resistance in Cascode Transistors, *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 9978-9981, Oct. 2020, doi: 10.1109/TPEL.2020.2978658.

8 Armin Jafari, Mohammad Samizadeh Nikoo, Furkan Karakaya and Elison Matioli, Enhanced DAB for Efficiency Preservation using Adjustable-Tap High-Frequency Transformer *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 6673-6677, July 2020, doi: 10.1109/TPEL.2019.2958632.

9 Mohammad Samizadeh Nikoo, Armin Jafari, Nirmana Perera, and Elison Matioli, New Insights on Output Capacitance Losses in Wide-Band-Gap Transistors, *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 6663-6667, July 2020, doi: 10.1109/TPEL.2019.2958000.

10 Mohammad Samizadeh Nikoo, Armin Jafari, Nirmana Perera, and Elison Matioli, Measurement of Large-Signal C_{OSS} and C_{OSS} Losses of Transistors Based on Nonlinear Resonance, *IEEE Transactions on Power Electronics*, vol. 35, no. 3, pp. 2242-2246, March 2020, doi: 10.1109/TPEL.2019.2938922.

11 Mohammad Samizadeh Nikoo, Armin Jafari, Nirmana Perera, and Elison Matioli, Output capacitance losses in wide-band-gap transistors: A small-signal modeling approach, in Proc. 32nd Int. Symp. Power Semiconductor Devices ICs (ISPSD), Sep. 2020, pp. 190–193, doi: 10.1109/ISPSD46842.2020.9170093.

12 Mohammad Samizadeh Nikoo, Armin Jafari, Nirmana Perera, Halil Kerim Yildirim, and Elison Matioli, Investigation on Output Capacitance Losses in Superjunction and GaN-on-Si Power Transistors, In 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), pp. 48-51. IEEE, 2020. doi: 10.1109/IPEMC-ECCEAsia48364.2020.9367884.

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