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2-Watt Router

Ultra Low Power Residential Gateway

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Zusammenfassung

Der Stromverbrauch eines einzelnen Residential Gateways beträgt heutzutage ca. 7-10 Watt. Als einzelnes Gerät betrachtet ist das nicht viel, doch wenn man bedenkt, dass durch die zunehmenden ip-Services ein Residential Gateway bald in jedem Haushalt 24 Stunden in Betrieb sein wird, trägt er gesamtschweizerisch trotz allem zu einem Stromverbrauch in der Höhe von 12 – 17 Megawattstunden bei

Ziel dieser Arbeit war es zu beweisen, dass es möglich ist, einen Gateway zu bauen, der im Durchschnitt nur 2 Watt Strom verbraucht. Das geht weit über die gesetzten Ziele des European Code of Conduct hinaus, einem strengen Standard, der jährlich verschärft wird und von der Industrie immer nur knapp eingehalten werden kann.

Die gesetzten Ziele wurden erreicht. Die Arbeit zeigt, dass man nebst sorgfältiger Evaluation der HW Komponenten die konventionellen Systemgrenzen verlassen muss und HW und SW intelligent miteinander verknüpfen muss, wenn man bei der Anwendererfahrung nur kleine Kompromisse machen will.

Résumé

La consommation en énergie d'un seul Residential Gateway est actuellement de 7-10 Watts. Cela ne semble pas excessif pour un seul appareil. Toutefois, lorsqu'on considère le fait que bientôt, à cause de la recrudescence des services IP, un Residential Gateway sera en service 24/24 h dans chaque ménage suisse, il contribuera à une consommation d'énergie de l'ordre de 12-17 Mégawattheure

L'objectif du présent travail est de prouver qu'il est possible de construire un Gateway qui consomme seulement 2 Watts. Cela va bien au-delà des objectifs fixés par le Code de Conduite européen (European Code of Conduct), un standard strict qui devient de plus en plus exigeant chaque année et que l'industrie a beaucoup de peine à pouvoir respecter.

Les objectifs définis ont pu être atteints. Le présent travail démontre qu'en plus d'une évaluation méticuleuse des composantes de l'appareil, l'on doit dépasser les limites conventionnelles du système. Pour ce faire, il faut étroitement lier les composants matériels avec les composants logiciels, surtout si l'on veut éviter de faire de grands compromis quant à l'expérience des utilisateurs.

Abstract

The energy consumption of a single Residential Gateway is currently 7-10 Watts. This may not seem excessive for one device. Nevertheless, considering the fact that IP services will very soon require that gateways remain on 24/7 in every Swiss household, this will amount to a total consumption of 12-17 Megawatthours
The aim of this study is to prove that it is possible to build a gateway that only consumes 2 Watts. This goes beyond the targets set by the European Code of Conduct, a very strict code that has become stricter with each year and that the industry can only barely respect.
The set targets have been achieved. This study shows that, besides a very careful selection of HW components, the conventional system limits have to be abandoned. The key is to combine HW and SW in an intelligent manner, especially if we want to avoid making big compromises in the User Experience.

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1 Introduction and Goal of Project

Swisscom is one of the ten biggest consumers of electricity in Switzerland. While being responsible company, Swisscom is introducing different measures to use resources such as electricity, fuel, and waste more efficiently. As one of these measures Swisscom works on improving the efficiency of its infrastructure.

One component of this infrastructure is the Residential Gateway (also called IAD). The Residential Gateway is a device connected to the telephone line in each household that uses Swisscom broadband Internet access. These devices currently consume between 7 and 10 Watts of electricity and they typically remain switched on all the time (24 hours a day, 7 days a week). For a single device this does not sound that much but when multiplied by the 1.7 Mio (approximate number of Swisscom broadband users) this is a an aggregated constant electricity consumption of 12 – 17 MWh which is already a significant number.

The intention of this project is to design a communication system, which allows VDSL2 transmission, voice communication (VoIP) and is also equipped with wireless access point (Wi-Fi) called later in this document a Low Power Residential Gateway (LPRG). The key point is the energy efficiency. The system should be optimized with regard to power consumption.

2 Requirements

The gateway should be realized according to ITU-T recommendations. In particular since the LPRG is equipped with FXS, the incoming calls must be possible at all times (unless the user explicitly disables them).

2.1 The main (minimal) functional requirements

- VDSL2 module, which use profile 17a and is interoperable with COs/DSLAMs used in Swisscom over POTS
- WLAN 802.11g/n functionality
- One Fast Ethernet socket
- One FXS port (VoIP)
- Power switch
- Status LED
- WPS button

2.2 Power consumption requirements

The average (calculated over the period of at least 1 week) power consumption of the Low Power Residential Gateway (LPRG) should be as low as possible. Ideally not more than 2 Watts, which is significantly less than the current maximum allowed power consumption defined by the Broadband Equipment Code of Conduct (Version 4.1) - Tier 2013-2014 for such Residential Gateway. It is presented in the table 1 below.

Component	**Idle State [Watt]**	**On State [Watt]**
Gateway with VDSL2 17a	3.2	4.6
Wi-Fi interface, single band IEEE 802.11nradio with up to 23 dBm total EIRP (up to 2x2)	0.8	2.0
1 x Fast Ethernet port	0.2	0.4
1 x FXS port	0.3	1.2
Total	**4.5**	**8.2**

Table 1: Code of Conduct Values

2.3 Project phases

The project has been split into the following 4 phases:

- Phase I
  - Several options of the block-level HW architecture
  - Block-level SW architecture
  - High-level functional description of the SW with a special focus on the power management functions
  - Start of sourcing of evaluation boards, development kits and reference designs
  - Planned duration: 2 month (1/11/2012 – 31/12/2012)
- Phase II
  - Detailed analysis of each option of HW architecture and selection of the most efficient from the power consumption point of view
  - Selected the best chipset to fit low power requirements
  - Final detailed HW architecture
  - Continuation of sourcing of evaluation boards, development kits and reference designs
  - Verification of the interoperability of the selected VDSL2 chipset with Swisscom VDSL2 network
  - Planned duration: 2 months (1/01/2013 – 28/02/2013)
- Phase III
  - The first working prototype based on development kits and reference designs
  - The first version of LPRG firmware
  - Initial report on the prototype power consumption in different usage profiles
  - Initial verification of the interoperability of the prototype with Swisscom VDSL2 network
  - Planned duration: 2 months (1/02/2013 – 31/03/2013)
- Phase IV
  - Final electronic circuit schematics for the prototype of the LPRG
  - BOM of the prototype of the LPRG
  - PCB layout (Gerbers) of the LPRG
  - Final, refined LPRG firmware
  - 10 pcs of fully assembled and working LPRGs, in Swisscom Centro Grande enclosures (enclosures will be provided by Swisscom)
  - Verification of the interoperability of the prototypes with Swisscom VDSL2 network
  - Planned duration: 3 months (1/04/2013 – 30/06/2013)

3 Phase I

3.1 xDSL Energy consumption – State of the art

For many years ITU-T and Broadband Forum have tried to find answer on the following question:

How to minimize energy consumption by ADSL and VDSL?

Generally there are two ways possible. One of them is based on minimizing energy consumption by elements (chipsets). Unfortunately even with the most power efficient chipsets available today as well as in the near future the power consumption of VDSL2 modem alone (without other IAD functions) is in the range of 2-3 Watts.

The second one is based on monitoring of customer behaviour. It can be divided into the following two approaches:

1. methods recommended by ITU-T,
2. solutions, which are out of recommendations.

In this point of the report the state of ITU-T standardization of ADSL and VDSL from a point of view of energy consumption is shortly described.

3.1.1 Low power modes for ADSL2 and ADSL2+

ADSL modem can be in one of the following three states:

State L0

The state L0 is the mode of normal operation. Only when a modem is in this state a full bit rate transmission is possible. So-called bit-swapping operation is allowed only in the state L0. Of course energy consumption level is the highest in the state L0, independently of customer activity. Because of it other states are preferred when modem is not used.

State L2

The state L2 is low power mode. When there is no need for transmission from office unit to customer modem (downstream) the L2 state can be used.

Transition from L0 to L2 is possible. If there is no downstream traffic, central office unit initiates transition procedure. New bit rate and gain are established. Modem can reject request of central office unit.

Modem can initiate transition from L2 to L0, and return to previous full rate transmission, if FIFO buffer is full.

State L3

The state L3 is the mode when no signal is transmitted. In this state the maximum energy saving is achieved.

3.1.2 Low power modes for VDSL2

There is an ongoing work in the ITU-T to define the low power modes for VDSL2, however as of now (December 2012) VDSL2 low power mode similar to ADSL low power (L2) mode do not exist.

Answer to the question 4a/15 Title: VDSL2 low power mode. COM 15 – LS 450 – E, addressed to ITU – Telecommunication Standardization Sector:

> "While early 2011, Q4a/15 agreed to define a VDSL2 low power mode with the goal to consent before the September 2012 SG15 meeting, this goal has not been met. At its 5-9 November, 2012 meeting, ITU-T Q4a/SG15 has re-addressed the VDSL2 low power mode. Q4a/15 has agreed to set the goal to consent of a VDSL2 low power mode before the end of 2013.
>
> To facilitate reaching this goal, Q4a/15 agreed that the VDSL2 low power mode shall be defined in odifyttion with ITU-T G.998.4, shall be friendly for ITU-T G.993.5, and that requirements for VDSL2 low power mode shall be submitted to Q4a/15 by the 18-22 March 2013 Q4a/15 meeting. Q4a/15 invites the Broadband Forum to timely submit requirements related to data rates, latency, impulse noise protection,

and power savings in various low power (sub)states and related to the transitions between such (sub)states and the full power state."

Metanoia (one of the VDSL2 vendors) in July 2013 (COM 15 – C 0173 – E) has submitted a proposal for odifycation of the ITU-T G.998.4 standard that would introduce a support for the Power Efficient Transmission (PET) mode of operation. That proposal would allow up to approx. 40% reduction in the power consumption of the Line Driver. Unfortunately this is only an initial proposal and it is still not clear if this proposal will be accepted by the ITU-T.

3.2 Low power consumption – proposed approach

As outlined in the previous section there are no low power modes defined by the ITU-T yet. Additionally it is not possible to reduce the power consumption to the required level (2 Watts) only by optimizing the chipset used in the LPRG solution.

However, it is always possible to switch off the VDSL2 modem completely, which corresponds to state L3 in ADSL. Naturally the consequence of such approach is that the user is not connected to the Internet and the reconnection time is in the range between 30 seconds and 60 seconds.

It has to be noted that according to our findings switching the VDSL2 modem off should have no serious adverse effect on other VDSL2 pairs/lines in the cable bundle. This is also valid even if the operator, in order to allow higher throughput rates, uses VDSL2 Vectoring technology to cancel the crosstalk between the pairs in the cable bundle.

This approach (see table 2) is expected to be very effective in terms of the power savings because the VDSL2 chipset (DMT, AFE and LD together) is the biggest single contributor in the overall power consumption of the residential gateway.

Mode	Description	Estimated Maximum Power [Watt]	Average duty hours per day	Average consumption [Watt]
M0	VDSL is off, devices are inactive with the exception of modules responsible for incoming calls handling	0.8	12	9.6
M1	VDSL is off, all other parts (including WLAN) are active but not in use	1.2	4	4.8
M2	All devices and ports are active but not in use (FXS in on-hook state, no Ethernet traffic, no WiFi traffic)	4	6	24
M3	All ports are in active use (maximum WLAN throughput, active LAN, ongoing FXS call)	5	2	10
	Average			**2.02**

Table 2: proposed power mode states

M1 mode is almost the same as M0 mode, except that in the M1 mode the WLAN is active. Later in this document they are called low power modes. M2 and M3 modes from the residential gateway sub-system confirmation point of view are the same. Later in this document they are called normal modes.

3.3 Considered high level HW architectures

3.3.1 Single, highly integrated SoC with included DMT as well as AFE but ex-ternal LD

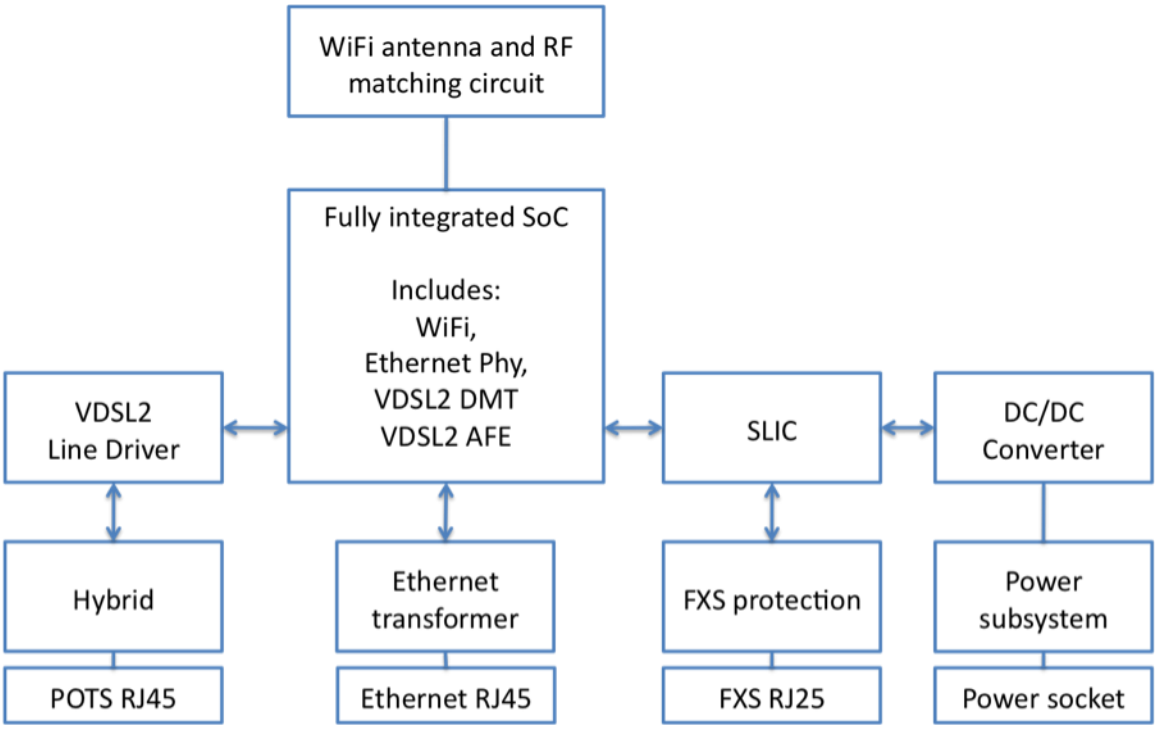

Figure 1: Single, highly integrated SoC with included DMT as well as AFE but ex-ternal LD

3.3.2 Single, highly integrated SoC with included DMT but external AFE and LD

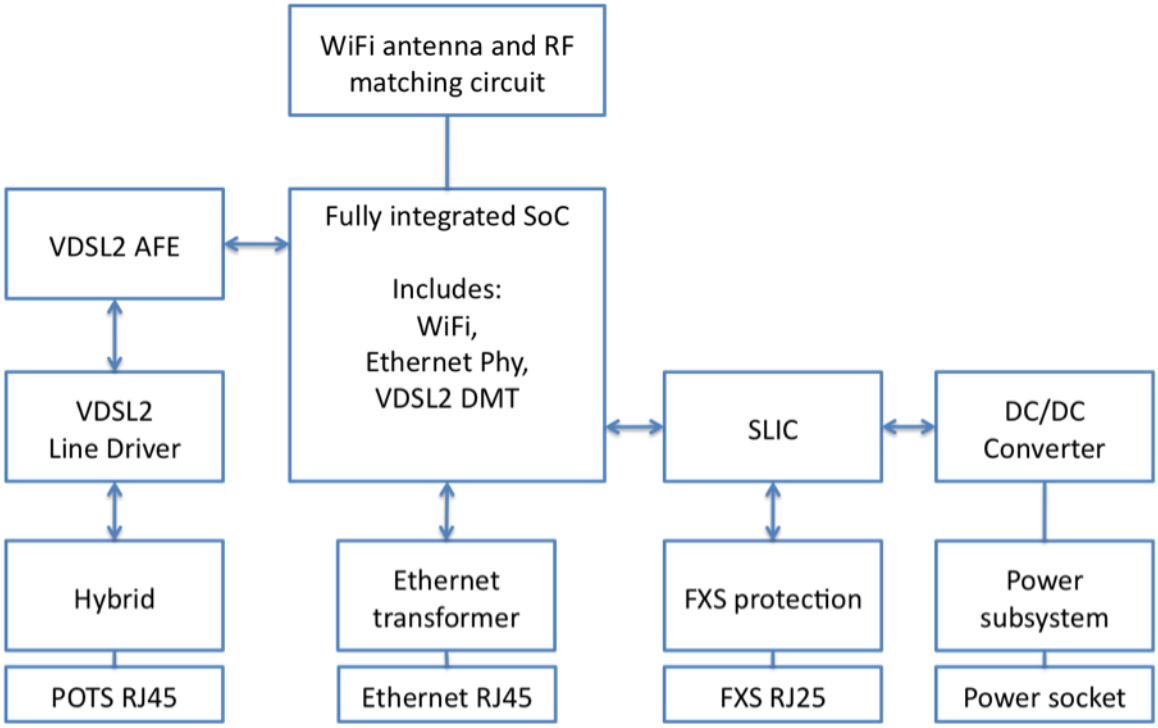

Figure 2: Single, highly integrated SoC with included DMT but external AFE and LD

3.3.3 VDSL2 chipset completely independent of the SoC

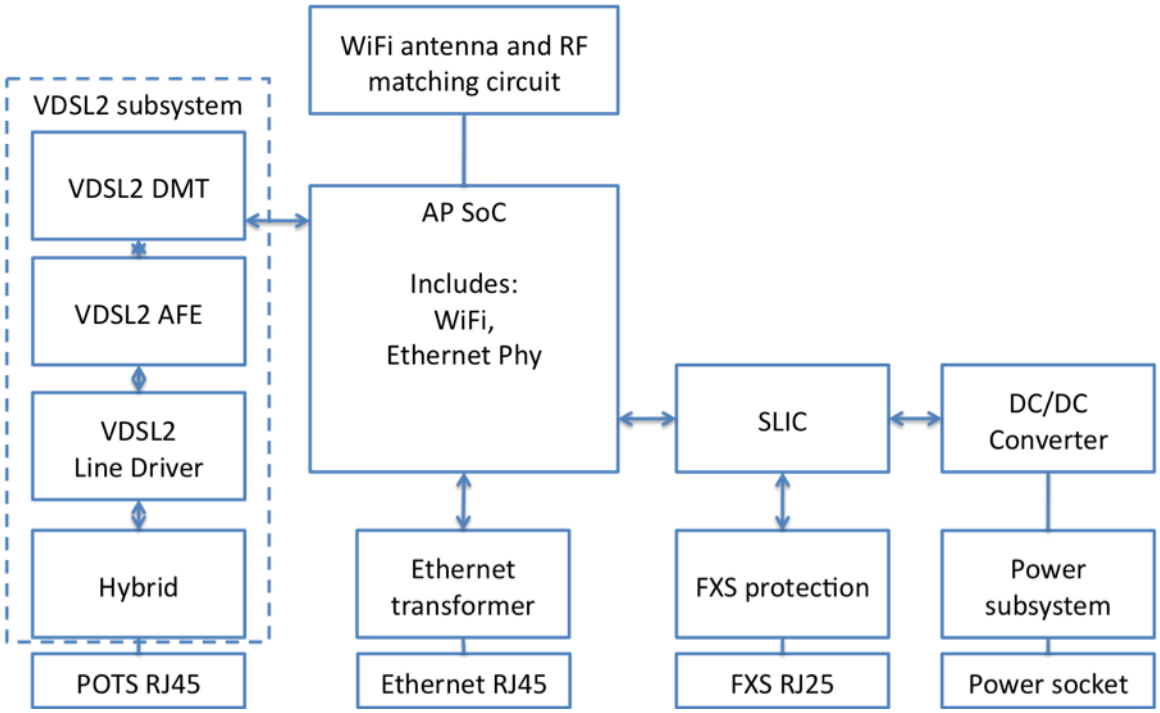

Figure 3: VDSL2 chipset completely independent of the SoC

3.3.4 VDSL2 chipset completely independent of the SoC with additional GSM backup

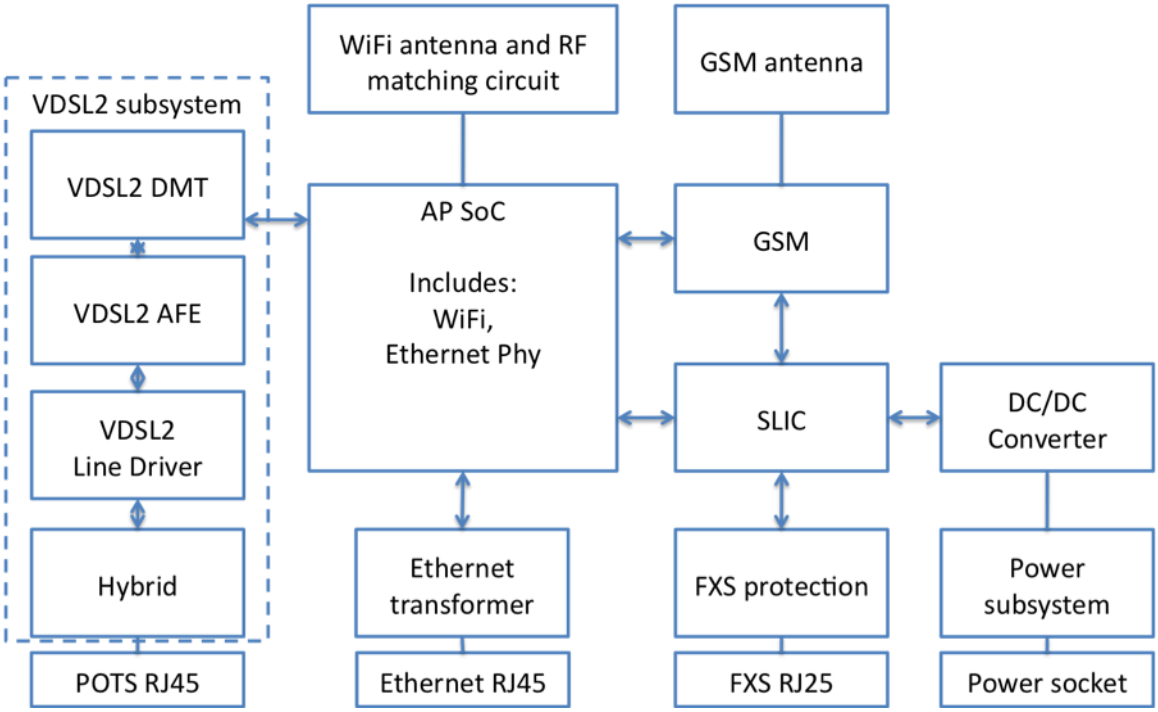

Figure 4: VDSL2 chipset completely independent of the SoC with additional GSM backup

3.4 Block level SW architecture

The block level software (firmware) architecture of the LPRG is presented on the diagram below.

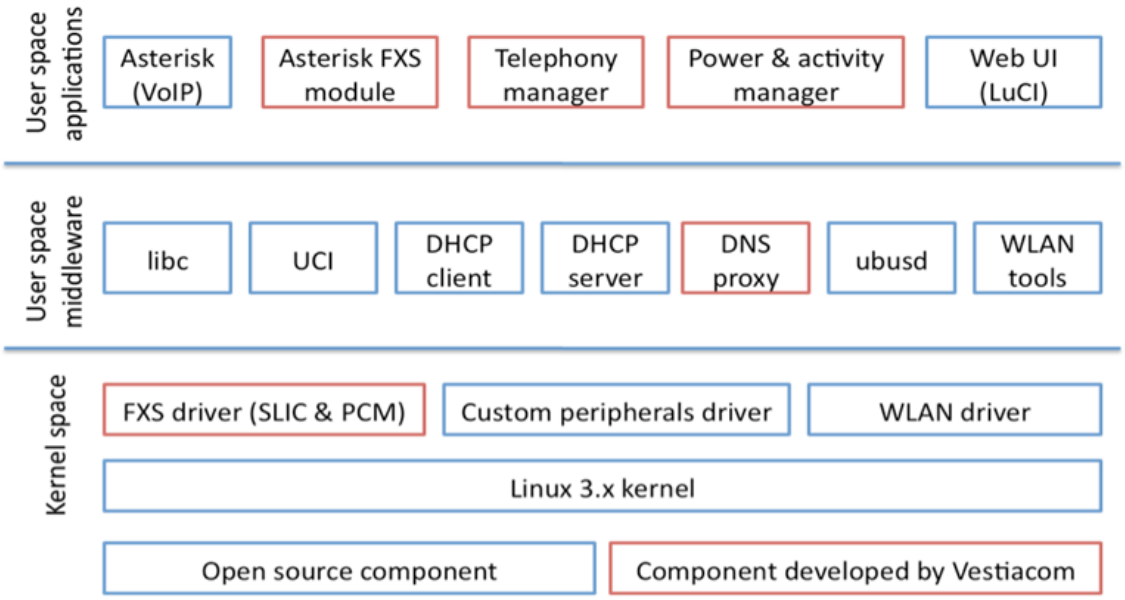

Figure 5. SW architecture

3.5 High-level functional description of the SW

Functional description is divided into the following 3 groups:

- Functions that are active in all modes
- Functions that are active only in the normal power modes (M2 and M3)
- Functions that are active only in the low power modes (M0 and M1)

3.5.1 Functions active in all modes

The following software functions are active in all modes:

- Collecting power consumption data
- Executing power scheduler events (switches between low power and normal power modes)

3.5.2 Functions active only in the normal power modes

The following software functions are active only in normal power modes:

- Collecting usage data (calls, internet usage, WLAN associations)
- Sending collected usage and power consumption data to the cloud
- Handling incoming and outgoing VoIP calls (Asterisk)
- Enabling/disabling incoming call forwarding to GSM number
- Handling Internet/WAN access

3.5.3 Functions active only in the low power modes

The following software functions are active only in the low power modes:

- Handling incoming GSM calls and routing them to FXS
- Handling outgoing FXS calls and routing them via GSM module
- Initiating switch to normal power mode on any of the following events:
    - Button press
    - Incoming GSM call
    - FXS handset off-hook
    - User generated WAN/Internet access

3.5.4 Description of the GSM backup approach

One of the required functions of the LPRG is FXS port for connecting an analogue phone that gateway connects to via VoIP to Swisscom. During low power mode when VDSL2 subsystem is switched off the VoIP is not possible and thus neither incoming calls nor outgoing calls would be possible. In order to address this issue a GSM backup has been proposed.

It is intended to work in such a way that when the gateway decides to switch to low power mode it sends a request to the soft switch to setup an unconditional call forwarding of the incoming calls to the GSM number assigned to the gateway (gateway includes built-in GSM SIM card). Then after the return to the normal power mode the gateway sends another request to the soft switch to cancel the call forwarding. This way incoming calls are possible regardless of the power mode of the gateway.

The outgoing calls are also handled via the GSM. When the gateway switches to the low power mode it reconfigures the handling and signalling of the FXS socket such that outgoing calls are not handled by VoIP but rather by the GSM module.

It is up to Swisscom to decide if all outgoing calls should be handled via GSM backup or only calls to the emergency numbers.

If Swisscom decides to allow only emergency outgoing calls via GSM backup then it can be done in such a way that after the user dials the number there is an announcement that the call is being setup and it will take a little longer because the Internet connectivity needs to be re-established. The average time to setup VDSL2 is between 30 and 60 seconds, but the LPRG initiates this process as soon as the user picks up the handset of the phone connected to FXS port.

Once the call via the GSM backup is established it is NOT handed over to VoIP even if during the call the VDSL2 connectivity is re-established. Naturally once the VDSL2 connection is re-established VoIP handles all new incoming as well as outgoing calls again.

3.6 Phase summary

State of the Art concerning energy consumption in DSL systems was identified. During the initial evaluation of possible approaches of building a residential gateway that would on average consume not more than 2 Watts it became apparent that achieving this goal:

- Is NOT possible by ONLY using the most energy efficient chipsets;
- Is NOT possible by activating all standard low power consumption modes of all residential gateway subsystems;
- CAN be achieved by using the most power efficient design AND switching the entire VDSL2 subsystem off when it is not required.

However, due to the fact that this residential gateway includes one VoIP based FXS port the design must allow as a minimum incoming calls as well as outgoing alarm calls even when the VDSL2 subsystem is switched off. In order to achieve this requirement a GSM based fallback was proposed. Therefore the HW architecture based on the **VDSL2 chipset completely independent of the SoC with additional GSM backup** was selected.

During this phase of the project Vestiacom also found and signed a contract with Telecommunications Department at Warsaw University of Technology for the technical support in the areas of HW design and VDSL2 related issues. The Telecommunications Department has the necessary experience and equipment (lab) to design, build and test VDSL2 CPE.

Vestiacom started working on this phase of the project started on 1/11/2012 and it was completed on 15/12/2012.

4 Phase II

4.1 VDSL chipset selection

Several VDSL2 chipsets from different vendors were analyzed. They are summarized in the table 3 below.

Vendor	Chipset	Description	Applications
Broadcom	BCM 6368	System on chip, includes VDSL2 DMT and AFE (without line driver) Single-chip VDSL2/ADSL2+ integrated access device (IAD) solution with seamless, multiuser support for 10/100/1000 Ethernet, USB 2.0 host and devices, ISDN, DECT, multichannel VoIP, and IEEE 802.11a/b/g/n wireless home networking. VDSL2/ADSL2+ auto-detecting, G.933.2 (vdsl2), G.992.1, G.992.2, G.992.3, G.992.5, and T1.413-compliant DSL transceiver. Estimated power consumption: 3319 mW	Alcatel Cellpipe 7130 ZTE ZXDSL931CII ZyXEL P-2812HNU-51c Freebox
	BCM 63168/63268	System on chip, includes VDSL2 DMT and AFE (without line driver) The BCM63168 single-chip multi-mode ADSL2+/VDSL2 Integrated Access Device (IAD) SoC. BCM63168 xDSL IAD SoC integrates multi-mode ADSL2+/VDSL2, supporting 5-band channel bonding with 802.11n, DECT, VoIP and Ethernet Switching into a single chip. WLAN included, without front-end module (FEM). Estimated power consumption: 3567 mW	Swisscom Internet Box (Will be introduced in 2014)
Ikanos (Conexant)	DA87781	System on chip, includes VDSL2 DMT and AFE DA87781 VDSL2 chipset is targeted at Ethernet bridges, routers, wireless local area network (WLAN) and broadband residential gateways, and integrated access devices (IADs). Compliant with ITU-TVDSL2/G.993.2, VDSL/G.993.1 ITU-T, ANSI T1-424, ETSI TS 101270, and China MII VDSL standards	2Wire/Pace VDSL2 Residential Gateways, the 3600HGV and 3800HGV
	Vx180/IFE-6	System on chip, includes VDSL2 DMT and AFE Chipset Processor for Multi-mode VDSL2/ADSL2+ Residential Gateways. Integrated Multi-mode DSL Data pump supporting VDSL2, ADSL2+, ADSL2 and ADSL. Integrated Dedicated Voice Processing Engine. 2x GMII/MII/RMII Interfaces. PCI Interface	DSL-6641K and selected models of FRITZ_Box
Lantiq	VRX268	System on chip, includes VDSL2 DMT Chip-Set - True Universal DSL Router Solution. 6-band DSL System-on-Chip (SoC) in combination with 6-band and single chip Analog Frontend and Line Driver (AFE and LD) XWAY™ VRX208. Supports all profiles and band-plans up to 30A.	ECI B-FoCuS CPE used by BT Openreach
	VRX288	System on chip, includes VDSL2 DMT VDSL2/ADSL2/2+ True Universal DSL Gateway Solution for Triple-play Applications/Gigabit Ethernet. System-on-Chip (SoC) in combination with 6-band single chip Analog	Arcadyan modems

Vendor	Chipset	Description	Applications
		Frontend and Line Driver (AFE and LD) XWAY™ VRX208 (AFE/LD).	
	VRX208	VDSL2 AFE Analog functions necessary for receiving and transmitting data. Operates with VRX268 and VRX 288.	
PMC-Sierra	PM4380	VDSL2 AFE Customer Premises Equipment (CPE). Suitable for VDSL2 and VDSL CPE, and is fully backwards compatible with ADSL2+, ADSL2, and ADSL interface technologies	Uverse 3801HGV
Metanoia Comms	MT2311	VDSL2 DMT Programmable Discrete Multi-Tone (DMT) Digital Subscriber Loop (DSL) digital modulator/ demodulator processor units for broadband access. Device supports all committee T1E1.4 and ITU-T G.993.2 DSL discrete multitone based specifications, as well as IEEE 802.3 10PASS-TS. Estimated power consumption: 341mW	Draytek VDSL2 Vigor 2850n modem Planet VC-230N
	MT3302	VDSL2 AFE Provides all analog functions necessary for receiving and transmitting data. Includes integrated line driver. A serial control interface allows programming of a various functional blocks. Power back off linked with power down for every block provides the flexible power saving properties. Estimated power consumption: 1440mW	
Triductor	TRI-VSPD210	VDSL2 DMT xDSL Customer Premise Equipment for internet access and single port router. TRI-VSPD210 integrates VDSL2/ADSL2 DSP transceiver, TPS PTM and ATM SAR, 5X5 Switch/Router, GMAC Estimated power consumption: 582mW	
	TRI-VSPA210	VDSL2 AFE (without line driver) Provides all analogue functions necessary for receiving and transmitting data. Includes line driver. It supports all VDSL2 profiles including 8a, 8b, 8c, 8d, 12a, 12b, 17a and 30a. It can also support ADSL/ADSL2+ standards. It integrates the high performance ADC, DAC, filter and DCXO. Estimated power consumption: 1350mW	

Table 3: VDSL chipset selection

All SoC solutions that integrate (fully or partially) VDSL2 function into the SoC were discarded because they would not allow switching the VDSL2 subsystem completely off and thus achieve maximum power saving during the low power modes M0 and M1.

After the analysis, taking into consideration power consumption, functional parameters (such as support for VDSL2 Vectoring), and the readiness of the vendor to support this kind of project the Metanoia chipset (MT2311 DMT and MT3302 AFE) was selected as a the most suitable for further implementation.

4.2 Possible HW architectures

The following 2 different options were considered:

- SoC based on Texas Instruments AM1802 ARM Microprocessor with an external (connected with SDIO) WiFi module (Qualcomm/Atheros AR6103)
- SoC based on Qualcomm/Atheros AR9331 AP SoC that has WiFi AP function integrated

In both options the following subsystems are the same:

- VDSL part consisting of Metanoia DMT MT2311 chip and AFE MT3302,
- Silicon Labs Si32178 Subscriber Line Interface Circuit,
- Huawei Mu509 GSM module,
- DRAM and SPI Flash.

The power estimations presented for both options do not include the power consumption of the GSM module while it is in use (talk time), which is approx. 1100mW. This only happens when there is a GSM call (incoming or outgoing) while the LPRG is in the low power mode. This is assumed to be very rare case and thus this additional power consumption is negligible.

4.2.1 Texas Instruments AM1802 Option

The hardware architecture of the AM1802 based option is presented on the diagram below.

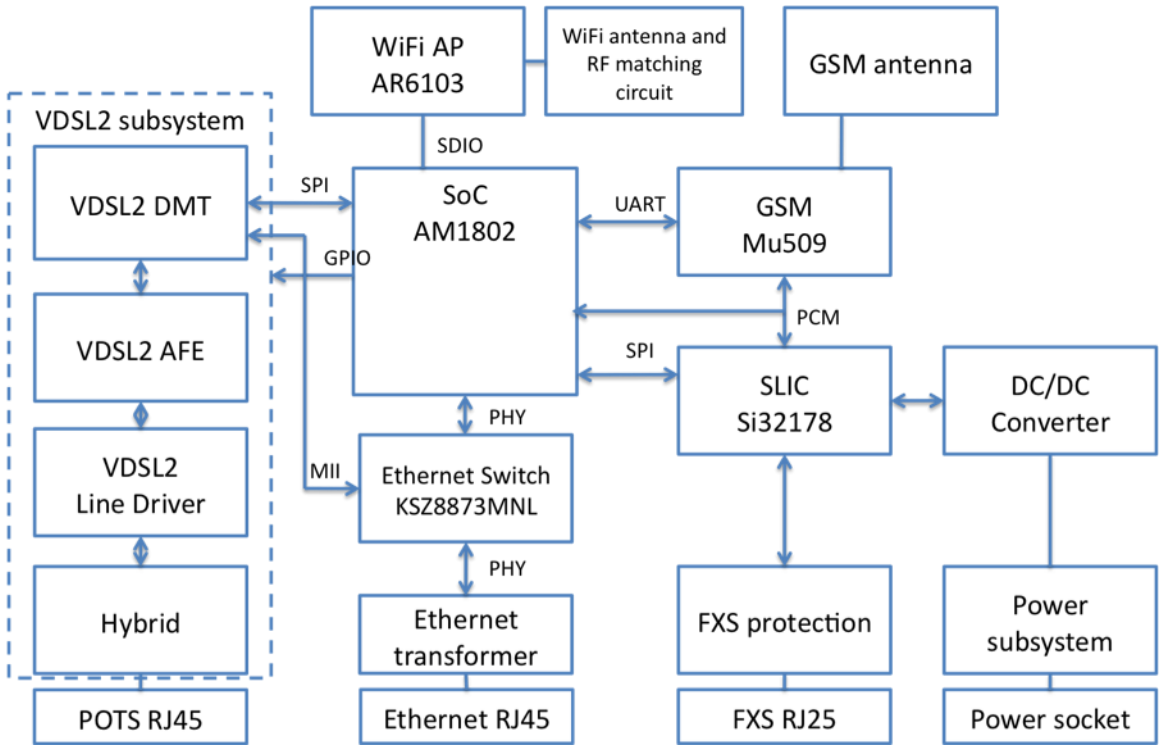

Figure 6: Texas Instruments option

In the table below estimated power consumption for 4 different modes of the AM1802 based option is presented.

Component	**M0 [mW]**	**M1 [mW]**	**M2 [mW]**	**M3 [mW]**
SoC - AM1802	402	402	402	402
VDSL2 DMT - MT2311	0	0	342	342
VDSL2 AFE - MT3302	0	0	1440	1440
Switch - Micrel KSZ8873MNL - energy detect	50	50		
Switch - Micrel KSZ8873MNL - ports active			347	347
WiFi - AR6103 - sleep mode	0.4			
WiFi - AR6103 - receive only		172	172	
WiFi - AR6103 – transmit				686
SLIC - Silabs Si32178 - on-hook	79	79	79	
SLIC - Silabs Si32178 – talk				325
DRAM	270	270	270	270
GSM Module - Huawei Mu509	12	12	12	12
Total	**813.4**	**985**	**3064**	**3824**

Table 4: Power consumption in the different power modes

4.2.2 Qualcomm/Atheros AR9331 Option

The hardware architecture of the AR9331 based option is presented on the diagram below.

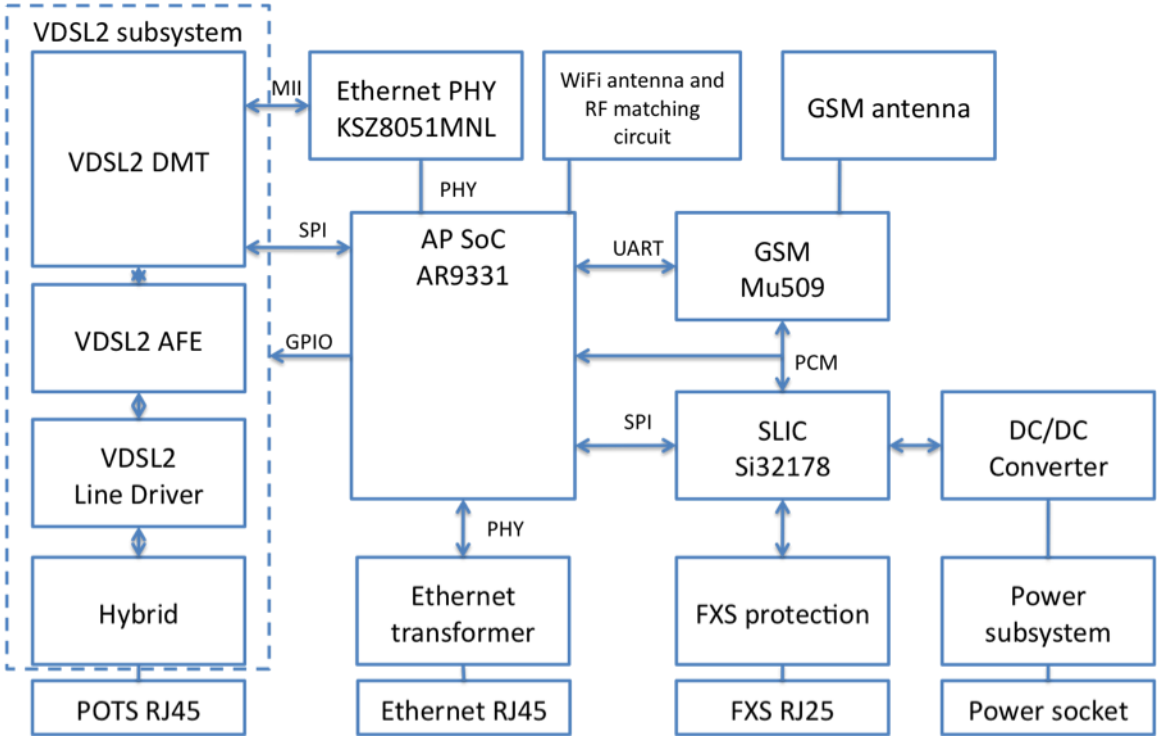

Figure 7: Qualcomm / Atheros Option

In the table below estimated power consumption for 4 different modes of the AR9331 based option is presented.

Component	**M0 [mW]**	**M1 [mW]**	**M2 [mW]**	**M3 [mW]**
SoC - AR9331 - WiFi off	360			
SoC - AR9331 - WiFi receive only		615	615	
SoC - AR9331 - WiFi transmit				1304
VDSL2 DMT - MT2311	0	0	342	342
VDSL2 AFE - MT3302	0	0	1440	1440
Phy - Micrel KSZ8051MNL	0	0	162	162
SLIC - Silabs Si32178 - on-hook	79	79	79	
SLIC - Silabs Si32178 – talk				325
DRAM	270	270	270	270
GSM Module - Huawei Mu509	12	12	12	12
Total	**721**	**976**	**2920**	**3855**

Table 5: estimated power consumption in the different power modes

4.3 Selected HW architecture

Presented estimated power consumptions indicate that for both schemes the power consumption is on similar level. **Considering lower complexity of the second scheme (based on AR9331 SoC) this solution was chosen for possible implementation.**

Therefore the main elements of the system solution chosen for further implementation and evaluation were the following:

- System on Chip with Wi-Fi capabilities (always on)

  Qualcomm/Atheros AR9331

- VDSL2 realization (switched off in low power modes)

  Metanoia MT2311 (DMT functions)

  Metanoia MT3302 (AFE functions)

- Subscriber Line Interface Circuit (FXS)

  SiLabs Si32178

- GPS module for calls handling when VDSL is switched off in low power modes

  Huawei MU509

- Ethernet to PHY transceiver – required to connect MII of MT2311 with Phy of AR9331

  Micrel KSZ8051MNL

- Voltage regulators for 5V, 3.8V, 3.3V, and 2.6V
- Transformers and sockets for VDSL, Ethernet and FXS user end

4.4 Phase summary

This phase started with a review of VDSL2 for customer premises equipment (CPE) chipsets available on the market. Based on that review Metanoia VDSL2 chipset was selected. Then 2 possible alternatives for the remaining HW architecture were analysed and since the estimated power of both of these alternatives was similer, the less complex (based on AR9331 AP SoC) was selected. After that the remaining components of the desired architecture were selected. We have started ordering the necessary development kits and evaluation boards that were required to assemble the first working prototype.

Vestiacom together with designed staff from the Telecommunications Department of Warsaw University of Technology started working on this phase of the project started on 15/12/2012 and it was completed on the 18/02/2013.

5 Phase III

5.1 System evaluation

Based on the findings in the Phase II an initial functional prototype assembled from the available evaluation boards and reference designs was built. In particular the following components were used:

- AP 121-050 Reference board replaced later with Oolite dev board (AR9331 SoC functions with W-Fi),
- Metanoia EVB2311-BL/E consisting of MT2311 and MT3301 (VDSL2 functions),
- FX S110M later replaced with Silabs Si32176/8 EVB (FXS),
- Huawei GSM/UMTS Mu509 evaluation kit,
- Purpose built integration board that made the connection of the above modules possible. The evaluation board also included real-time total power measuring as well as measuring of the power consumption of individual functional blocks (SoC, VDSL2, FXS and GSM).

The following diagram shows how the components of this prototype were connected.

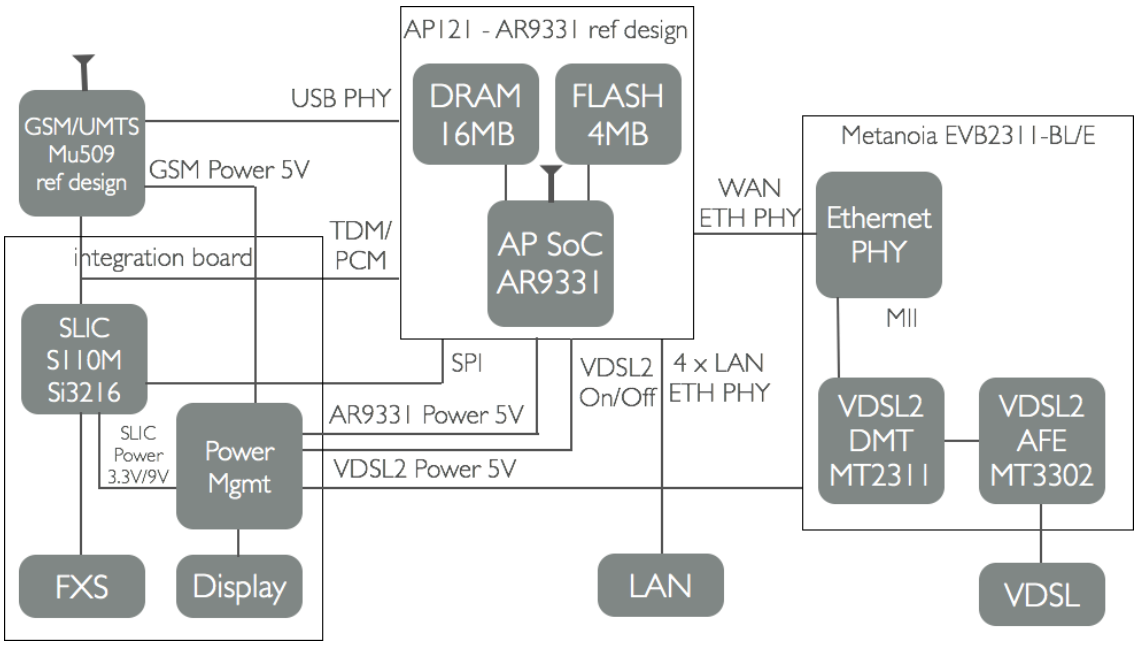

Figure 8: design of prototype

5.2 Power consumption

The following table presents the measured power consumption of the individual elements of the prototype.

Component	M0 [mW]	M1 [mW]	M2 [mW]
AP121 (AR9331) - WiFi off	360		
AP121 (AR9331) - WiFi idle (receive only)		660	660
Metanoia EVB2311-BL/E	0	0	2200
SLIC - S110M - on-hook	40	40	40
SLIC - S110M – talk			
GSM Module - Huawei Mu509 ref. Design	200	200	200
Total	**600**	**900**	**3100**

Table 6: measured power consumption

5.3 Phase summary

The prototype assembled from the readily available evaluation boards and development kits was built and brought up. The prototype has been connected to the Swisscom VDSL2 line in the Swisscom lab and was able to synchronize and send/receive data over the VDSL2 connection. It was also presented to the Swisscom.

Vestiacom with the help of designed staff from the Telecommunications Department of Warsaw University of Technology started working on this phase of the project started on 19/02/2013 and it was completed on the 28/04/2013.

6 Phase IV

The main goal of this phase was to complete the gateway and server software and manufacture LPRG functional prototypes.

Software development related activities in the phase IV:

- Server software (written in PHP and deployed on http://lprg.vestiacom.com/) that offers LPRG users a web interface, which allows:
    - Creating a user account and associating LPRG with this account
    - Configuring the gateway (GSM call forwarding on/off numbers, non-user generated Internet access rules, scheduler)
    - Viewing the history of the gateway consumption and state transitions
    - Viewing the history of the user's activity
- Scheduler that switches the mode of operation of the LPRG according to the predefined weekly schedule (defined by the user in the backend)
- Power consumption monitoring that collects real time LPRG power consumption and uploads it to the backend (when LPRG is in normal mode)
- Captive portal that is displayed when the user is trying to access the Internet while the LPRG is in low power mode
- Custom DNS proxy that acts as a regular DNS proxy when the LPRG is in the normal mode and as a fake DNS server when LPRG is in the low power mode
- User activity monitor that:
    - While LPRG is in normal power mode stores the user activity and uploads it to the server
    - While LPRG is in low power mode monitors user's activity (LAN/WLAN traffic, FXS handset off-hook, LPRG button press) and determines when the LPRG should be brought back to normal power mode

Hardware development related activities in the phase IV:

- Initial Cut-1 schematics and PCB layout
- Review of the Cut-1 schematics and PCB layout by Metanoia
- Cut-1 production (1 pcs)
- Cut-1 bring up
- Cut-2 schematics and PCB layout
- Cut-2 production (2 pcs)
- Cut-2 bring up

6.1 Final HW design

The final HW design is presented on the drawing below. Both Cut-1 and Cut-2 baords produced during this phase where based on this design.

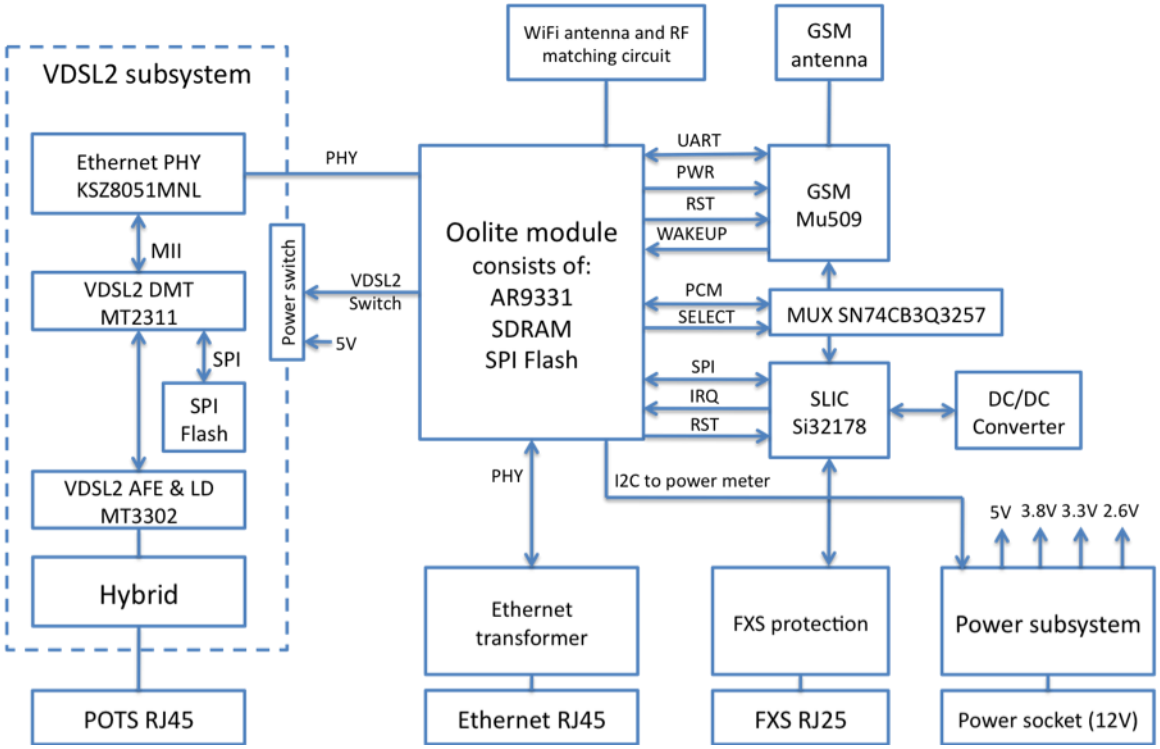

Figure 9: Final HW design

6.2 Power consumption measurements

In the table below power consumption measurements for 4 different modes are presented.

Mode	Description	Measured Power [Watt]	Average duty hours per day	Average con-sumption [Watt]
M0	VDSL is off, devices are inactive with the exception of modules responsible for in-coming calls handling	0.876	12	10.512
M1	VDSL is off, all other parts active but not in use8	1.032	4	4.128
M2	all devices and ports are active but not in use	3.756	6	22.536
M3	all ports are in use	4.800	2	9.6
			Average	**1.95**

Table 7: Power consumption measurements

6.3 Phase summary

It was assumed that 2 to 3 PCB cuts would be required to get the fully working prototype. The Cut-1 prototype was built in quantity of 1. There were several HW bugs that had to be fixed before it was fully operational. However, it was possible to achieve that with minor PCB modifications. There were also few mechanical problems, which prevented installing the prototype in the Centro Grande case.

In the design of Cut-2 PCB all issues discovered in Cut-1 were addressed.

Vestiacom started working on this phase of the project started on 29/04/2013 and it will be completed on the 26/11/2013. The more detailed timeline of this phase is outlined in the table below.

Activity	**Start**	**End**
Cut-1 schematics & PCB design	28/04/2013	29/07/2013
Cut-1 schematics & PCB review by 3rd party and Metanoia	1/08/2013	13/09/2013
Cut-1 production (1 pcs) 2 weeks	14/09/206	2/10/2013
Cut-1 bring up 2 weeks	3/10/2013	18/10/2013
Cut-2 schematics & PCB layout	19/10/2013	30/10/2013
Cut-2 production (2 pcs)	31/10/2013	20/11/2013
Cut-2 bring up	20/11/2013	22/11/2013
Cut-2 delivery		26/11/2013

Table 8: PCB Cut phases

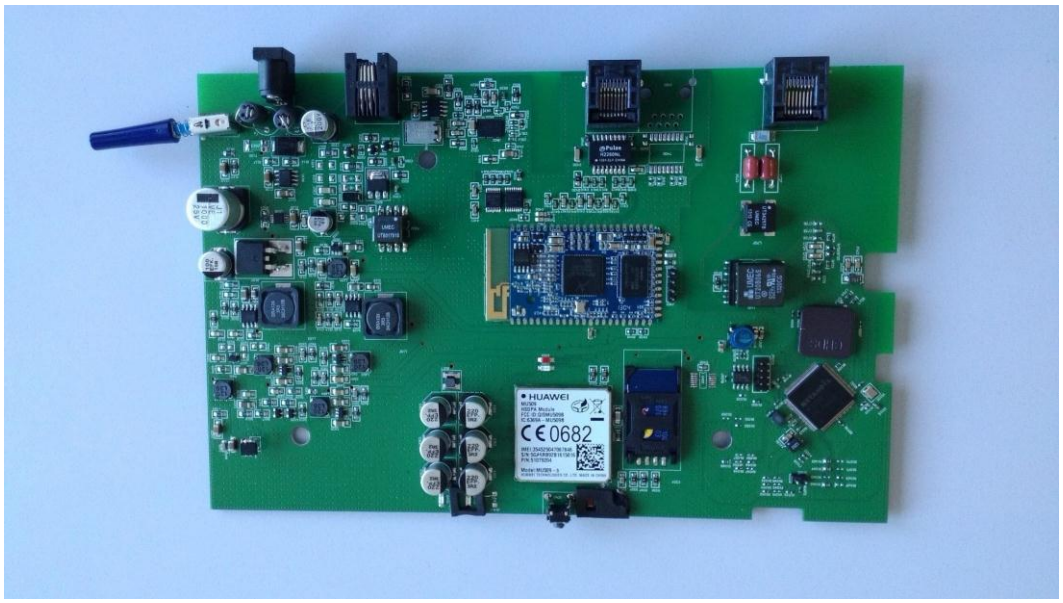

Figure 10: PCB Final Layout

7 Project summary and conclusions

During the project we evaluated several approaches of how to reduce the power consumption of a residential gateway. We identified that the only effective method to reduce the average power consumption of a residential gateway is to introduce a HW and SW mechanisms that will allow switching off the entire VDSL2 subsystem when it is not used for longer period (e.g. over night) together with using the most power efficient remaining components.

Conceptual model based on the technical data provided by the chip manufacturers was initially verified using reference designs and development kits. Such initial prototype also allowed to confirm the correctness of the design in regard to its functional requirements.

In the next phase the “real” LPRG schematics and PCB was designed. The design (both schematics and PCB) passed an external review by the VDSL2 chip vendor (Metanoia). Once the review was finished the Cut-1 board was produced and brought up.

The HW issues identified during the bring-up of the Cut-1 PCB and corrected in the Cut-2 PCB.

In parallel with the HW development activities special software was created for the gateway as well as management server software that allows the user to monitor the LPRG power consumption profile and define the times when the gateway should switch to low power mode.

The overall target of the project has been achieved. We managed to build a prototype (hardware and software) of a residential gateway that with a specific usage profile consumes less than 2 Watt on average and at the same time has all the features stated in the project requirements.

The next step towards introduction of the LPRG to the market is industrialization of both HW and SW. Additional work on the SW may involve introduction of the Artificial Intelligence algorithms that would look at the LPRG usage history and automatically define when the LPRG should switch to low power mode.

8 Outlook

In 2014 the prototype should be at a stage of development that would allow us to test it in 200 households in Switzerland.

In order to do so the following steps are necessary:

1. Make the PCB hardware ready for mass production (CE Approval level)
2. Production of a suitable casing
3. Selection of the most efficient power supply
4. Production of 200 devices

As soon as the 200 test devices are ready, they will be dispatched to customers for testing. The test phase is closely accompanied and observed by Swisscom through regular questionnaires, surveys and tests on the server side, allowing to measure the energy consumption.

The objective of those observations is to determine whether this energy saving device will be received with high acceptance by the customers and also to identify weaknesses that we need to work on further.

Another objective is to evaluate the various user profiles and, based on those, to develop an algorithm that - depending on the customer - would automatically adapt the router in order to bring it into the optimal power consumption mode.

Based on the experiences made with the 200 tests customers, we will define the next steps. In the best case we would be able to further develop the product into a mature, mass-launch ready router that we could offer our customers as an energy-efficient option from 2015.

Furthermore, those activities would also allow us to intensify the discussions with the chip suppliers and have a significant influence on the industry in general.

9 Glossary

Name	Description
ADSL	Asymmetric Digital Subscriber Line
AFE	Analogue Front End
BOM	Bill Of Material
CPE	Customer Premises Equipment
CO	Central Office
DHCP	Dynamic Host Configuration Protocol
DMT	Discrete Multi Tone Discrete multi tone modulation is used by VDSL2. The DMT modulation is a method of separating a digital subscriber line signal so that the usable frequency range is separated into 256 frequency bands (or channels) of 4.3125 KHz each.
DNS	Domain Name System
DSLAM	Digital Subscriber Line Access Multiplexer
EVB	Evaluation Board
FXS	Foreign eXchange System
Hybrid	Hybrid coil A transformer that has three windings, and which is designed to be configured as a circuit having four branches, (i.e. ports) that are conjugate in pairs.
IAD	Integrated Access Device
LD	Line Driver
LPRG	Low Power Residential Gateway
MAC	Medium Access Control
PCB	Printed Circuit Board
PCM	Pulse code Modulation
PHY	PHYsical layer
POTS	Plain Old Telephony System
PTM	Packet Transfer Mode Transport of packet-based services method based on the EFM IEEE802.3ah standard.
SLIC	Subscriber Line Interface Circuit
SoC	System on Chip
TDM	Time Division Multiplexing
VDSL	Very-high-bit-rate Digital Subscriber Line VDSL is a DSL technology that provides data transmission over a single, flat, untwisted or twisted pair of copper wires at faster rate.
VDSL2	Very-high-bit-rate Digital Subscriber Line 2nd generation VDSL2 is an enhancement to G.993.1 (VDSL) that permits the transmission of asymmetric and symmetric (full duplex) aggregate data at faster rate. VDSL2 is based on ITU-T G.993.2 (VDSL2) standard.
VDSL2 Vec-	Digital signal processing (DSP) computations involved to cancel the crosstalk between the pairs

toring	in the cable bundle http://www.gazettabyte.com/home/2012/11/9/vdsl2-vectoring-explained.html
VoIP	Voice over IP
WiFi/WLAN	Wireless Fidelity/Wireless LAN
WPS	Wireless Protected Setup

Table 9: Glossary